

28. (a) There are in total 16 non-trivial twiddle factors.
- (b) Consider, for example, the calculation of the three implementations. To compute an FFT of length N , a hardware-mapped approach takes 1 cycle, whereas a pipelined architecture needs 2 cycles and a time-multiplexed $N/2 \cdot \log_2 N$ cycles.
- (c) Either in- or output sequences appear in bit-reversed order.
29. In total, one needs $N + M$ points in the DFT. See also the preparation to Lab 1 for more information.
30. (a) There are in total 5 loops. The maximum loop bound is $T_\infty = 8$ t.u. The iteration period is determined by the critical path along **A-E-C**, which is 22 t.u. The sample rate is thus $1/22$.
- (b) The retimed DFG is shown in Figure 11. The iteration period is now 10 t.u. (computation time of node A), which is larger than the iteration bound and cannot be reduced by means of retiming.
- (c) Unfolding the original DFG with $J = 2$ results in a critical path along $A_0 - E_0 - C_0 - D_1$, that is, 28 t.u. which is equivalent to a sample rate of $1/14$. The unfolded retimed DFG (first retiming and then unfolding or vice versa gives the same result) has an iteration period of 18 t.u. which gives a sample rate of $1/9$. Apparently, this rate is larger than the sample rate of the original retimed DFG.

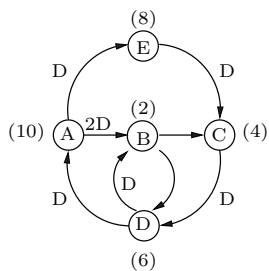


Figure 11: Retimed DFG.

31. The unfolded bit-serial adders for the $J = 4, 5$ are shown in Figure 12(a) and Figure 12(b), respectively.

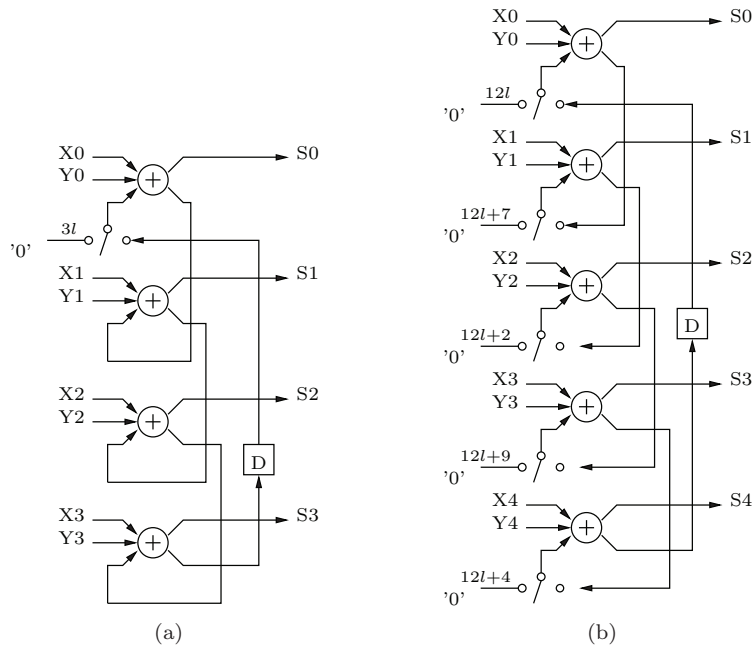


Figure 12: Unfolded bit-serial adder with factors $J = 4$ (a) and $J = 5$ (b).