12. (a) Considering the two critical paths **A-C-E-G** and **B-D-F-H**, the maximum sample rate becomes $f_s = 1/4T$.

    (b) According to Figure 1, 9 additional registers are needed.

    (c) Keeping only the cutset in the middle, only 4 registers are required and the sample rate becomes $f_s = 1/2T$, that is, one trades area for throughput.

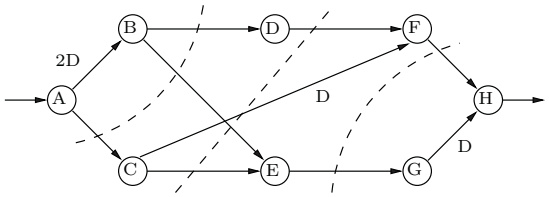

Figure 1: Feedforward cutsets in a DFG.

13. (a) The critical path is 10 t.u. and is shown bold in Figure 2.

    (b) The pipelining cutsets are shown dashed in the figure. There is an overhead of 9 registers. The lowest achievable clock period would be $T_\infty = 1.5$.

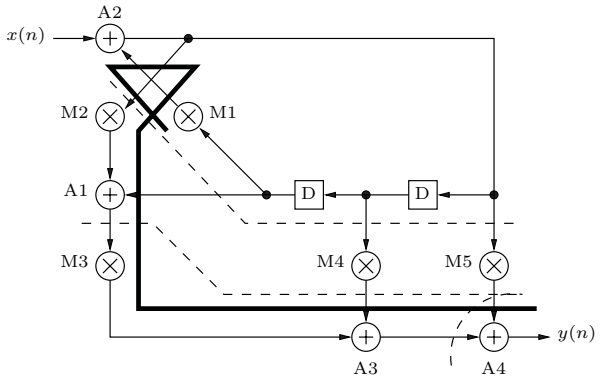

Figure 2: Digital IIR filter with critical path and cutsets.

14. (a) The pipeline is shown in Figure 3.

    (b) In the algorithm, substitute n with $3k$, $3k+1$, and $3k+2$. The 3-parallel filter is shown in Figure 4. The pipeline achieving a clock period of T is shown dashed and the sample rate is $3/T$.

    (c) A pipeline to achieve a critical path of $T/2$ is applied to the multipliers (fine-grain pipelining) since these units are the critical factor. The sample rate is now $6/T$.

15. (a) The pipelined filter is shown in Figure 5(b).

    (b) First slow down the filter by replacing the 2-delay with a 4-delay, thus there appears an idle cycle in every two cycles. These idle cycles are

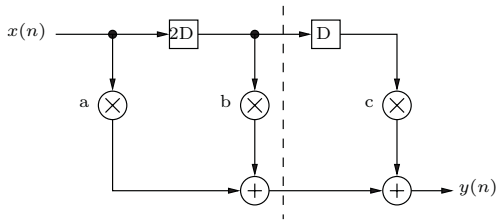

Figure 3: Pipeline in an FIR-filter.

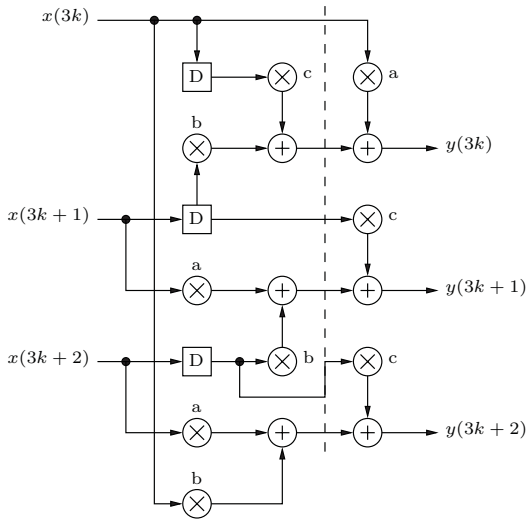

Figure 4: 3-parallel FIR filter.

used to operate $v(n)$. The scheduling is shown in Table 1 and the respective architecture in Figure 6.

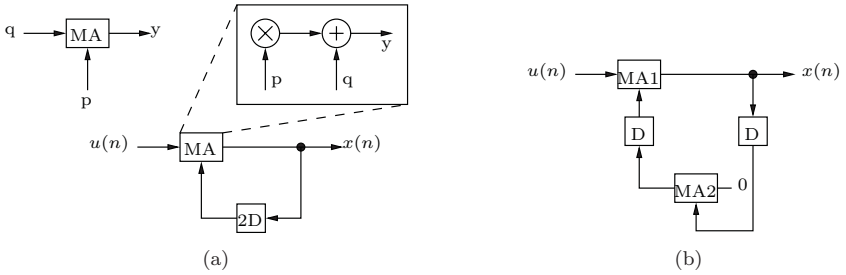

Figure 5: The original filter (a) with a multiply-add (MA) unit. In (b), the pipelined version is shown.

16. See pages 9–11 from the lecture about pipelining and parallel processing. Although only switching power consumption is considered in the following

Table 1: Scheduling of data, v, y are idle samples.

	1	2	3	4	5	6
Input	$u(1)$	$v(1)$	$u(2)$	$v(2)$	$u(3)$	$v(1)$
Output	$x(1)$	$y(1)$	$x(2)$	$y(2)$	$x(3)$	$y(1)$

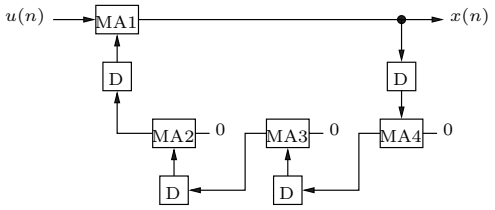

Figure 6: Pipelined structure of the 2-slow IIR filter.

assignments, leakage power becomes increasingly important as technology shrinks.

17. (a) See page 12 from the lecture about pipelining and parallel processing.
    (b) Given $M = 7/4$, the power ratio β can be derived from

$$M(\beta V_{\mathrm{dd}} - V_{\mathrm{t}})^2 = \beta(V_{\mathrm{dd}} - V_{\mathrm{t}})^2$$

18. As required, both filters have equal clock periods, thus

$$\frac{C_{\mathrm{ch,a}} \cdot V_{\mathrm{dd,a}}}{k(V_{\mathrm{dd,a}} - V_{\mathrm{t}})^2} = \frac{C_{\mathrm{ch,b}} \cdot V_{\mathrm{dd,b}}}{k(V_{\mathrm{dd,b}} - V_{\mathrm{t}})^2}$$

    Knowing that (a) has $T_{\mathrm{crit}} = 9T_{\mathrm{add}}$ and (b) $T_{\mathrm{crit}} = 4T_{\mathrm{add}}$, one can write

$$\frac{V_{\mathrm{dd,b}}\,(V_{\mathrm{dd,a}} - V_{\mathrm{t}})^2}{V_{\mathrm{dd,a}}\,(V_{\mathrm{dd,b}} - V_{\mathrm{t}})^2} = \frac{C_{\mathrm{ch,a}}}{C_{\mathrm{ch,b}}} = 9/4.$$

    Solving for $V_{\mathrm{dd,b}}$, one yields an expression for the saved power according to

$$1 - \frac{V_{\mathrm{dd,b}}^2}{V_{\mathrm{dd,a}}^2}.$$

19. This assignment is best solved by writing a program that calculates β^2 for different values of M. One should end up with an optimal pipeline level of $M = 13$, which gives a supply voltage of 1.0929V and $\beta^2 = 82.83\%$.

20. Given a pipelining level of $M = 4$ and block size $L = 4$, we get

$$16\,(\beta V_{\mathrm{dd}} - V_{\mathrm{t}})^2 = \beta(V_{\mathrm{dd}} - V_{\mathrm{t}})^2.$$

    Solving for β gives a power ratio of $\beta^2 = 3.12\%$.

21. By simply writing out the equations, one should arrive at the same algorithmic structure.

(a) For a general L-parallel filter, one has L^2 subfilters of length N/L, N number of taps. Therefore, the total number of multiplications and additions is LN and $L(N-1)$, respectively. Since every arithmetic operation is duplicated, the complexity per sample compared to the original non-parallelized filter stays the same. For the fast-FIR approach, there are only $(2L-1)$ subfilters of length N/L, and the number of mults and adds are reduced to only $(2N - N/L)$ and $(2L-1)(N/L-1)+2L$. Therefore, the complexity per sample is also reduced when comparing it to the original form.

(b) The critical path of the decomposed form has the same properties as that of the original filter since it is only a duplication of operations. The fast-FIR filter, though, has got an increased critical path due to pre- and postprocessing operations.

(c) See (a).

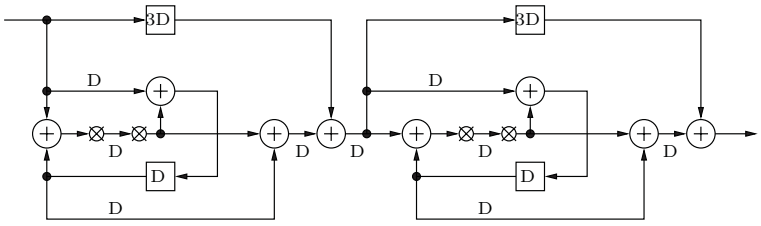

Figure 7: Retimed and pipelined wave digital filter structure.

22. The 2-parallel FIR filter is expressed in post-, pre-, and diagonal matrices are expressed as follows:

$$\mathbf{Y_2} = \mathbf{Q_2 H_2 P_2 X_2},$$

where

$$\begin{pmatrix} Y_0 \\ Y_1 \end{pmatrix} = \begin{pmatrix} 1 & 0 & z^{-2} \\ 1 & -1 & 1 \end{pmatrix} \operatorname{diag} \begin{pmatrix} H_0 \\ H_0 - H_1 \\ H_1 \end{pmatrix} \begin{pmatrix} 1 & 0 \\ 1 & -1 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} X_0 \\ X_1 \end{pmatrix}.$$

By transposing the matrices, another 2-parallel structure is obtained.

$$\mathbf{Y_{2F}} = (\mathbf{Q_2 H_2 P_2})^{\mathbf{T}} \mathbf{X_{2F}} = \mathbf{P_2^T H_2^T Q_2^T X_{2F}}$$

where the subscript F denotes a matrix with flipped elements. Therefore,

$$\begin{pmatrix} Y_1 \\ Y_0 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 \\ 0 & -1 & 1 \end{pmatrix} \operatorname{diag} \begin{pmatrix} H_0 \\ H_0 - H_1 \\ H_1 \end{pmatrix} \begin{pmatrix} 1 & 1 \\ 0 & -1 \\ z^{-2} & 1 \end{pmatrix} \begin{pmatrix} X_1 \\ X_0 \end{pmatrix}.$$

23. Apparently, the tap multipliers can be reused, just as in the case of a symmetric FIR-filter. In the case of the 2-parallel fast-FIR filter, one can consider the following 3 subfilters.

$$h_0 = \{a, 0, c\} \quad h_1 = \{b, b, c\} \quad h_1 - h_0 = \{b - a, b, 0\}$$

The goal here is to achieve as many zero taps as possible in the superpositioned subfilter.

24. (a) The iteration bound is $(T_{\text{mult}} + 2T_{\text{add}})/2 = 18$ ns.

(b) The critical path is $2(T_{\text{mult}} + 3T_{\text{add}}) = 88$ ns.

(c) See Figure 7 for the modified architecture. Note that the multipliers were split into two operations.