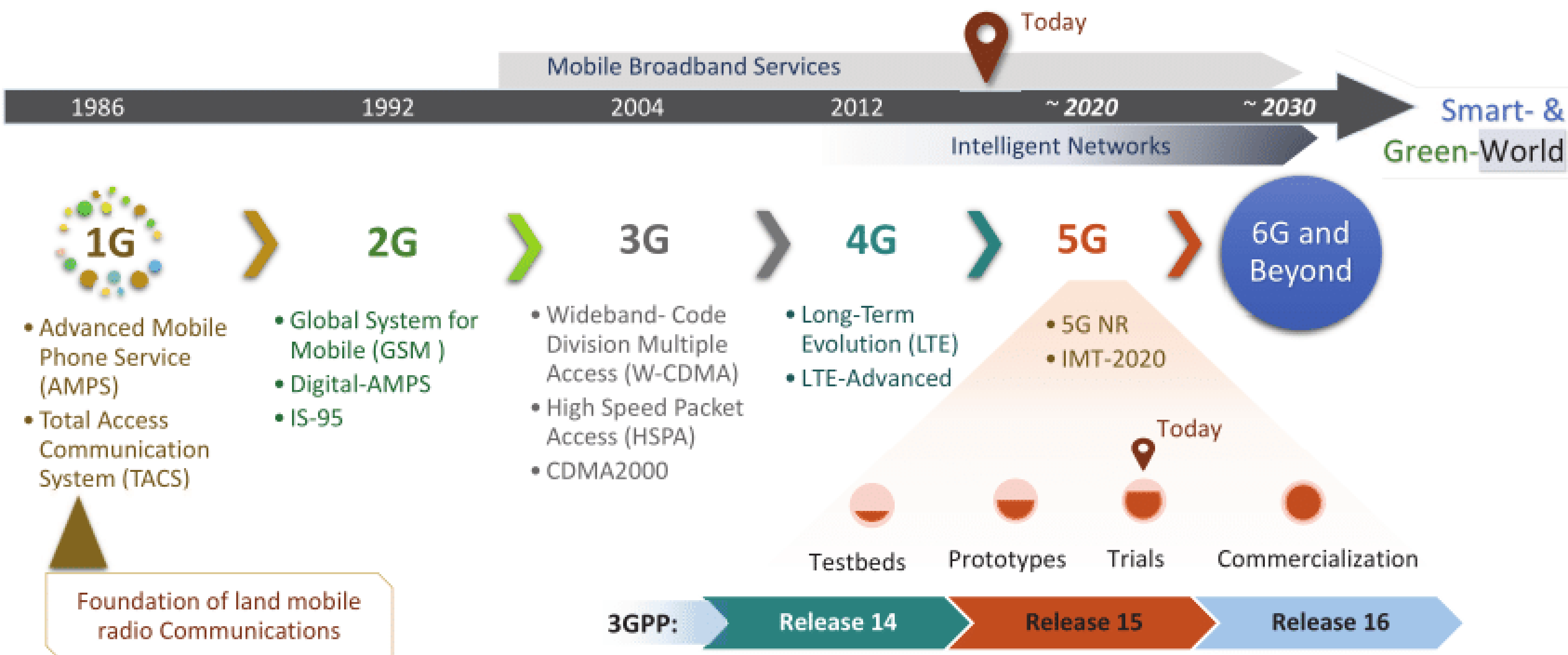
DSP Design in Wireless Communication

LIANG LIU AND FREDRIK EDMAN, LIANG.LIU@EIT.LTH.SE

Wireless connections in a phone

Evolution of mobile communication



CDMA | OFDM | MIMO | Massive MIMO

Wideband | HighMod

Figure from ResearchGate

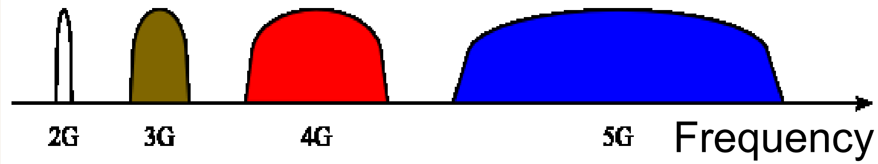
Same in other communication systems

Wider road

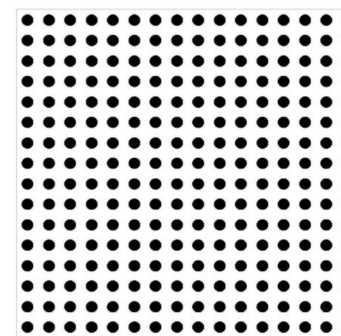
More passengers

Multiple dimensions

Wider bands

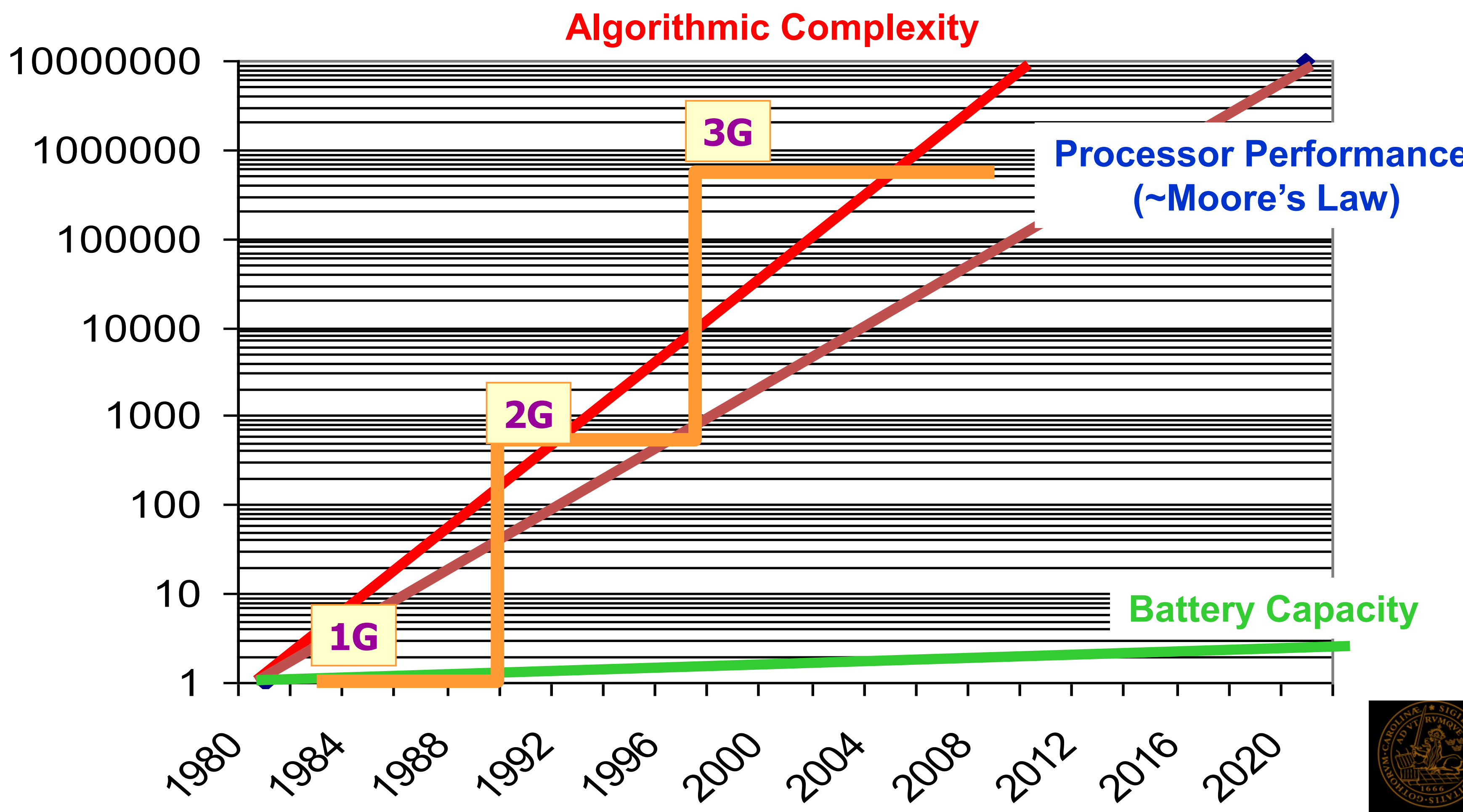


More bits



Multiple antennas

Algorithms beats Moore beats Chemists



Courtesy: Ravi Subramanian (Morphics)

Design Considerations

DESIGN TRADE-OFFS!

Small area

Low power

Low price

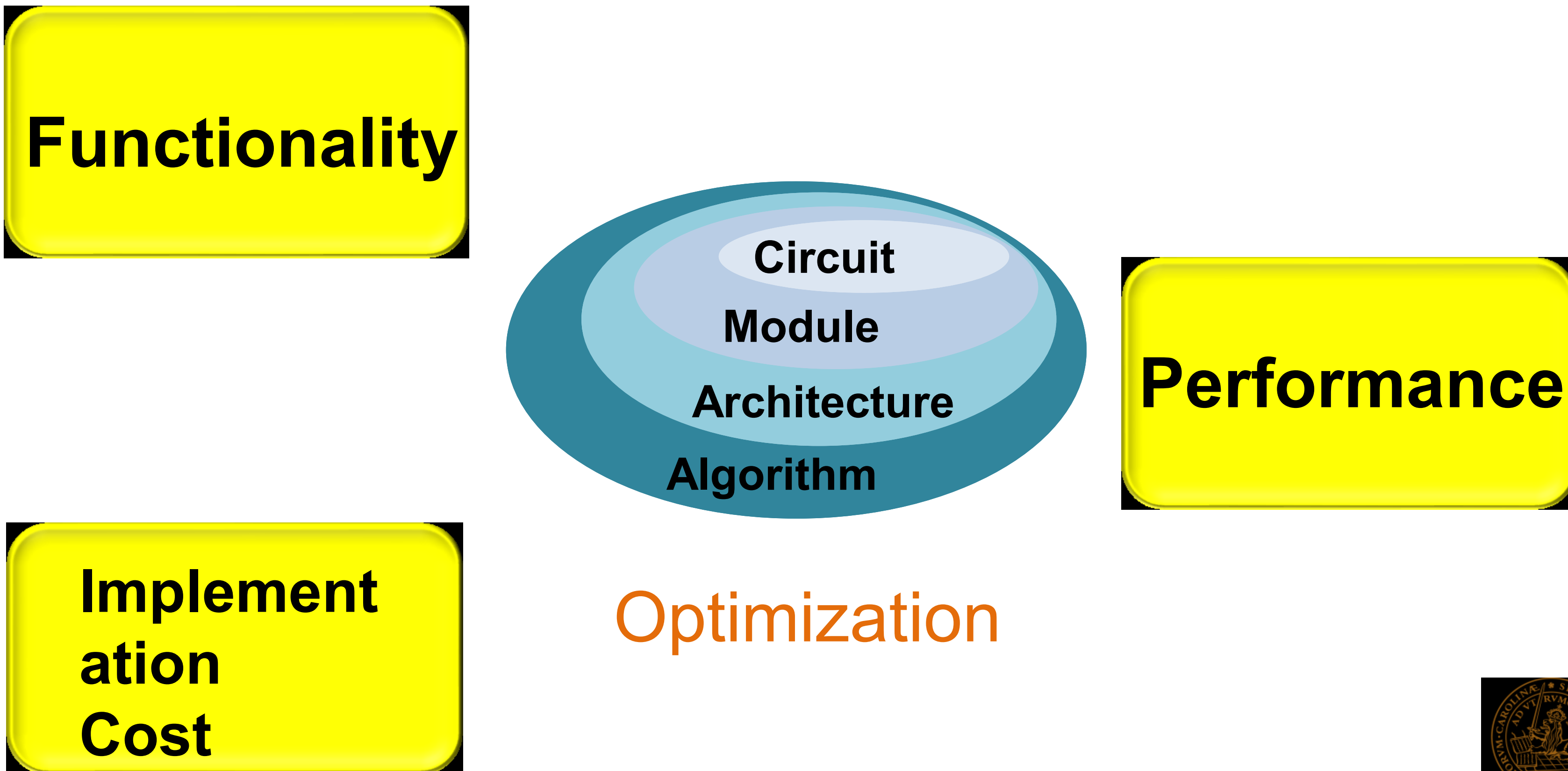
Reliable

High speed

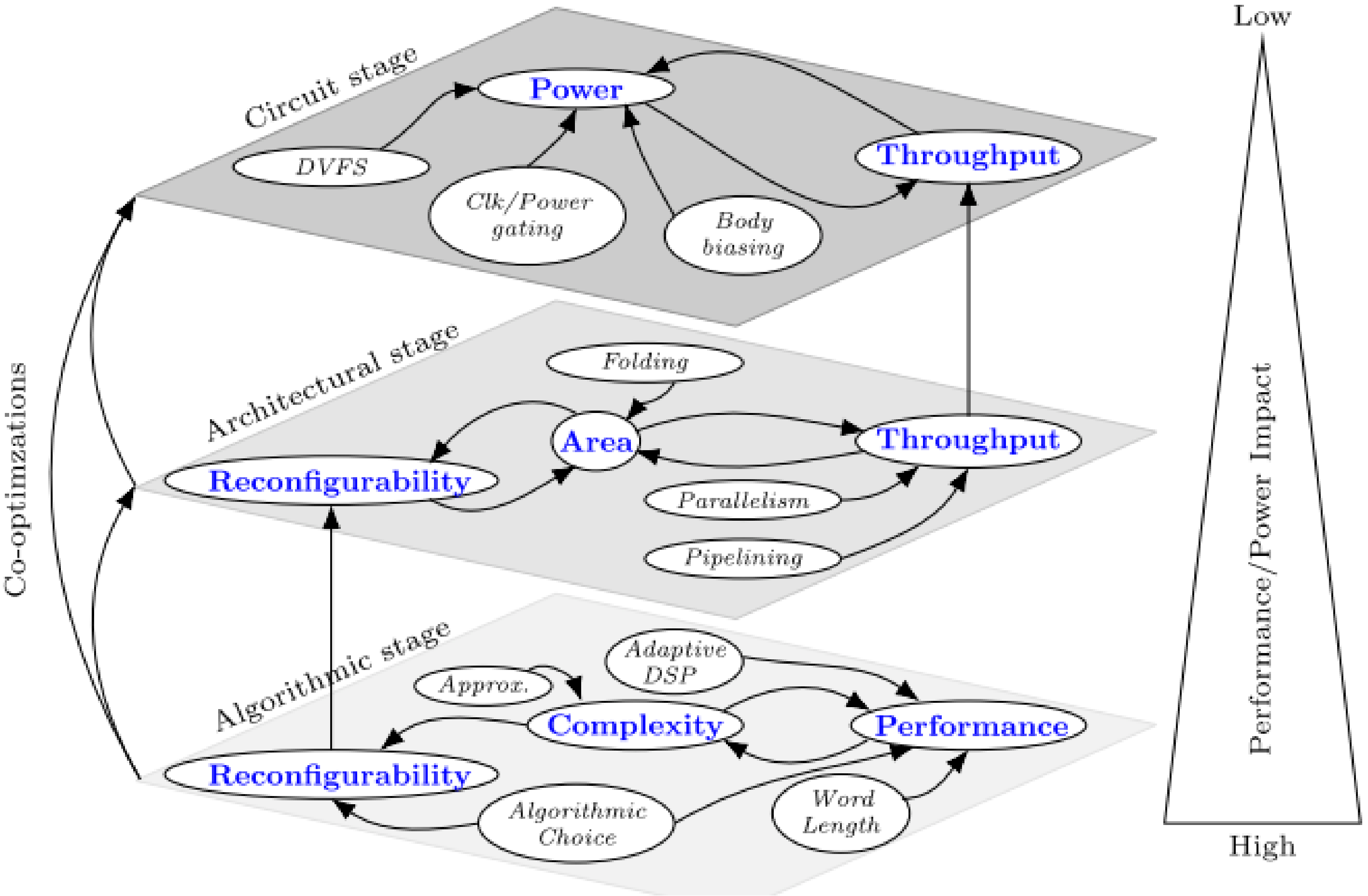
Flexible

Time to market

Optimizing DSP Implementation

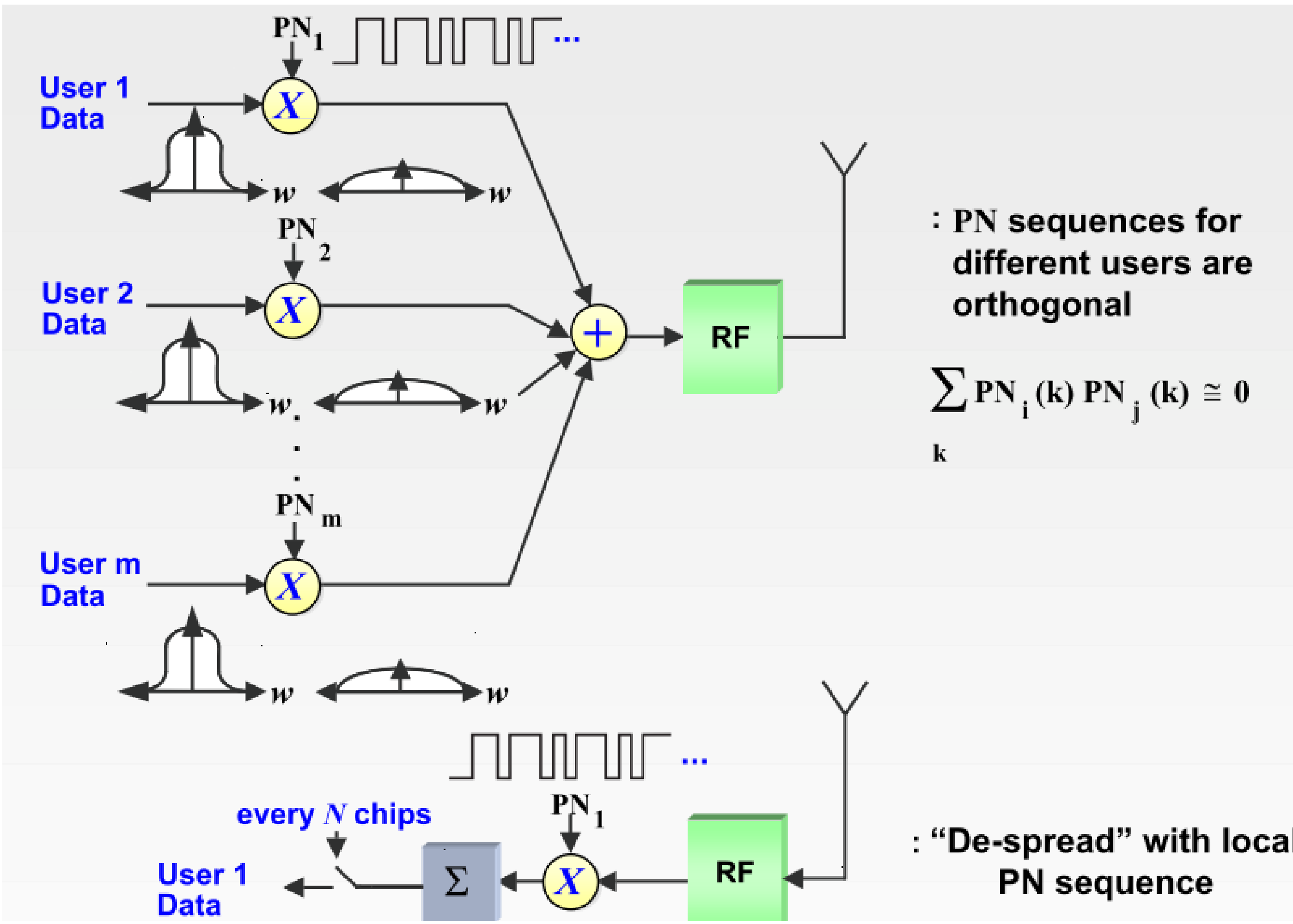


Optimizing DSP Implementation



CDMA

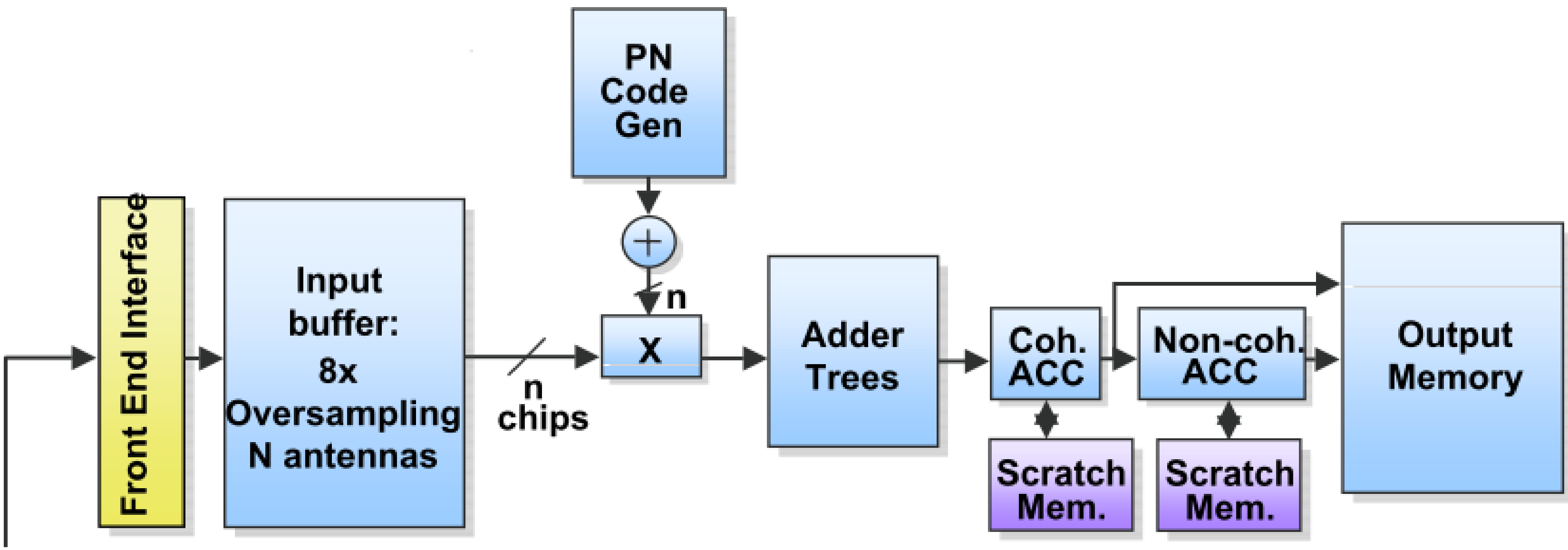
CDMA: Code Division Multiple Access



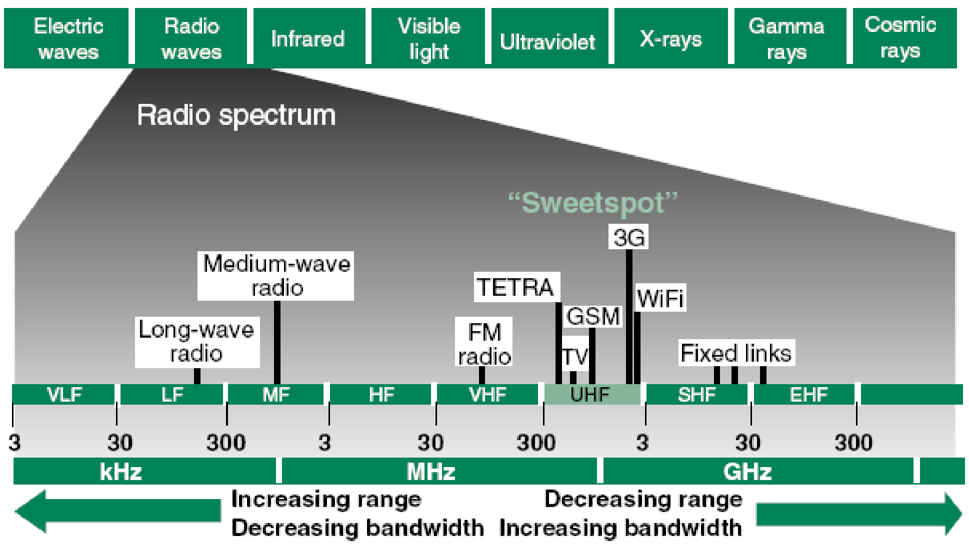
"A UMTS Baseband Receiver Chip for Infrastructure Applications", Texas Instruments, S. Sriram *et al.*

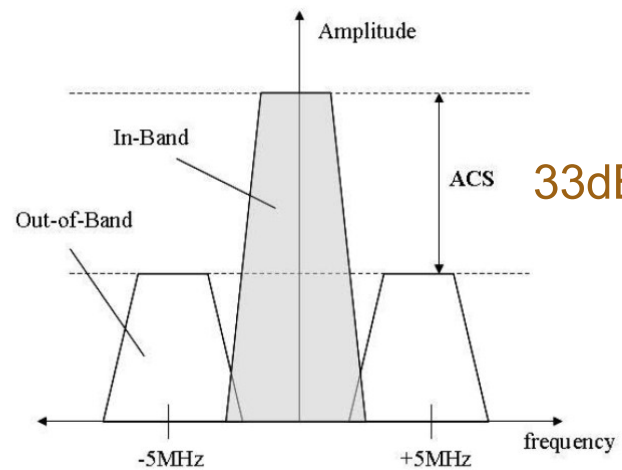
LUND UNIVERSITY

Accumulator

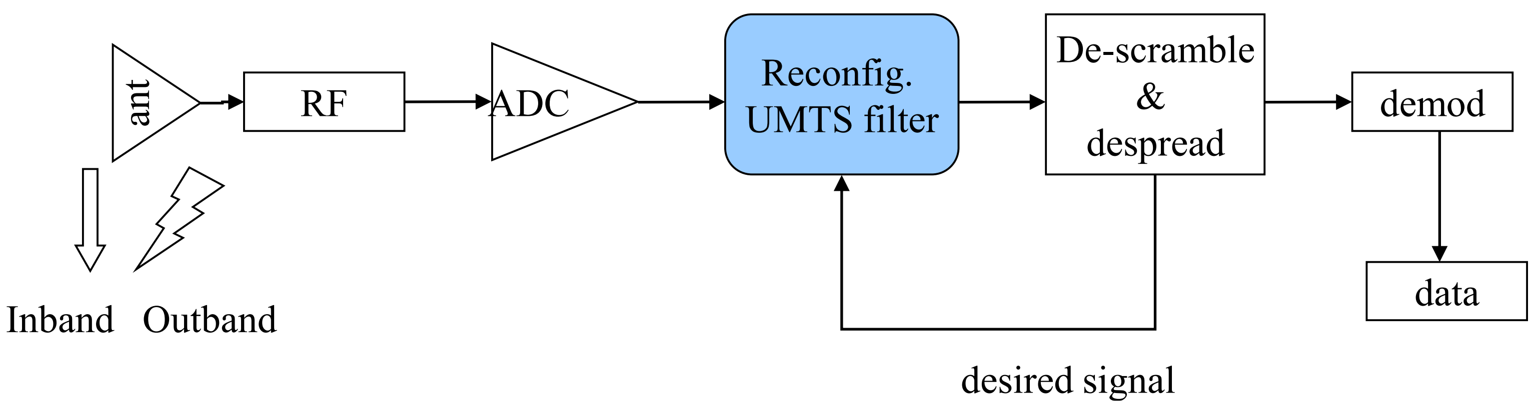


UMTS filter in receiver system





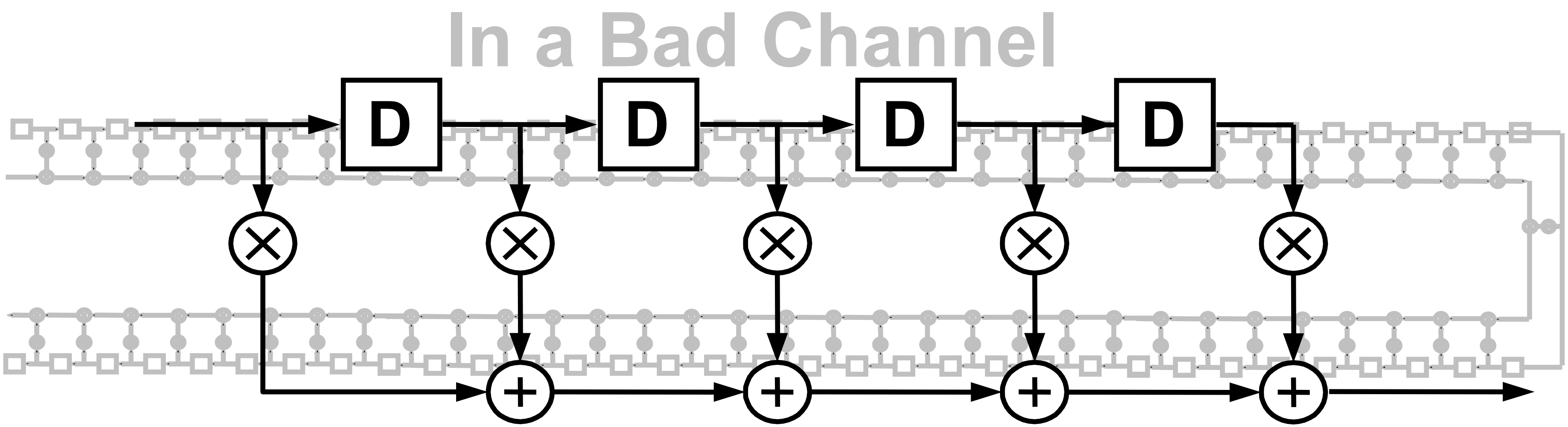
33dB



"Architectural Optimization for Low Power in a Reconfigurable UMTS Filter", in *Proceedings of Wireless Personal Multimedia Communications Symposium (WPMC)*, Deepak Dasalukunte *et al.* San Diego, USA

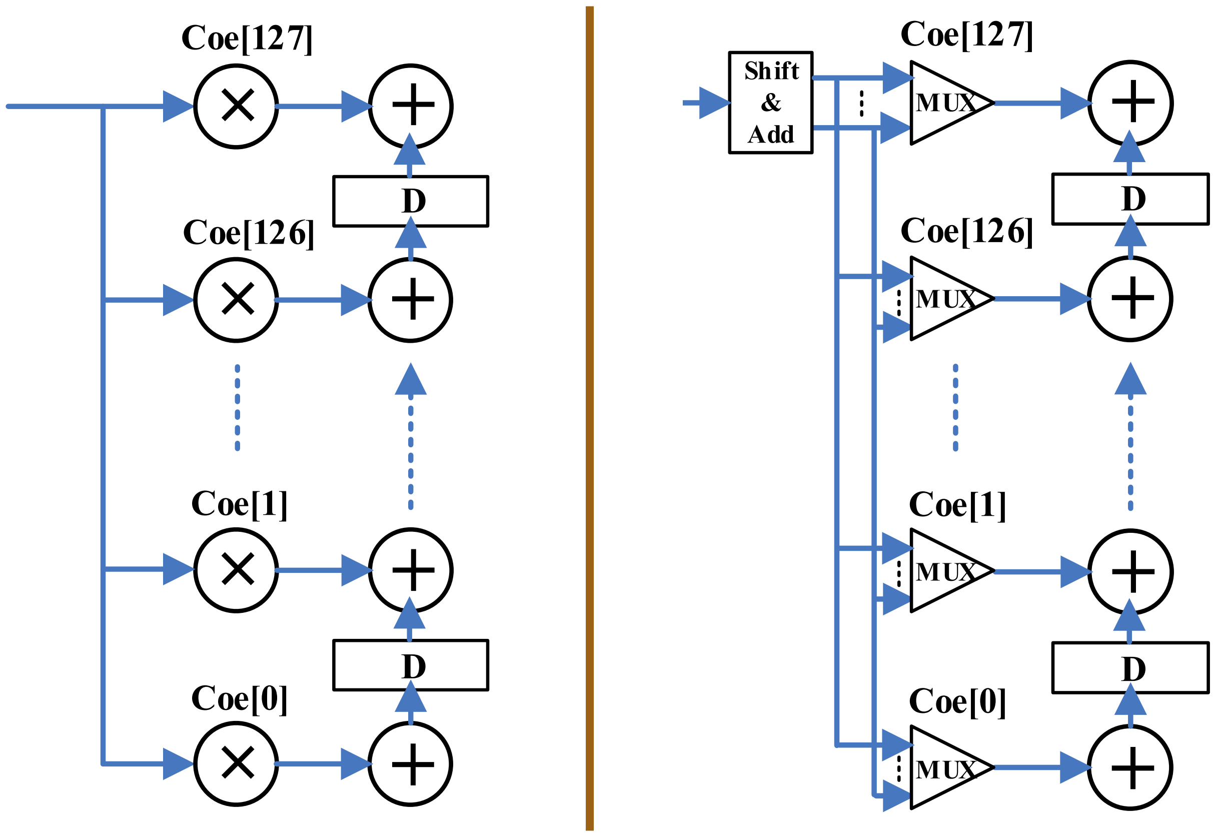
Adaptive UMTS Filter (Algorithm level)

- minimum 33dB stop band attenuation (3GPP specification)
- required filter length of 65 taps

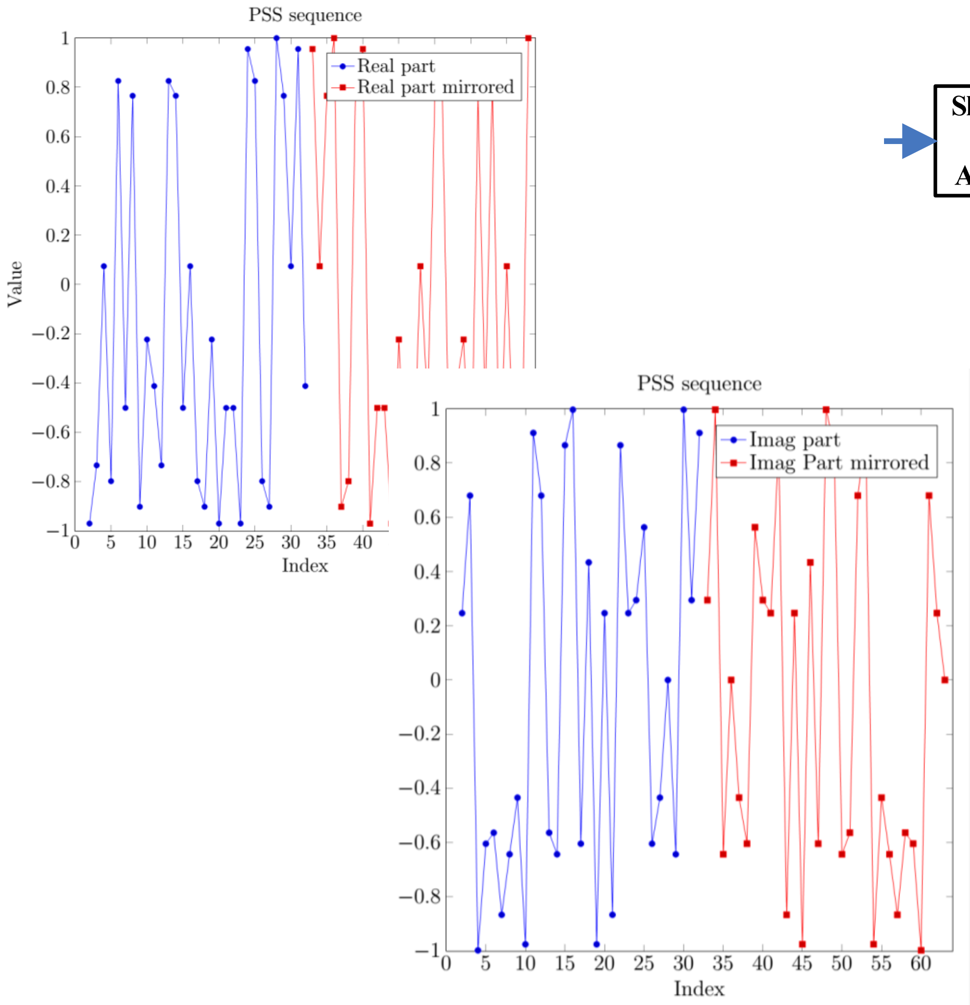


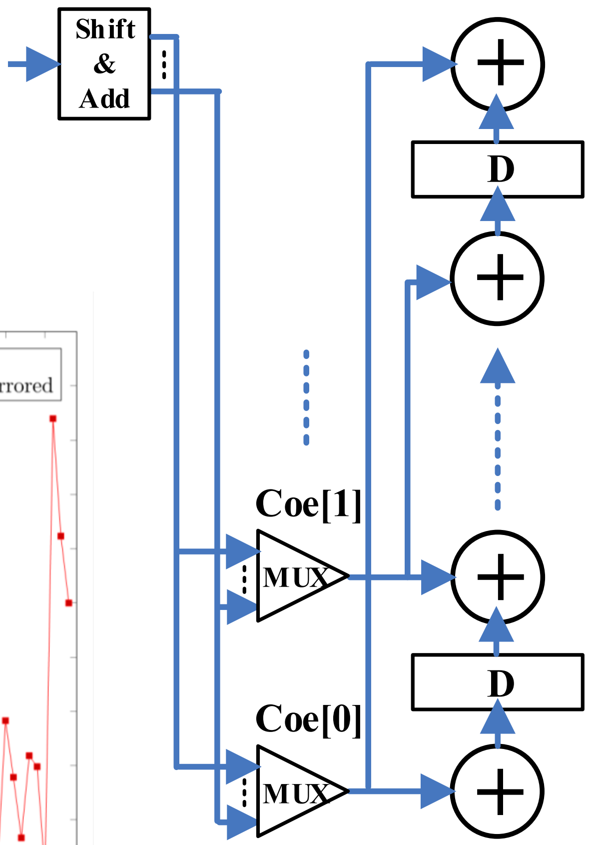
...but ONLY 5 is needed in a Good one!

Constant Multiplier (Module level)



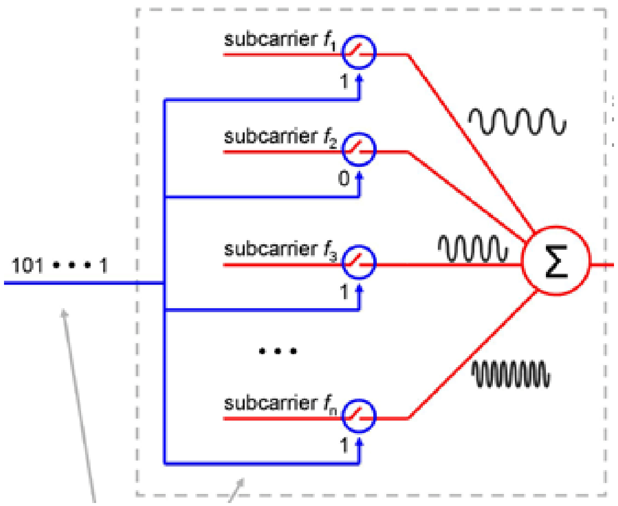
Symmetric Coefficient (Architecture level)

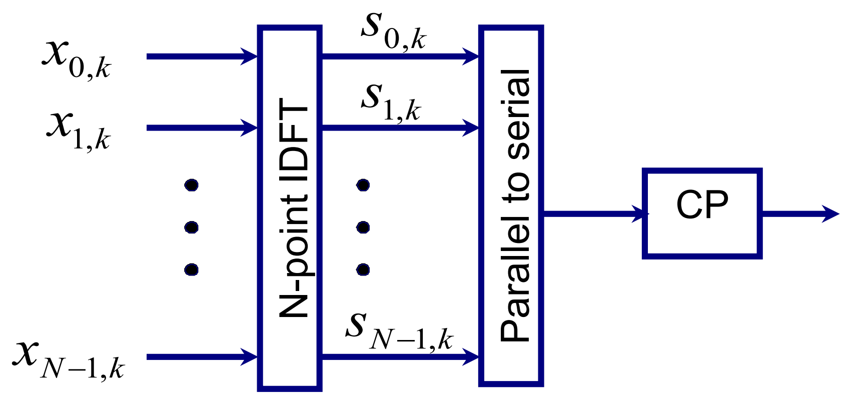




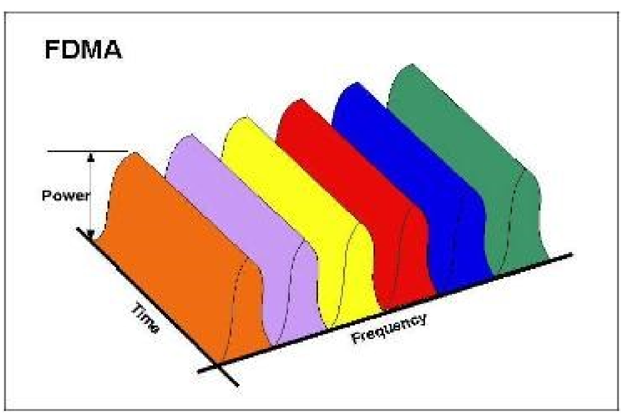
OFDM

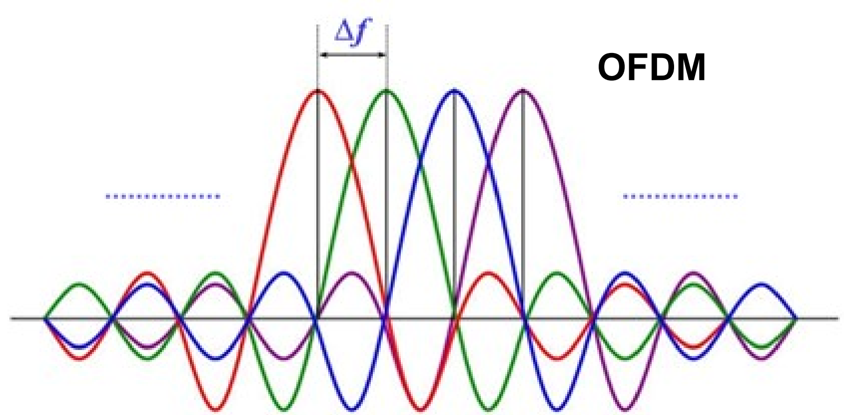
OFDM: Orthogonal Frequency Division Multiplexing



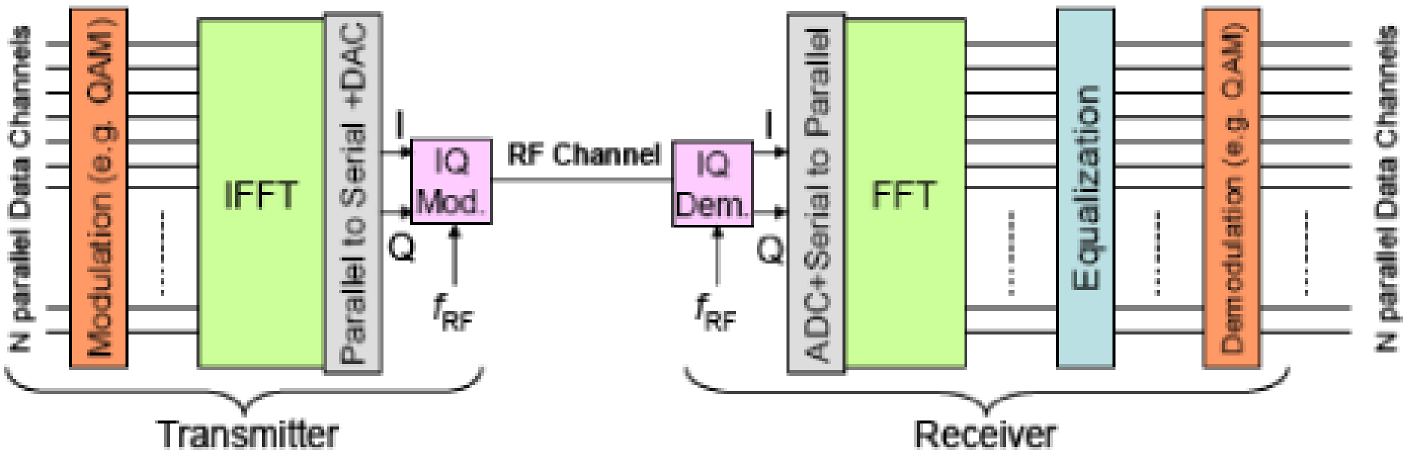


$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k)\cdot e^{j\left(\frac{2\pi}{N}\right)nk}$$





FFT/IFFT in OFDM Systems

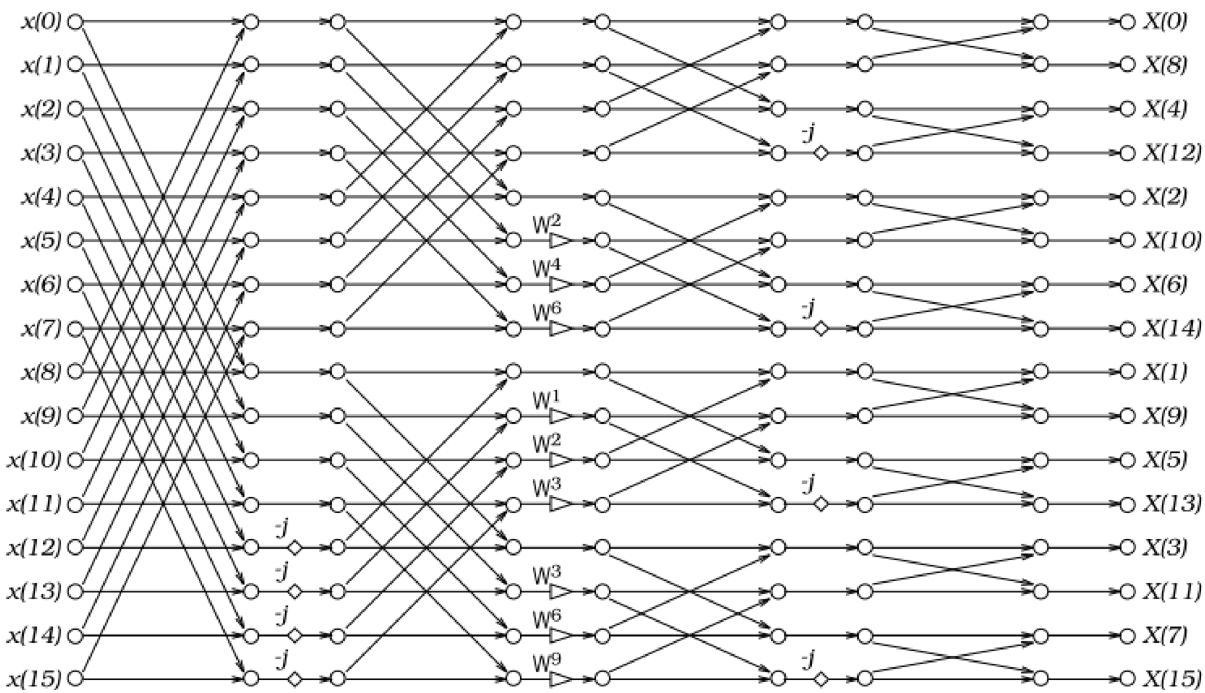


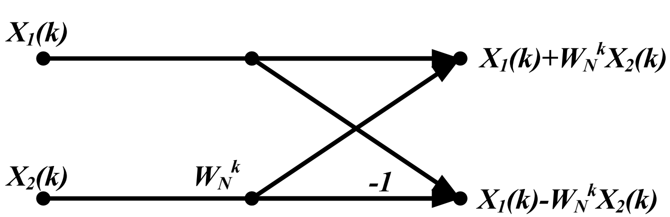
Large number of subcarriers ⇨ large FFT, ***O***(N$\log_2$N)

OFDM:

- DVB-2/4/8k FFT
- WLAN IEEE802.11a/g-64 FFT (48+4 subcarriers)
- LTE – Long Term Evolution: 2k FFT
- 5G: 4K FFT over 200MHz bandwidth
- 6G?

FFT: VLSI Architecture





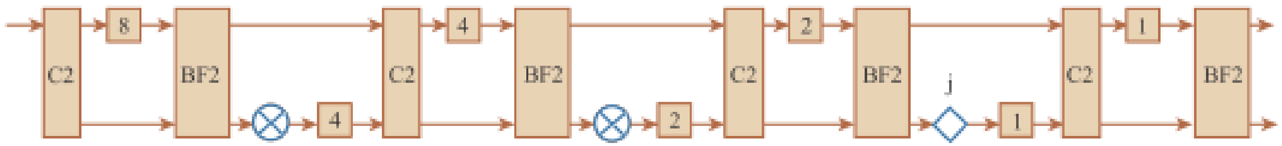
\+

→

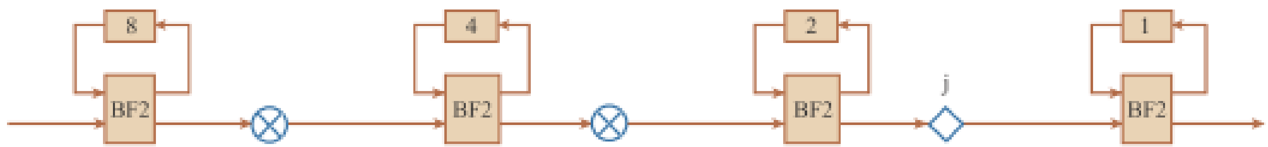
- Folding
- Pipeline
- Parallel

LUND UNIVERSITY

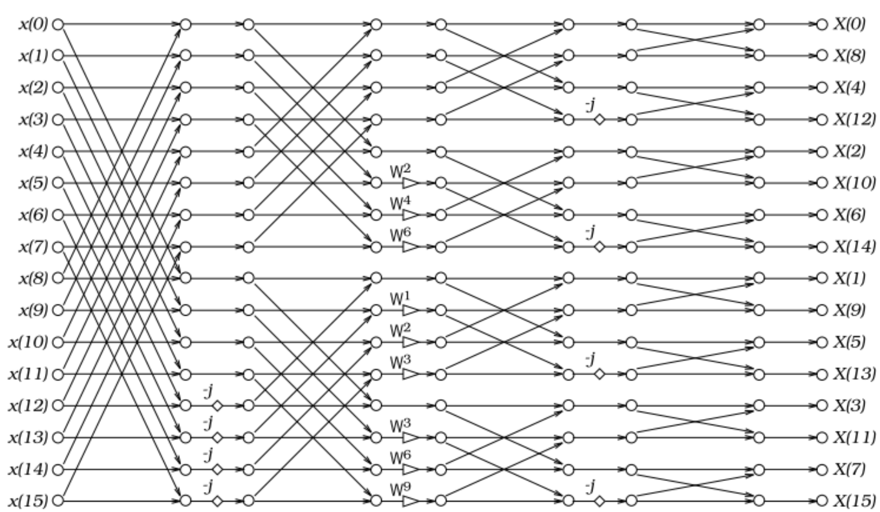
FFT: VLSI Architecture



(1) . R2MDC(N-16)

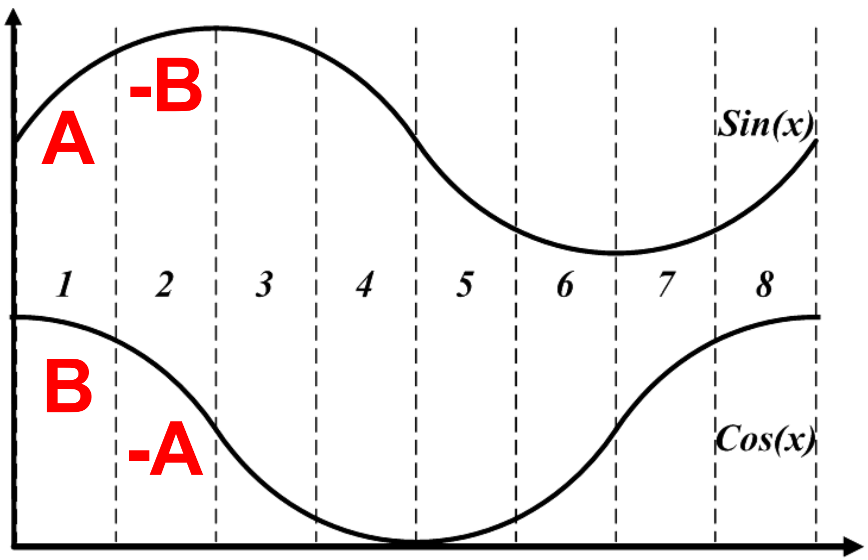


(2) . R2SDF(N-16)



FFT: Twiddle Factors (module level)

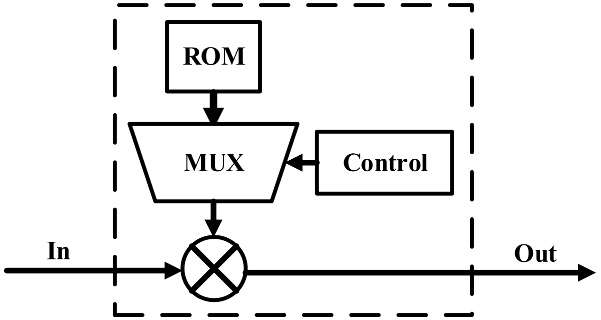
- Symmetry of twiddle factors
  - $e^{jx} = cosx + jsinx$
  - Reduce number of twiddle factors by 87.5%



region	Twiddle factor
0	A+Bj
1	-B-Aj
2	B-Aj
3	-A+Bj
4	-A-Bj
5	B+Aj
6	-B+Aj
7	A-Bj

FFT: Twiddle Factors

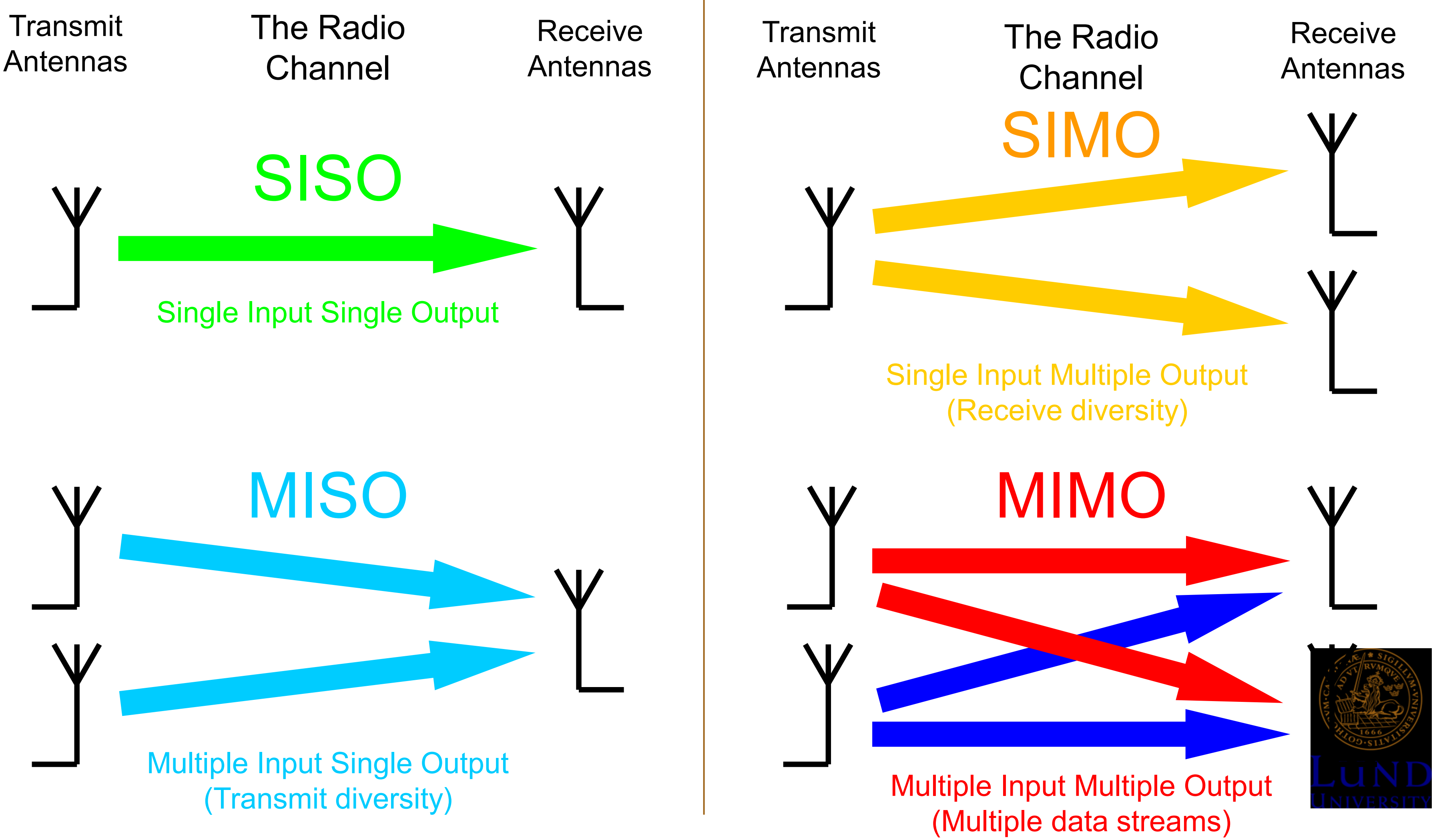
- Shift-add for constant multiplier



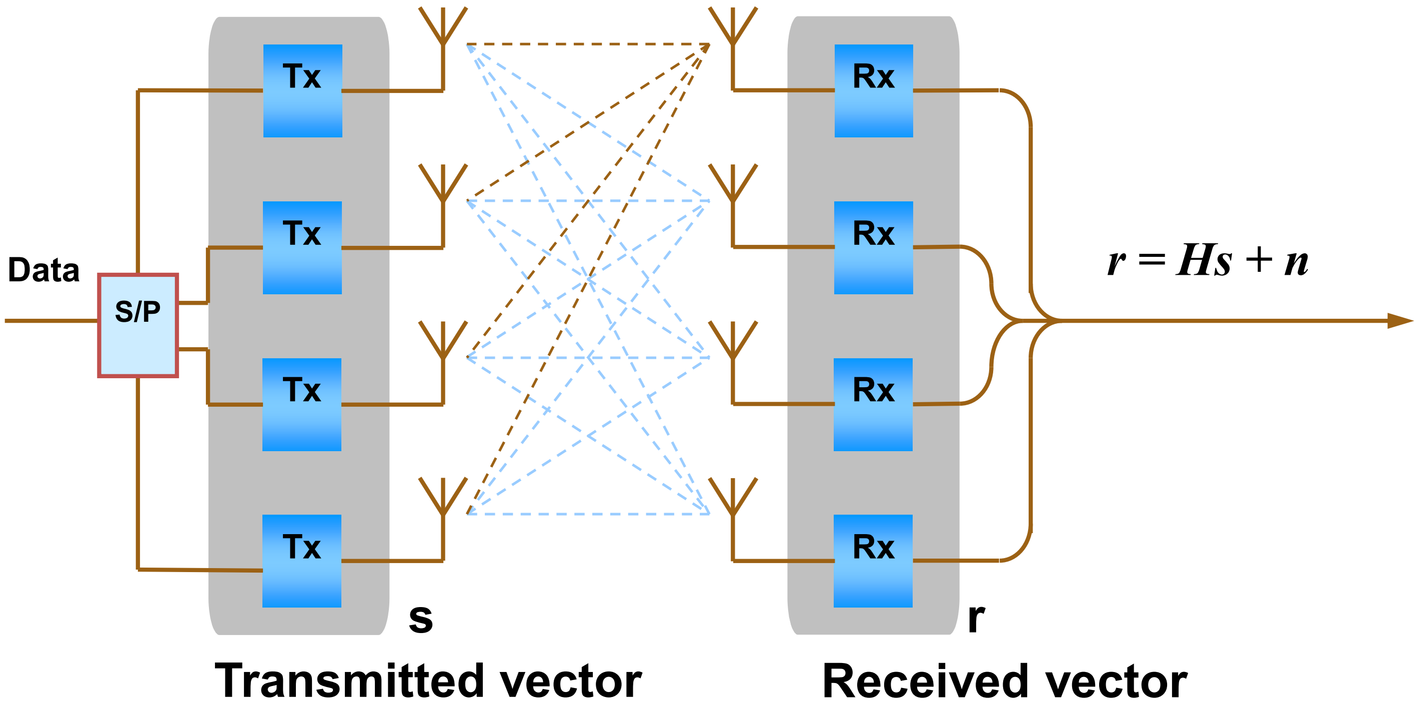
0.99518	$1-2^{-8}-2^{-10}+2^{-11}$	0.097961	$2^{-4}+2^{-5}+2^{-8}+2^{-11}$
0.980773	$1-2^{-6}-2^{-8}+2^{-12}$	0.195068	$2^{-3}+2^{-4}+2^{-7}-2^{-11}$
0.95691	$1-2^{-4}+2^{-6}+2^{-8}$	0.290283	$2^{-2}+2^{-5}+2^{-7}+2^{-10}$
0.923828	$1-2^{-4}-2^{-7}-2^{-8}-2^{-9}$	0.382629	$2^{-2}+2^{-3}+2^{-7}-2^{-11}$
0.881896	$1-2^{-3}+2^{-7}-2^{-10}$	0.471374	$2^{-1}-2^{-5}+2^{-9}+2^{-11}$
0.83142	$1-2^{-3}-2^{-5}-2^{-6}+2^{-8}-2^{-11}$	0.555541	$2^{-1}+2^{-4}-2^{-7}+2^{-11}$
0.77301	$1-2^{-2}+2^{-6}+2^{-7}-2^{-11}$	0.634338	$2^{-1}+2^{-3}+2^{-7}+2^{-10}+2^{-14}$
0.707	$2^{-1}+2^{-3}+2^{-4}+2^{-6}+2^{-8}+2^{-14}$	0.707	$2^{-1}+2^{-3}+2^{-4}+2^{-6}+2^{-8}+2^{-14}$

MIMO

Multiple Antenna System, MIMO



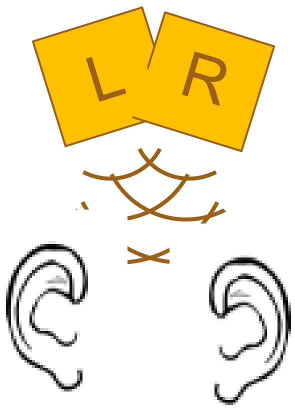
MIMO System Model



$$\boldsymbol{H} = M \overset{\longleftarrow \; N \; \longrightarrow}{\begin{bmatrix} h_{11} & h_{12} & \ldots\ldots.. & h_{1N} \\ h_{21} & h_{22} & \ldots\ldots.. & h_{2N} \\ . & . & \ldots\ldots.. & . \\ h_{M1} & h_{M2} & \ldots\ldots.. & h_{MN} \end{bmatrix}}$$

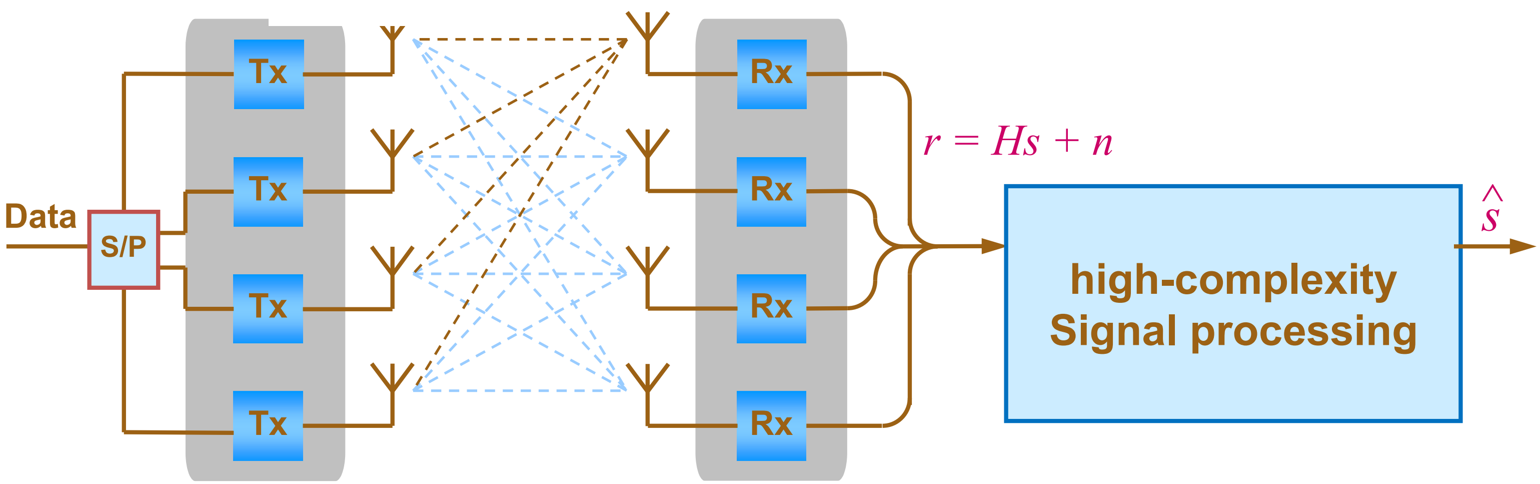
h_{ij} models fading gain between the j^{th} transmit and i^{th} receive antenna

MIMO Signal Processing - Receiver



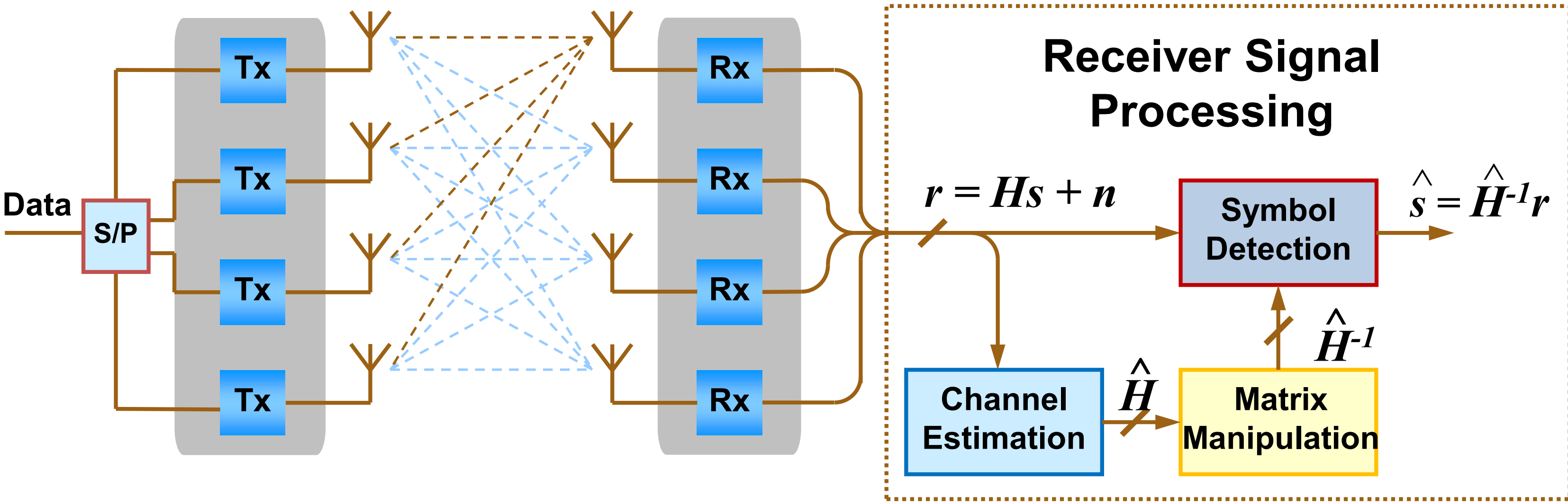
Interference

Cancellation!



- Recover the transmitted signal *s* from the received signal *r*, which contains interference and noise.

MIMO Signal Processing - Receiver



- *Channel estimation*: obtain the channel status by training signals
- *Matrix manipulation*: matrix inversion or decomposition depending on detection algorithm
- *Symbol detection*: estimate transmitted signal *s* given channel matrix *H* and received signal *r*

MIMO Signal Detection

$$\boldsymbol{r} = \boldsymbol{H}\boldsymbol{s} + \boldsymbol{n}$$

- *Linear Detection*: zero-forcing detection

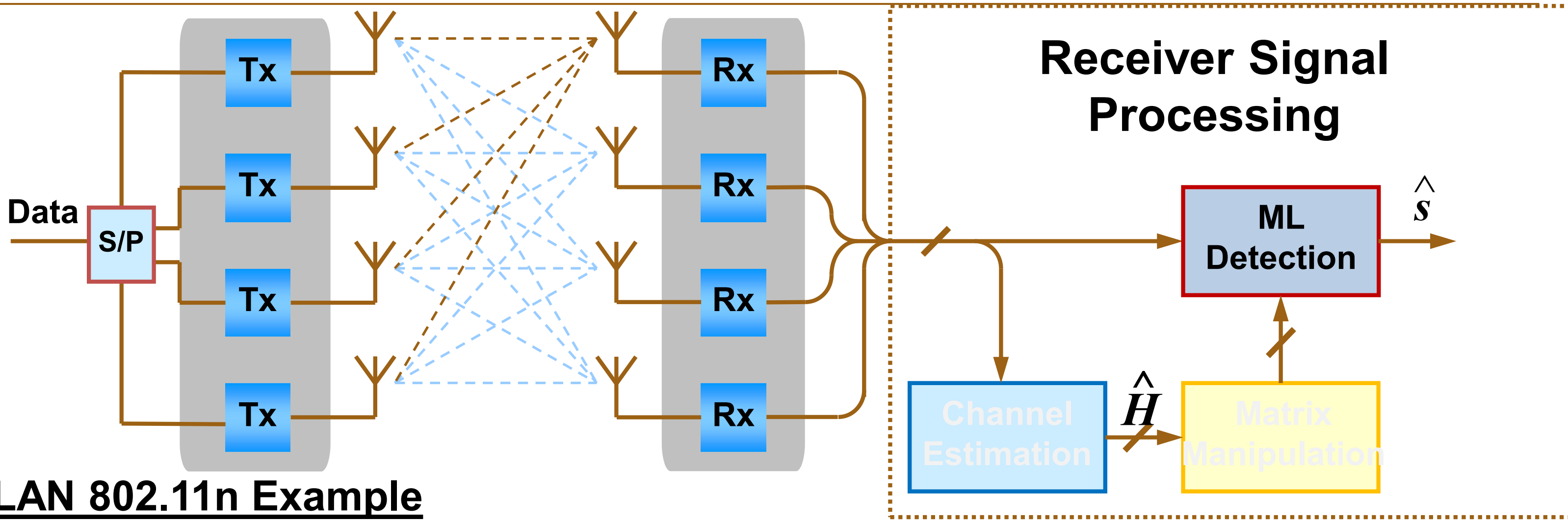
$$\hat{\boldsymbol{s}}_{\boldsymbol{zf}} = \boldsymbol{H}^{-1}\boldsymbol{r} = \boldsymbol{s} + \boldsymbol{H}^{-1}\boldsymbol{n}$$

- *Maximum Likelihood (ML) Detection*: exhaustive search

$$\hat{\boldsymbol{s}}_{\boldsymbol{ml}} = \boldsymbol{arg} \max_{\boldsymbol{s} \in |\boldsymbol{Q}|^{\boldsymbol{N}}} \boldsymbol{p}(\boldsymbol{s}|\boldsymbol{r}, \boldsymbol{H})$$
$$= \boldsymbol{arg} \min_{\boldsymbol{s} \in |\boldsymbol{Q}|^{\boldsymbol{N}}} |\boldsymbol{r} - \boldsymbol{H}\boldsymbol{s}|^2$$

- **1.6×10^7** points per vector detection for 64-QAM, 4×4 MIMO

High Complexity ML Detection



<u>WLAN 802.11n Example</u>

Modulation 256QAM; 4 Tx antennas; 108 sub-channels, 4µs per OFDM symbol

ML detection ➡ 1.159 x 10^{17} points/sec

Current DSP technology is 1G inst/sec ➡ 10^{8} processors!

OR ("Moores Law" ..... processor capability doubles every 18 months)

➡ MUST WAIT 40years!

Mike Faulkner 2005, Victoria Univ.

Today…

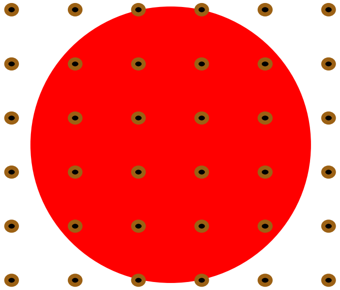
Intel i7 CPU: 10^{11} inst/sec

Sphere Decoding: Algorithm level optimization

Simplified 2D-case

ML Detection

Sphere Detection

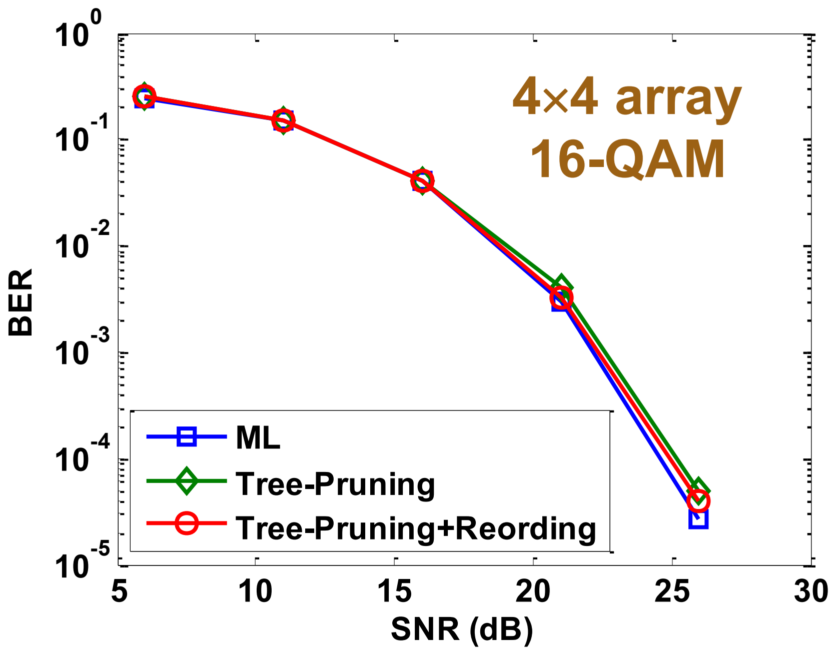


Limited search space ⇨ reduced complexity

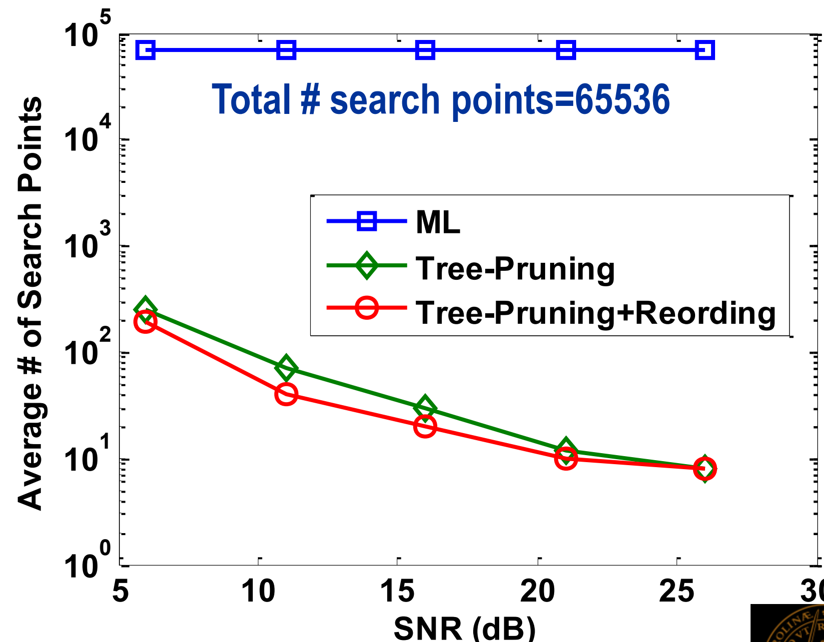
Sphere Decoding: complexity reduced

- ***Near optimal ML performance with significantly reduced computational complexity (# search points)***

Detection Performance



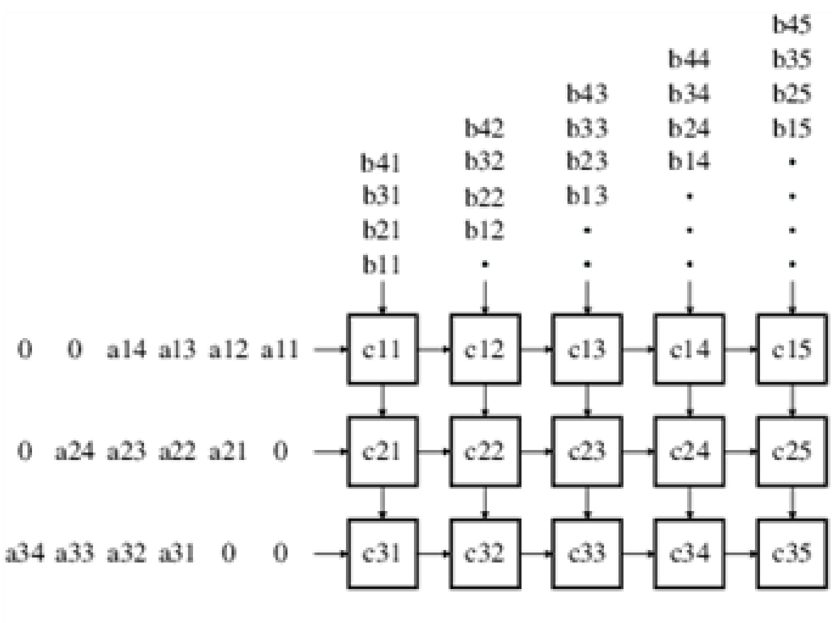
Computational Complexity

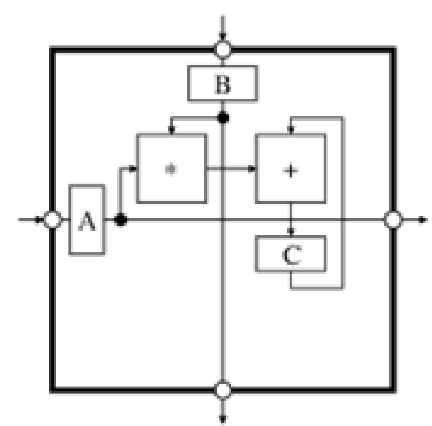


Near ML detection with 0.1% computational complexity

Systolic Array

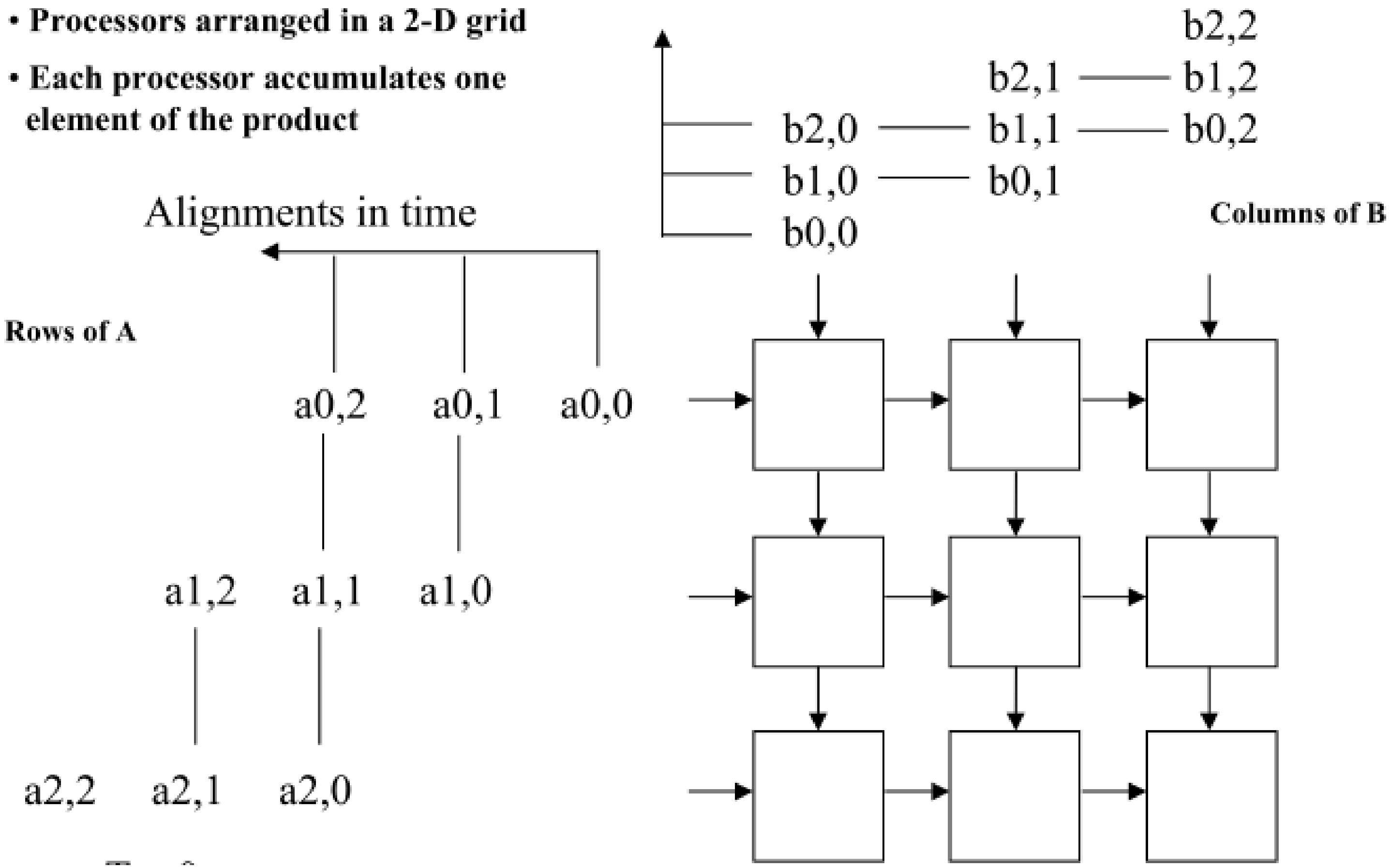
- **Systolic array**
  - A **homogeneous** network of tightly coupled Processing Elements (PEs) called cells or nodes
  - The wave-like propagation of data through a systolic array resembles the pulse of the human circulatory system, the name systolic was coined from medical terminology





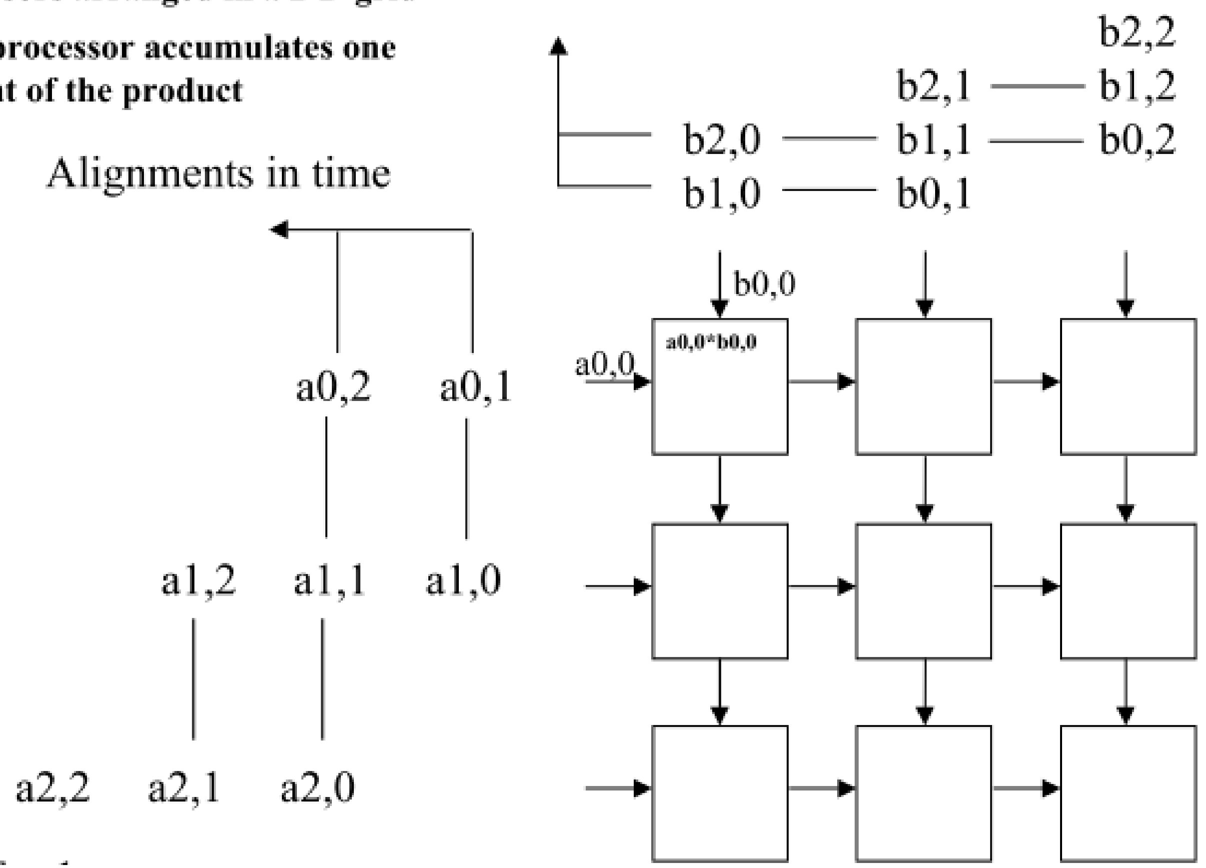
Systolic Array (example)

- Processors arranged in a 2-D grid
- Each processor accumulates one element of the product



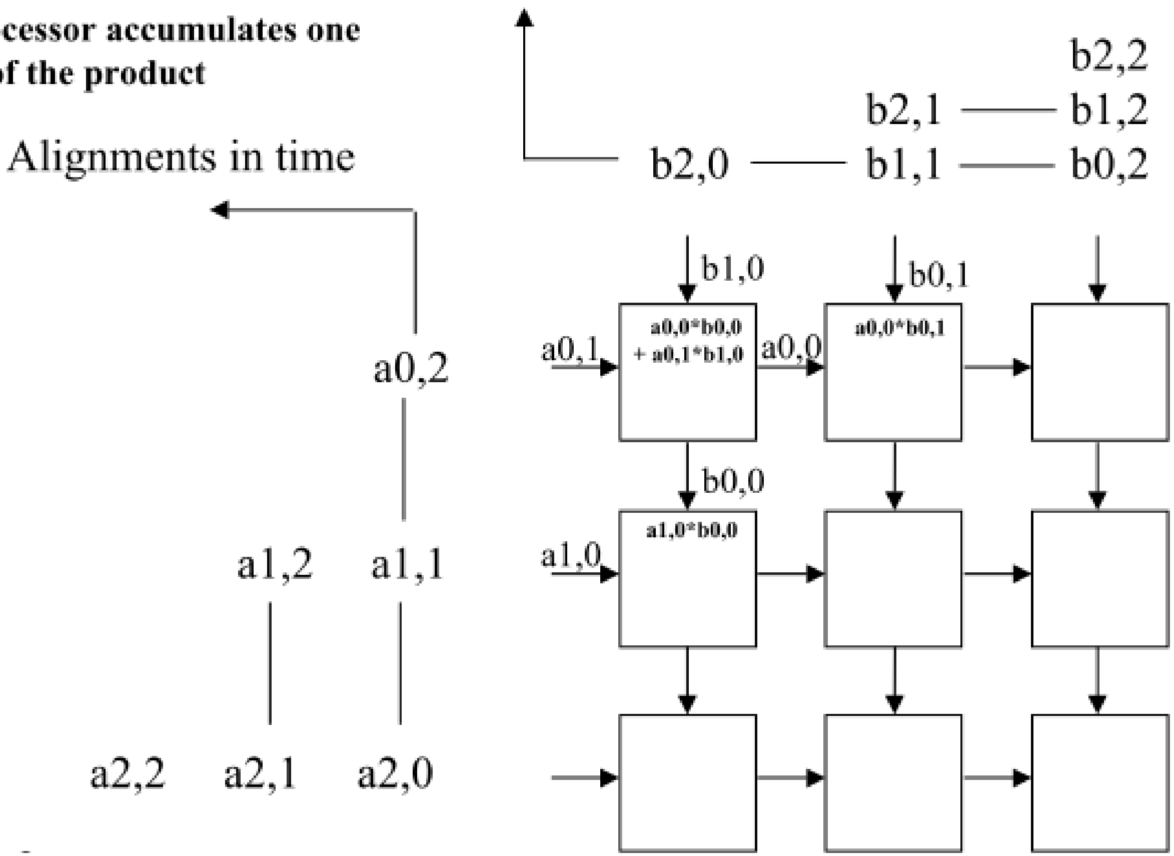
Systolic Array (T1)

- **Processors arranged in a 2-D grid**
- **Each processor accumulates one element of the product**



Systolic Array (T2)

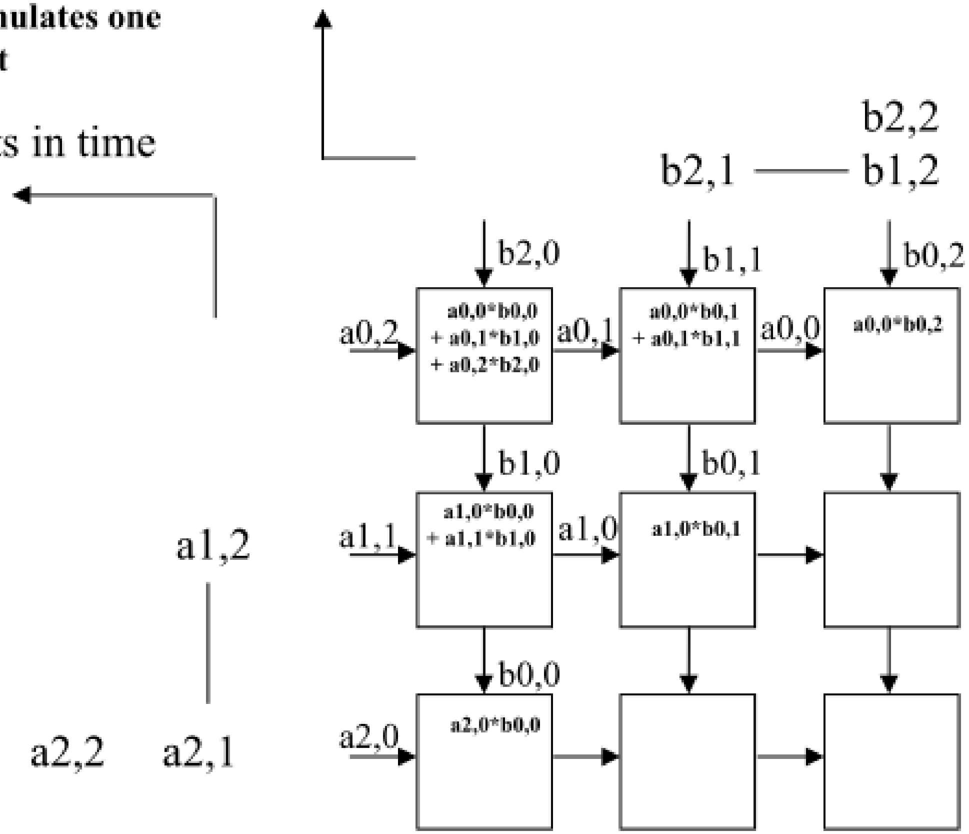
- **Processors arranged in a 2-D grid**
- **Each processor accumulates one element of the product**



Systolic Array (T3)

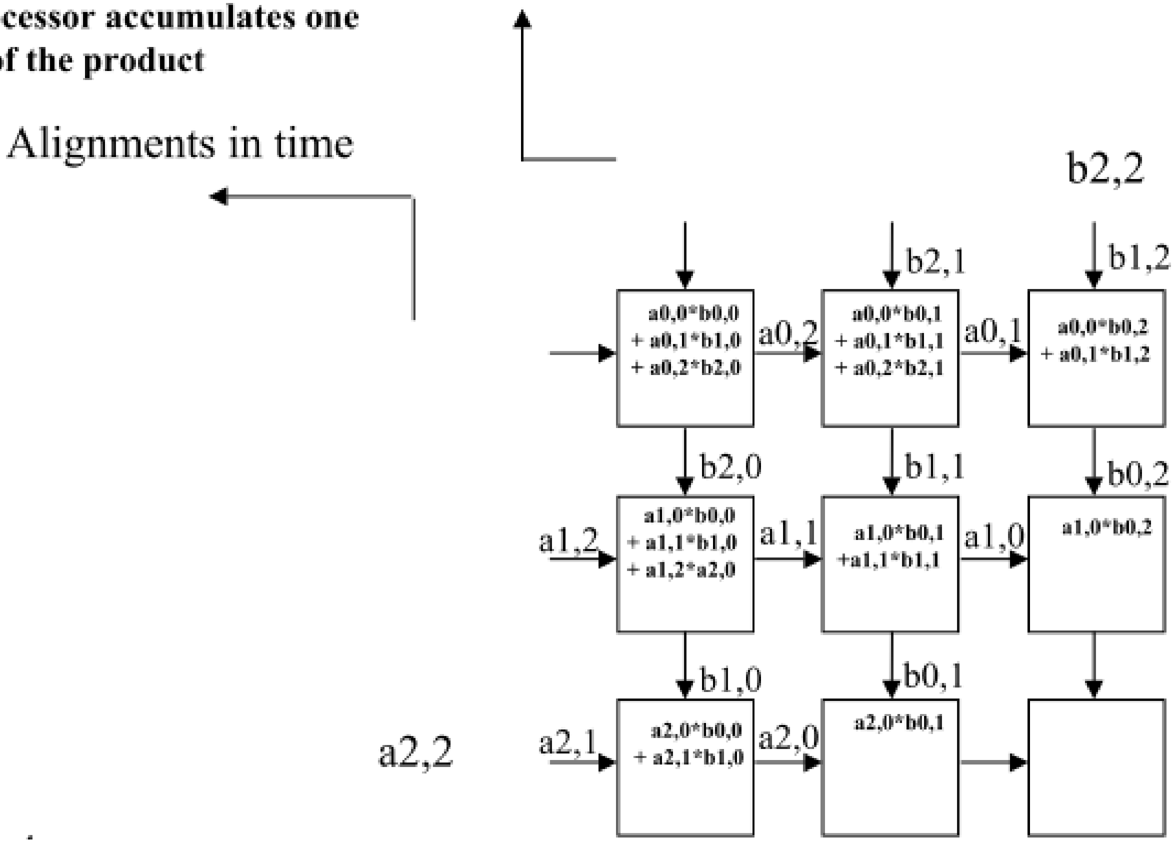
- Processors arranged in a 2-D grid
- Each processor accumulates one element of the product

Alignments in time



Systolic Array (T4)

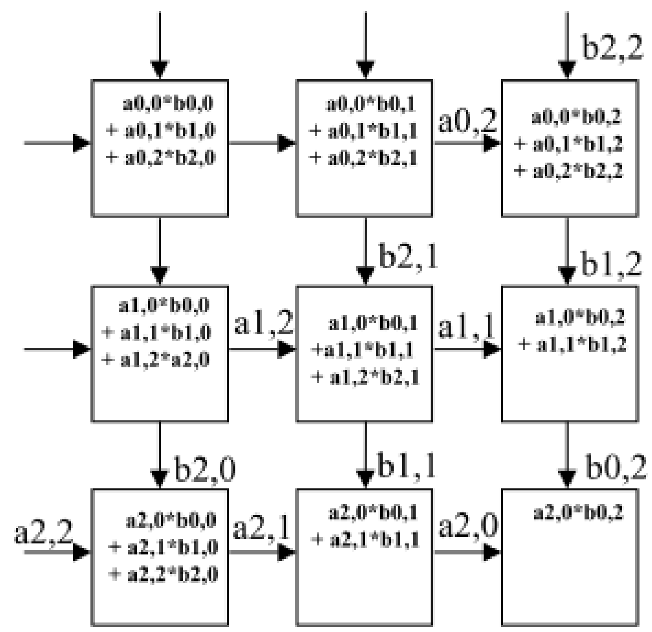
- **Processors arranged in a 2-D grid**
- **Each processor accumulates one element of the product**



Systolic Array (T5)

- **Processors arranged in a 2-D grid**
- **Each processor accumulates one element of the product**

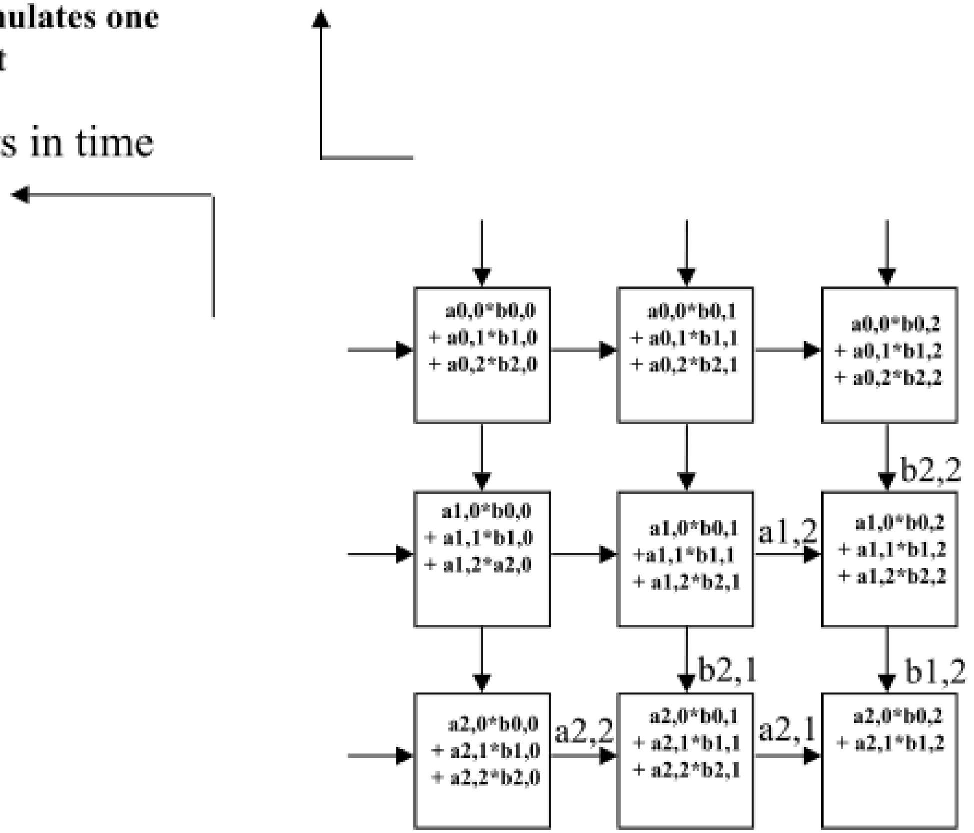
Alignments in time



Systolic Array (T6)

- Processors arranged in a 2-D grid
- Each processor accumulates one element of the product

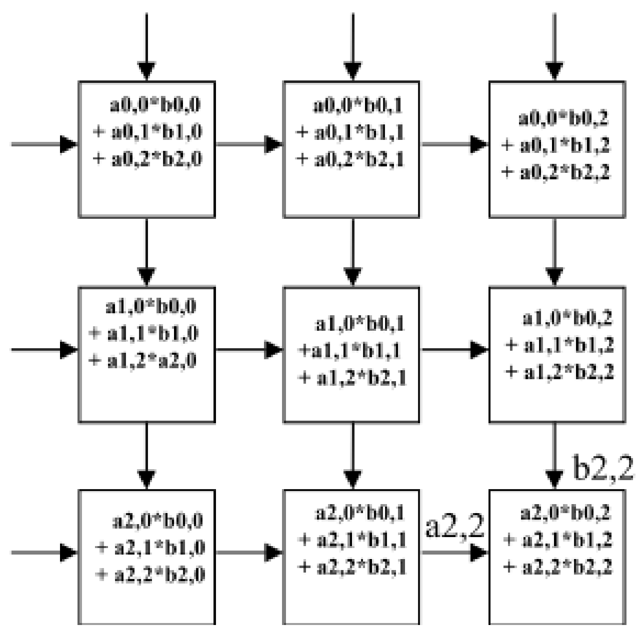
Alignments in time



Systolic Array (T7)

- **Processors arranged in a 2-D grid**
- **Each processor accumulates one element of the product**

Alignments in time



Done

Massive MIMO

Goes to 'LARGE' Dimension

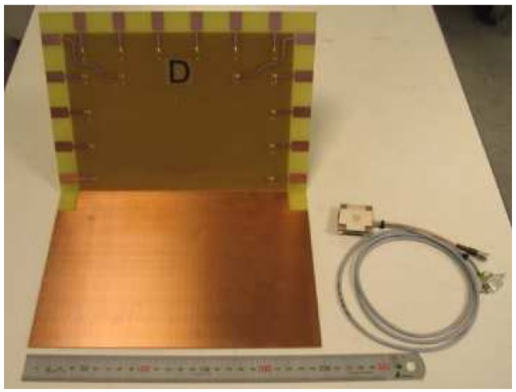
- Further Scaling Up?
  - Size limitation in terminals
  - Power consumption in portable devices

Cellular	Antenna	WLAN	Antenna
HSPA+	2×2	802.11n	4×4
LTE	4×4	802.11ac	8×4
LTE-A	8×8	802.11?	16×16

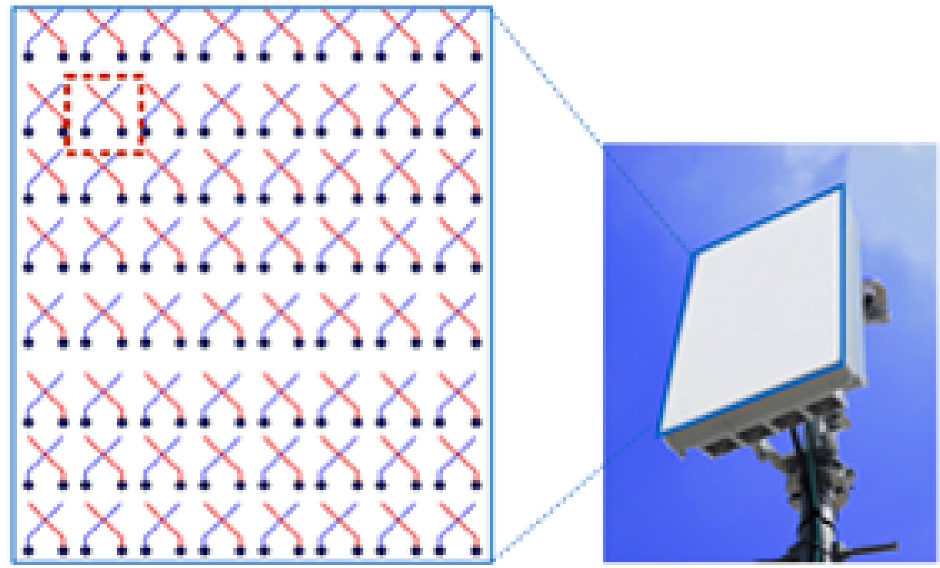
LUND UNIVERSITY

How many antennas can we have?

2 in a phone

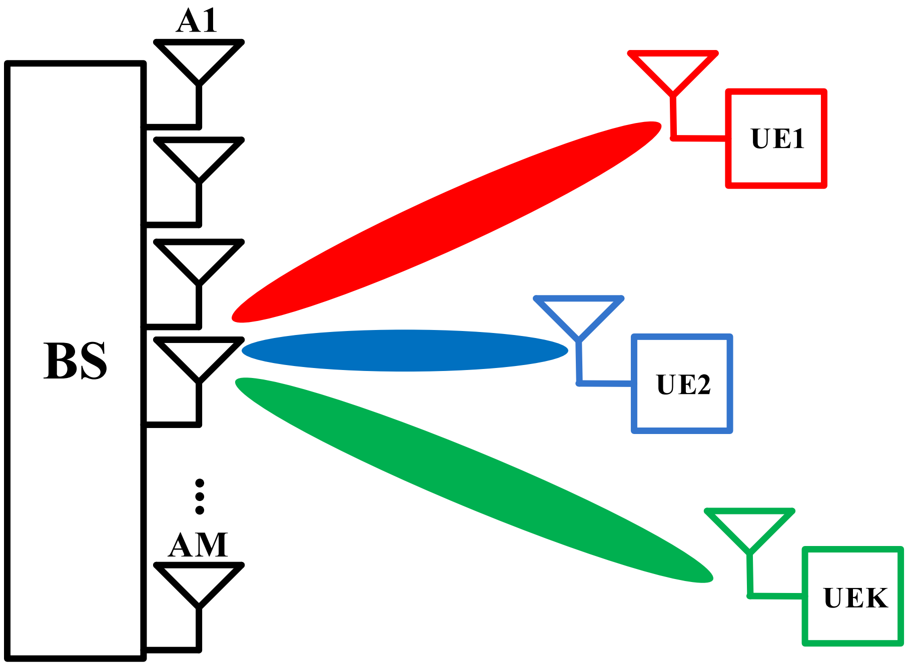


16 in a laptop



100X

Massive MIMO or Very-Large MIMO

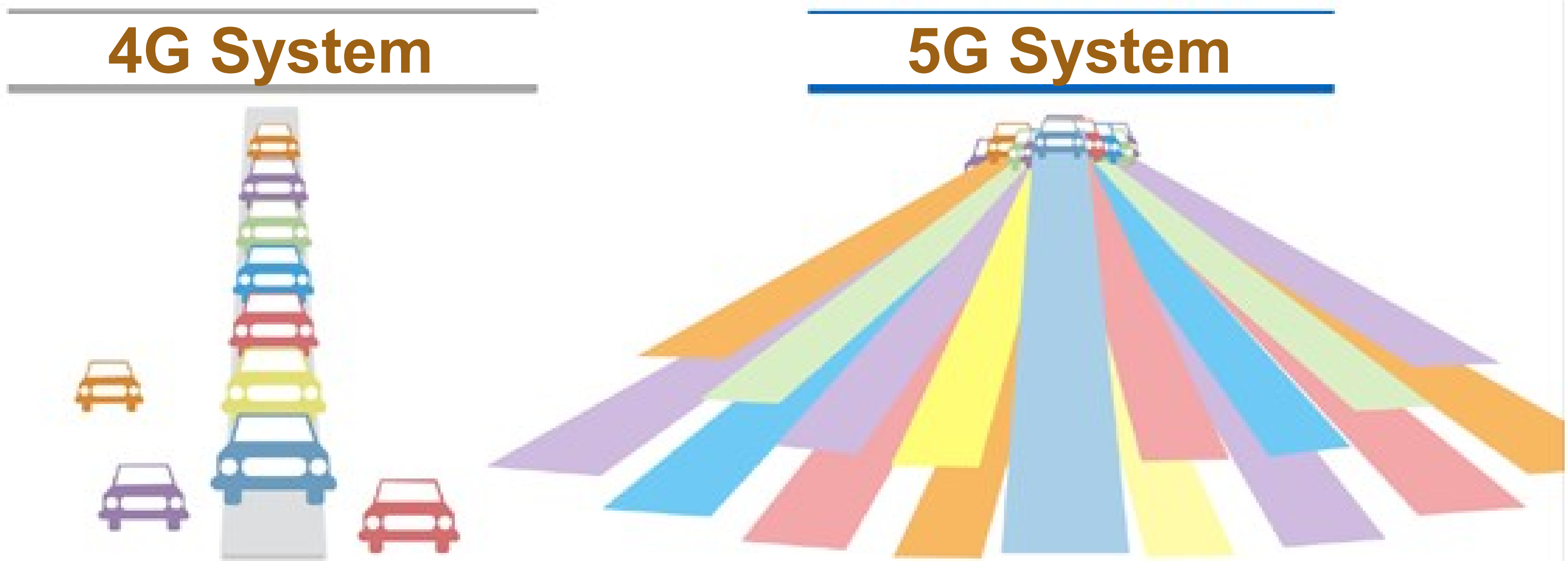


- We think of **very-large** MIMO (multi-user) system
- We mean **M>>K>>1**
- We are looking for **M>100 antennas!**
- We serve **10-20 users** concurrently

F. Rusek, D. Persson, B. K. Lau, E.G. Larsson, T.L. Marzetta, O. Edfors, and F. Tufvesson, "Scaling Up MIMO: Opportunities and Challenges with Very Large Arrays", *IEEE Signal Processing Magazine*, Jan. 2013

LUND UNIVERSITY

Dream case



Massive MIMO for 5G:
Imagine a highway created just for you,
no matter where you are!

Figure source: Softbank, WCP launch '5G Project', deploying 100 Massive MIMO base stations

LUND UNIVERSITY

Dream case

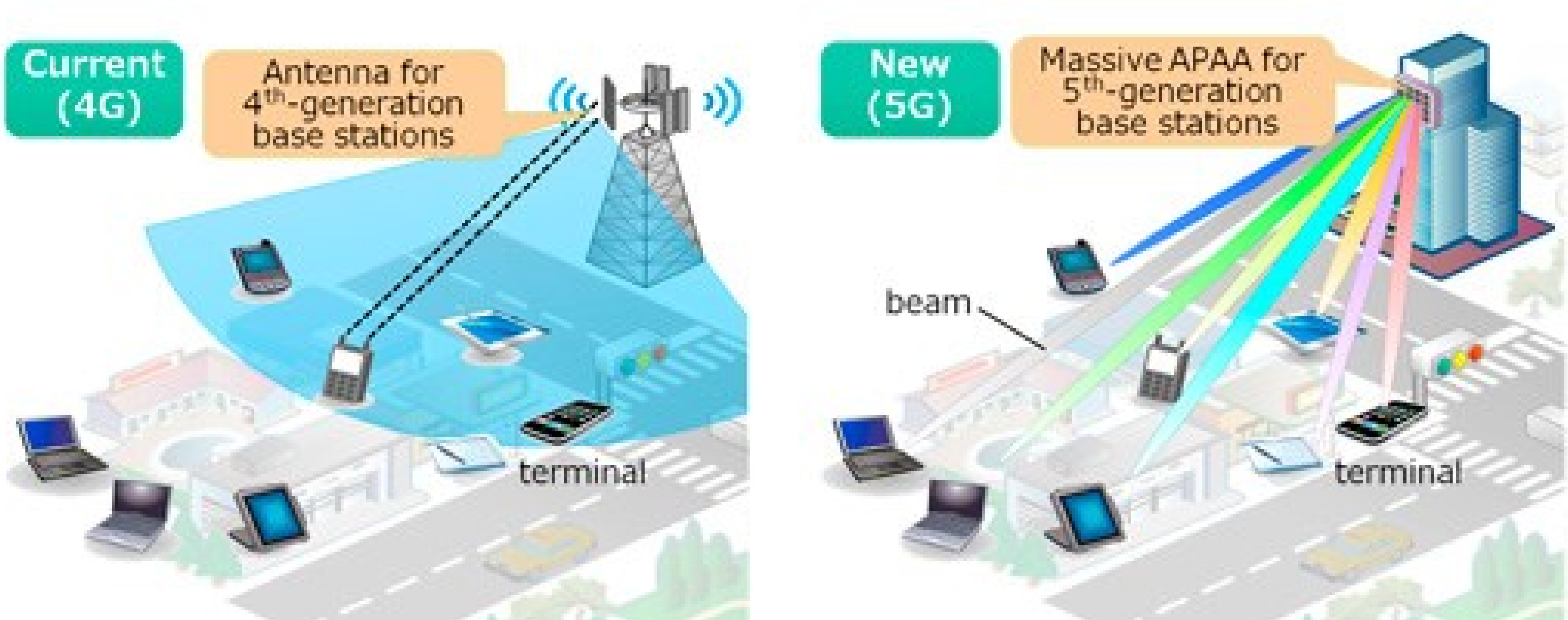
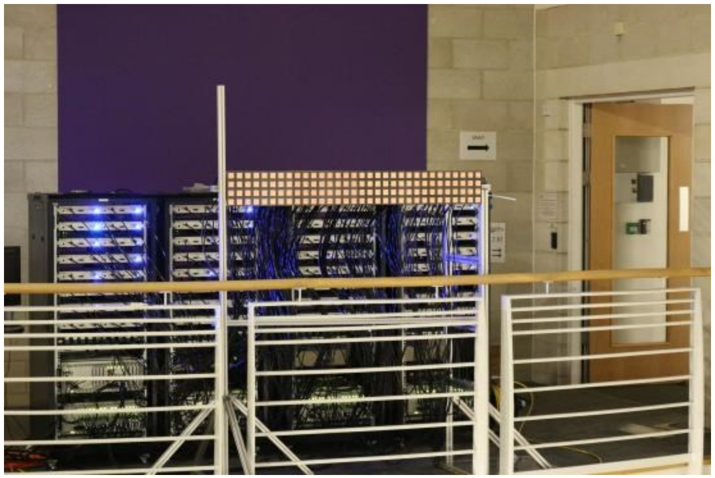


Figure source: "Mitsubishi Electric's New Multibeam Multiplexing 5G Technology Achieves 20Gbps Throughput," 21 January 2016. [Online]. Available: http://www.mitsubishielectric.com/news/2016/0121.html.

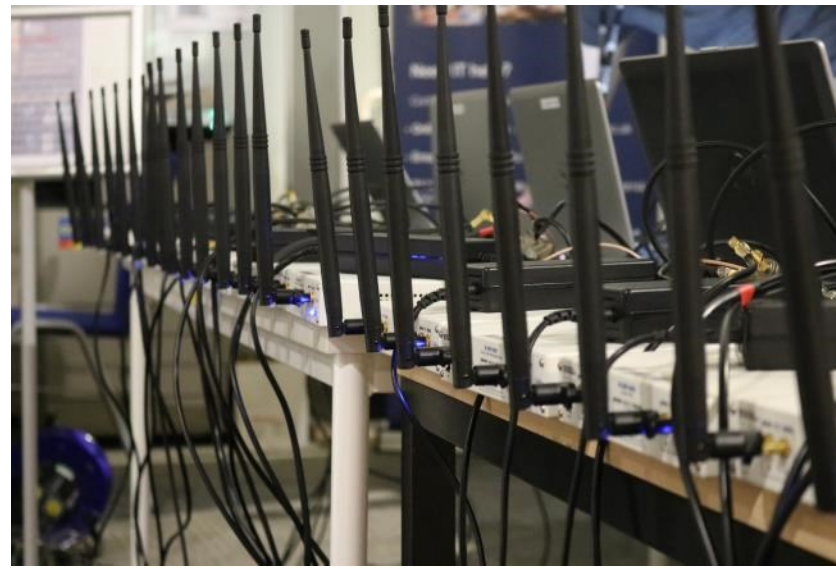
LUND UNIVERSITY

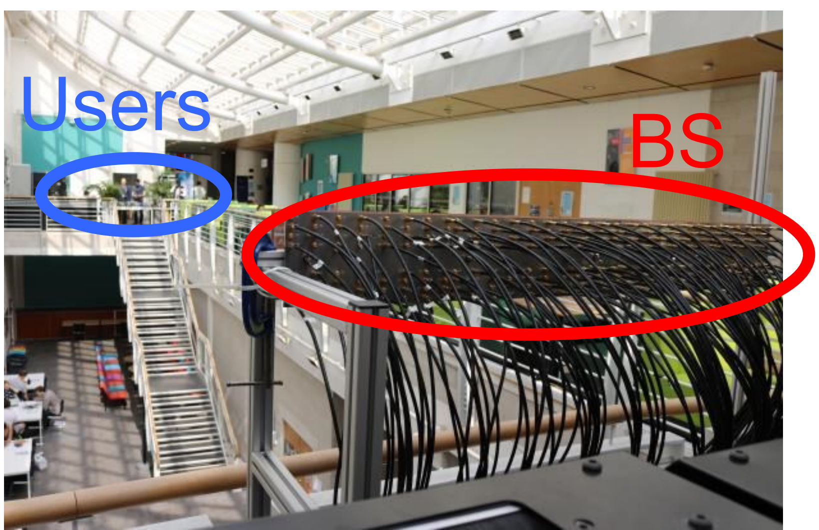
Measurement setup

Base station



Closely spaced users

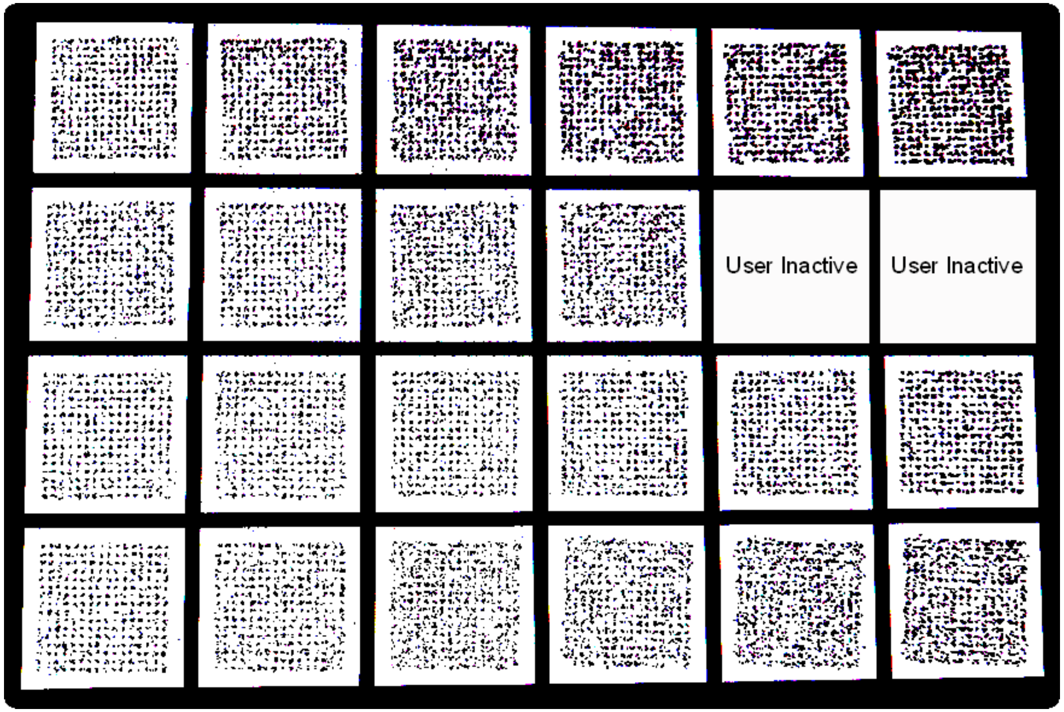




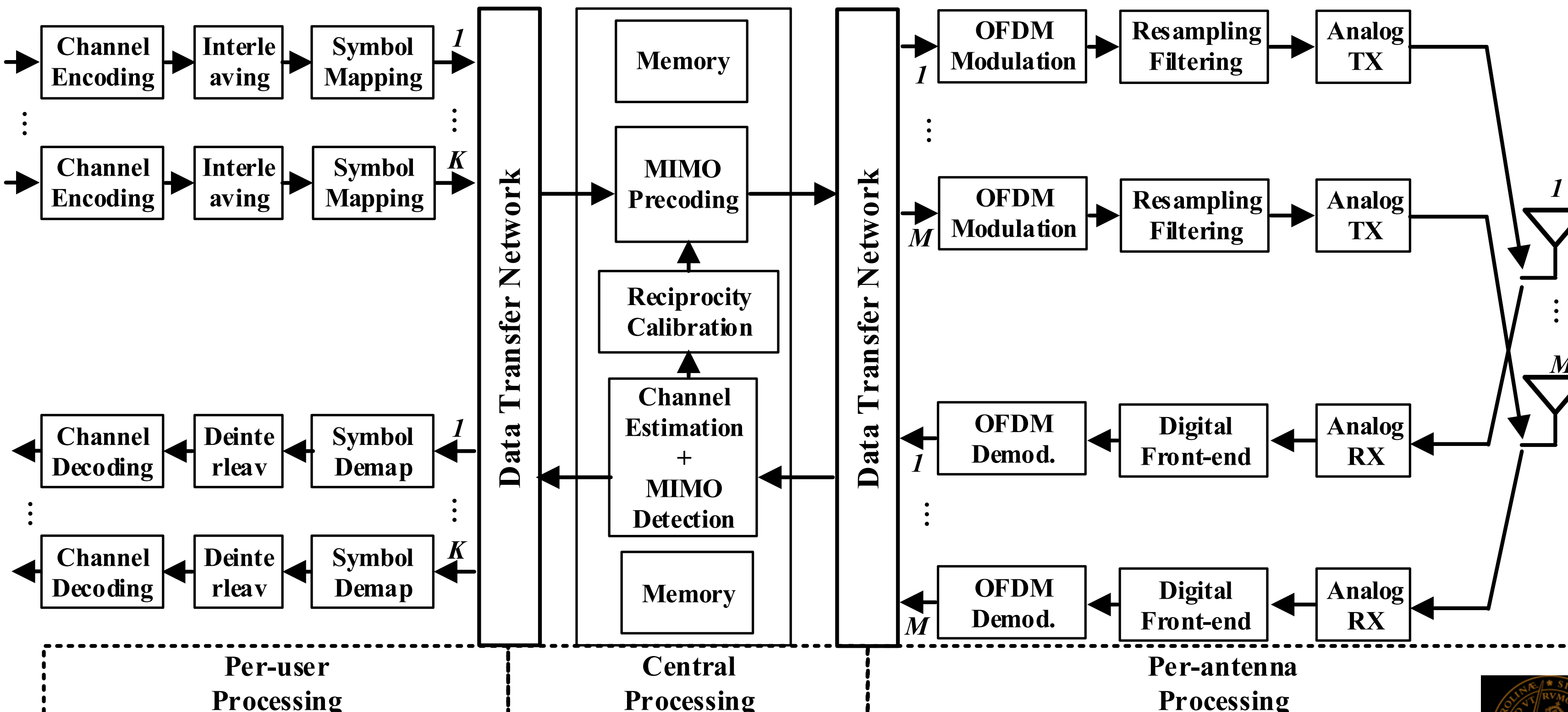
Overall setup from base station view

Measurement results

- 22 closely located UEs (256-QAM) served simultaneously
- Uncoded transmission
- Equating a spectral efficiency of **145 b/s/Hz**



DSP for Massive MIMO



Design challenges

128 × 16 massive MIMO system with 20MHz

➢ High computation count:

- 2×10^{11} multiplication/s for ZF-based MIMO processing

- **1.6×10^7** points per vector detection for 64-QAM, 4 × 4 MIMO

Not just data processing…

Digital Circuits:
Data Processing

Data Transfer

Data Storage

Design challenges

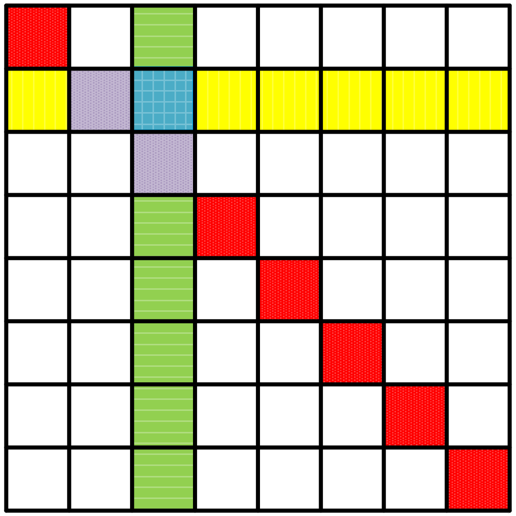
128×16 massive MIMO system with 20MHz

- High computation count:
  - 2×10^{11} multiplication/s for ZF-based MIMO processing
- Large data storage:
  - 9.8MB memory for channel matrix
- Complicated data shuffling:
  - 11GB/s information exchange for 16-bit wordlength

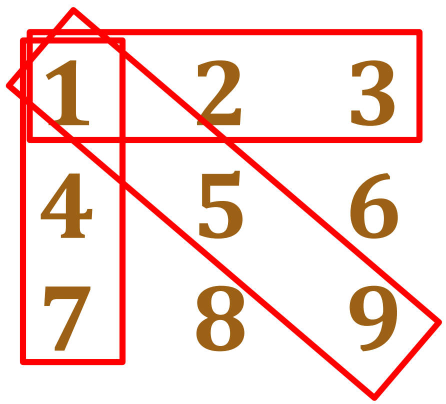
- **1.6×10^7** points per vector detection for 64-QAM, 4×4 MIMO

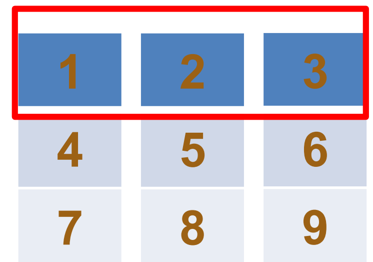
Memory subsystem in Massive MIMO

- High capacity and throughput
  - Channel matrix **128 × 16** in massive MIMO v.s. **4 × 4** in LTE-A
- Multiple access patterns
  - Column wise: $\boldsymbol{H}^{H}\boldsymbol{H}$
  - Row wise: $\boldsymbol{Hy}$
  - Diagonal wise: $\boldsymbol{H}^{H}\boldsymbol{H}+\alpha\boldsymbol{I}$
- Adjustable operand matrix size

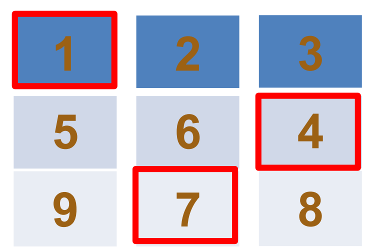


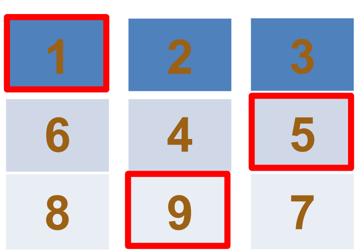
Flexible memory access



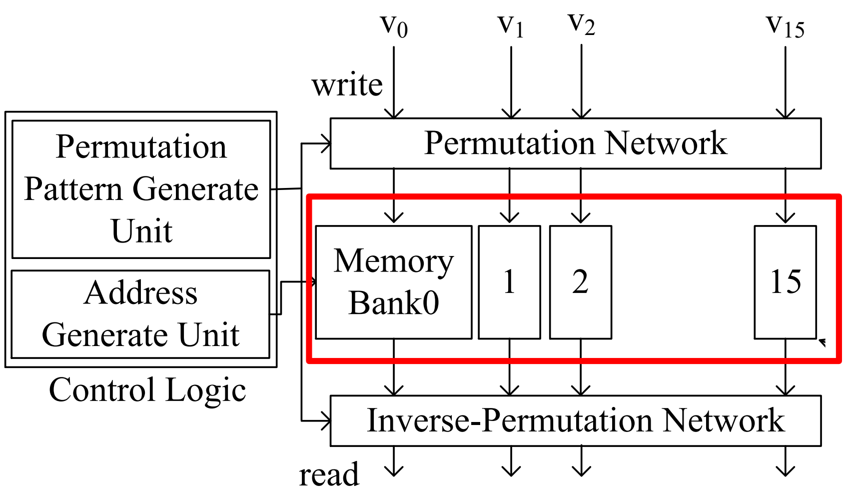


Multi-bank memory





Conflict-free parallel memory scheme



column

row

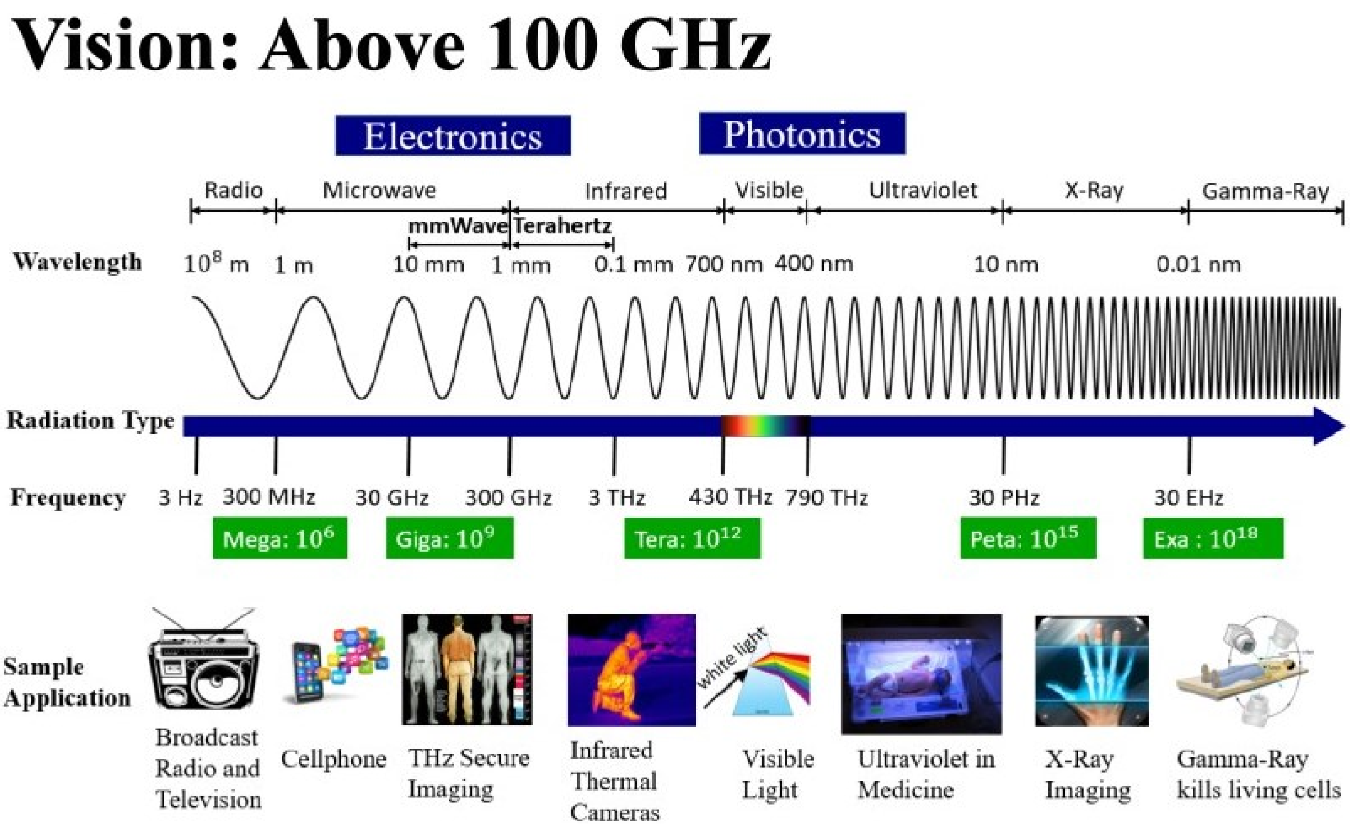
diagonal

16	1	2	3	4	5	6	7	8	9
14	15	16	1	2	3	4	5	6	7
12	13	14	15	16	1	2	3	4	5
10	11	12	13	14	15	16	1	2	3
8	9	10	11	12	13	14	15	16	1
6	7	8	9	10	11	12	13	14	15
4	5	6	7	8	9	10	11	12	13
2	3	4	5	6	7	8	9	10	11
9	8	7	6	5	4	3	2	1	16
11	10	9	8	7	6	5	4	3	2
13	12	11	10	9	8	7	6	5	4
15	14	13	12	11	10	9	8	7	6
1	16	15	14	13	12	11	10	9	8
3	2	1	16	15	14	13	12	11	10
5	4	3	2	1	16	15	14	13	12
7	6	5	4	3	2	1	16	15	14

What can be done to reduce the memory area?

6G?

(sub) THz communication



[1] T. S. Rappaport, Y. Xing, O. Kanhere, S. Ju, A. Alkhateeb, G. C. Trichopoulos, A. Madanayake, S. Mandal, "Wireless Communications and Applications Above 100 GHz: Opportunities and Challenges for 6G and Beyond (Invited)," IEEE ACCESS, submitted Feb. 2019.

Large intelligent surfaces

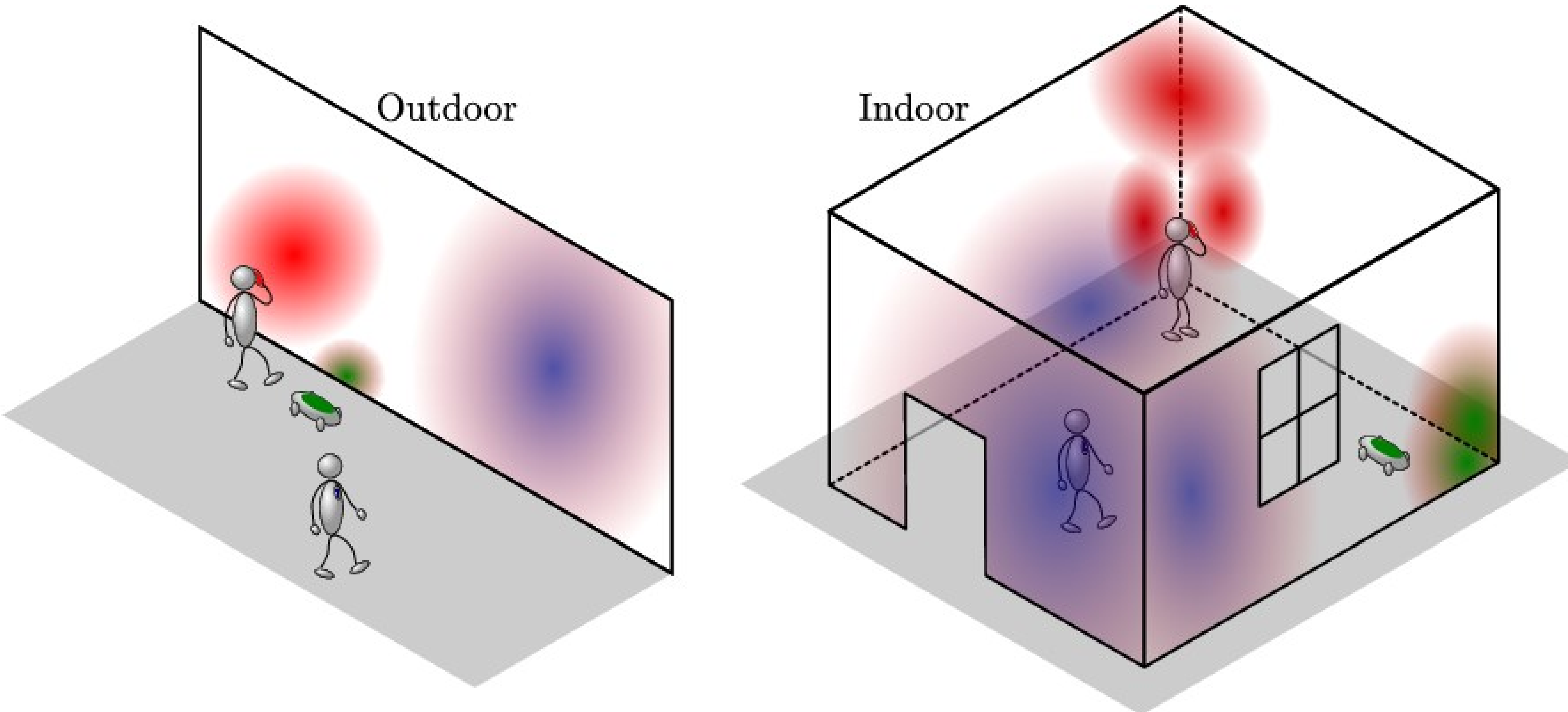


Figure source: Beyond Massive MIMO: The Potential of Data Transmission With Large Intelligent Surfaces

Conclusions

- Digital signal processing is evolving at fast pace with new wireless technologies and applications
- "Optimal" DSP implementation is crucial to bring new DSP algorithm into practice
- "Best" design achieves balanced trade-offs depending on application requirements
- Optimization at earlier stages and do cross-layer (or co-) optimization
- Keep tracking new technologies for both algorithm and implementation

Thanks