DSP-Design 2020
Homework 2

Each person must solve **ALL** exercises!

(1) Consider the lattice filter in Figure 1. The multiplications are to be mapped to a multiplier unit that is pipelined by 2 stages. The additions are executed on a 1-stage pipelined adder. Use the following folding set:

$$S_{A1} = \{A2, A1\} \qquad S_{A2} = \{A3, A4\}$$
$$S_{M1} = \{M1, M2\} \qquad S_{M2} = \{M3, M4\} \qquad S_{M3} = \{—, M5\}$$

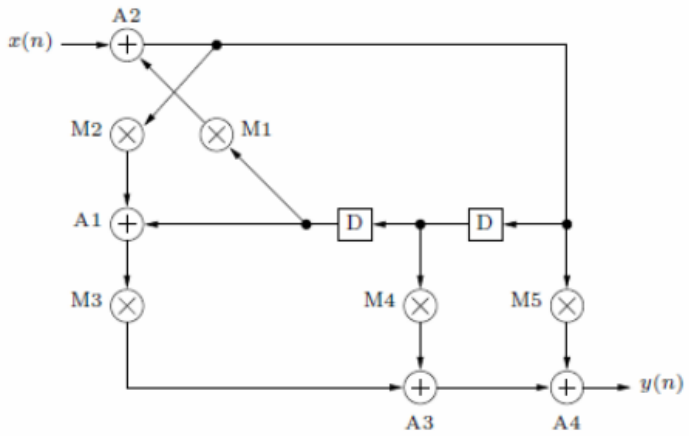

Figure 1: .

(a) Fold the filter with the given folding set. If required perform retiming for folding such that all folded edge delays are nonnegative.

(b) Do a lifetime analysis and reallocate the variables with the forward-backward-algorithm.

(c) Redraw the folded architecture after register minimization.

(2) Consider a FIR filter filter defined by the transfer function

$$H(z) = a + bz^{-1} + bz^{-2} + cz^{-4} + cz^{-5}.$$

Design a 2-parallel filter using the fast FIR approach which uses a minimum number of multipliers.

(3) A recursive computation is given by

$$y(n) = \frac{37}{64}y(n-2) + \frac{15}{64}y(n-3) + \frac{1}{4}x(n).$$

(a) Draw the block diagram for this recursive computation.

(b) How can you realize the multiplications only by shift and add operations? The shift and add operations has to be as minimal as possible.

(c) What is the total number of shifts and adders so required?

(d) Draw the architecture that uses this approach.

(e) List some advantages and disadvantages of the shift and add approach.

(4) Unfold the circuit in the Figure 2 by unfolding factors $J = 2$ and $J = 3$:

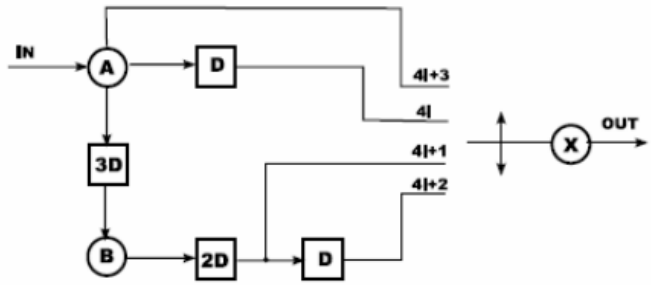

Figure 2: .

(5) You are required to choose an architecture for a 32 tap FIR filter depending on the type of application the filter finds itself in. The arithmetic units i.e. the multiplier and adder has propagation delay of 2 ns and 1 ns respectivey. The delay introduced by the registers is neglected. Furthermore all the signals are in the range $-1 \leq x < 1$.

(a) Propose a filter architecture when a sampling rate greater than 200 M samples/s is required. Motivate your choice of architecture by comparing with alternative architectures. What is the throughput of your proposed architecture.

(b) In another application, the sampling rate required is < 50 M samples/s. Propose another architecture that exploits this relaxed design requirement to reduce the arithmetic complexity.
At what throughput rate does this architecture run at?

(6) A variable x can be multiplied by a given set of fixed-point constants using a multiplier block that consists exclusively of shifts, additions and/or subtractions. The generation of a multiplier block from a set of constants is known as multiple constant multiplication (MCM).

a) Decompose the multiplication 71x into adds and shifts. How many adds and shifts do you need to perform the multiplication in this case? Draw a graphical representaion of the decomposition.

b) Decompose the multiplication 71x into substracts and shifts. How many substracts and shifts do you need to perform the multiplication in this case? Draw a graphical representaion of the decomposition.

c) Decomposes the multiplication 71x into both adds, subtracts and shifts by recoding the number into the canonical signed digit (CSD) representation. How many adds, substracts and shifts do you need to perform the multiplication in this case? Draw a graphical representaion of the decomposition.

(7) Unfold the switch in Figure 3. three times (J=3).

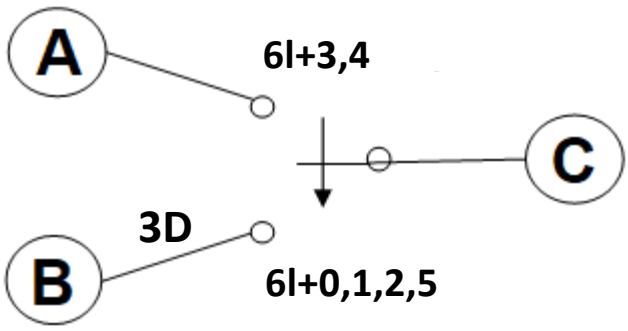

Figure 3.