ETIN35 – Digital IC Project 1

ASIC DESIGN FLOW OF MATRIX MULTIPLIER

By

XXXX YYYY

WWWW ZZZZ

Department of Electrical and Information Technology
Faculty of Engineering, LTH, Lund University
SE-221 00 Lund, Sweden

LUND UNIVERSITY

VT-1 2020

Abstract

The main objective of this project…

In the RTL design…

In order to provide a physical architecture to our RTL design…

The synthesized design is…

Table of contents

1. Design Specifications

The overall architecture was designed for…

In the RTL level…

We also focused on…

Signal	Direction	Number of pads	Utilization
clk	Input	1	Clock of the system
rst	Input	1	Reset of the system
-	-	-	-
-	-	-	-
-	-	-	-
Input	Input	8	Data input
Output	Output	18	Data output

Table 1. Design pads utilization

2. ASMD

For the architecture definition we drew an ASMD for each state machine used in the project…

Figure 1. Input buffer ASMD

This state machine was used for storing…

The other ASMD in the XXXX module is used…

Figure 2. Address switching ASMD

In this state machine when the *start* signal is set high…

A counter called *count is used* to…

In the Multiplier Unit we have defined an ASMD for…

Figure 3. Multiplier Unit ASMD

This state machine remains in the initial *idle* state until…

For the calculating the average of diagonal elements…

Figure 4. Diagonal average ASMD

The next figure shows the ASMD used for calculating the maximum value of the matrx…

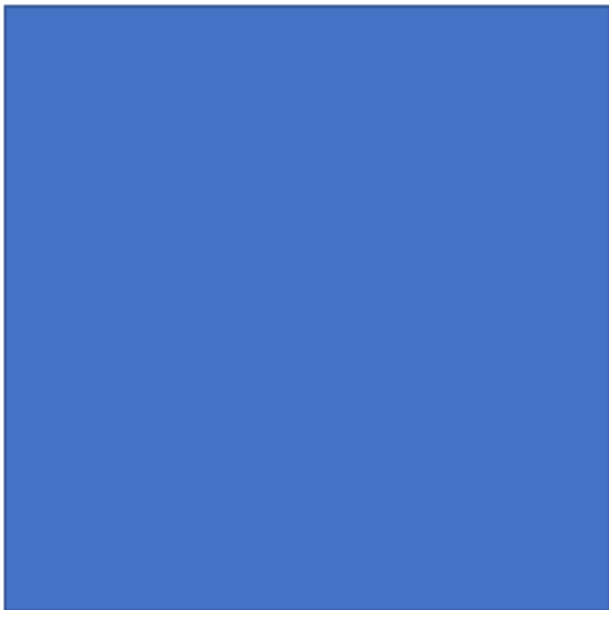

Figure 5. Max calculation ASMD

3. RTL

Once we defined the ASMD for each module of the project…

Figure 6. Design block diagram

The *TOP* module includes…

When reading from…

The *Controller* module…

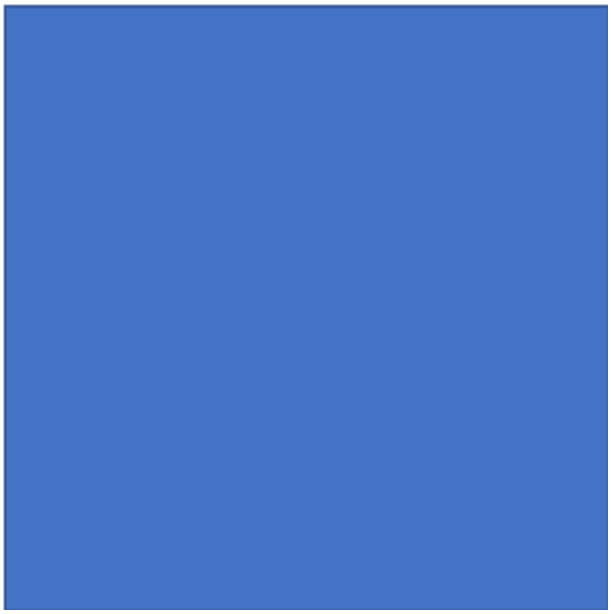

Figure 7. Controller module hardware representation

For the *Multiplier Unit*…

Figure 8. Multiplier Unit hardware representation

The system has been pipelined including registers after each operation…

The *Post Processing* module calculates…

Figure 9. Diagonal average calculation hardware representation

In the same module we have included…

Figure 10. Max calculation hardware representation

XX clock cycles are needed for the calculation and storing of one result matrix…

4. Synthesis

The synthesis has been…

The tool performed…

Figure 11. Synthesis schematic generated

The above figure shows the schematic of the top-level design generated after synthesis…

4.1. Timing Reports

After Synthesis, the maximum sampling frequency of the design was…

The critical path includes the…

Figure 12. Critical Path

Figure 13. Second Longest Path

The second longest path includes the…

4.2. Power Reports

The leakage power was XX nW and dynamic power consumption was XX mW…

The next figures summarize the power consumed per each module of the synthesis…

Figure 14. Power Report for High Throughput

Figure 15. Low Power Consumption at Lesser Sampling Frequency

Reducing the system frequency, the total power is reduced from XX mW to XX mW. This means a power reduction of XX %...

4.3. Area Reports

The next figure is the synthesis result of the area used by our design working at XX MHz…

Figure 16. Area Report

The total area defined by the synthesis report is XX μm^2.

5. Place and Route

This process is…

The next figure is the layout generated after finishing the Place and Route process…

Figure 17. Layout of the initial design

5.1. Timing Reports

Timing reports generally includes…

5.1.1. Setup time

The next two figures show the results of the timing reports for setup before and after optimization…

Figure 18. Setup Timing Report before Optimization

Figure 19. Setup Timing Report after Optimization

5.1.2. Hold time

The next two figures show the results of the timing reports for hold before and after optimization…

Figure 20. Hold Timing Report before Optimization

Figure 21. Hold Timing Report after Optimization

6. Post Layout Simulations

The post layout simulations…

The netlist and the SDF (Standard Delay Format) file…

The figure below shows the simulations of the top level instance after…

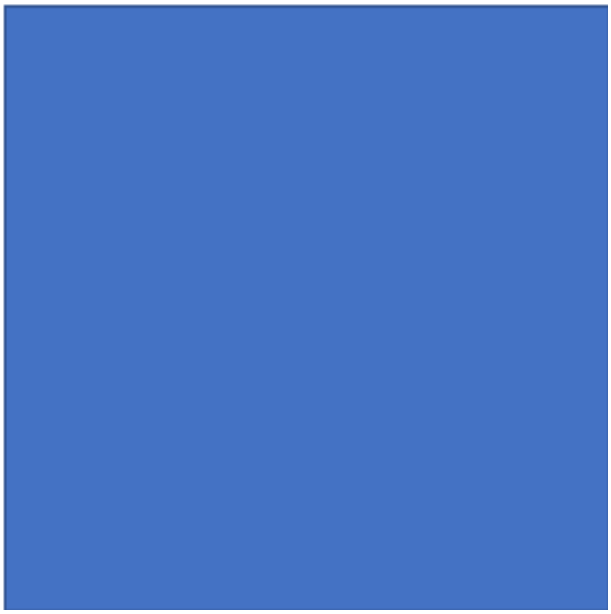

Figure 22. Post Layout Simulations

7. Power and STA Simulations

Prime Time was used for Static Timing Analysis and Power simulations…

8. Optimizations

We optimized further in our initial design in order to enhance…

To implement this optimization, first…

Figure 23. Post process output area optimized ASMD

For the implementation of this ASMD we have done some modifications in the hardware architecture…

Figure 24. Design block diagram optimized

The next figure illustrates the hardware implemented for this process…

Figure 25. Output definition hardware representation

The new design with the modifications were used for doing the Synthesis and the Place and Route processes again. The layout result is showed in the following figure…

Figure 26. Layout of the optimized design

With the area optimizations, the new layout presents a core utilization of XX %...

8.1. Timing Reports

Figure 27. Timing report for the optimized design

8.2. Power Reports

Figure 28 Power consumption of the optimized design

From the above reports, the power consumption of the optimized design reduced from **XX µW** (initial design) to **XX µW.** This means an improvement of XX % in power consumption.

8.3. Area Reports

Figure 29. Area report for the optimized design

The design area of the optimized design cut down from **XX µm²** to **XX µm².** This means an improvement of XX % of area.

9. Conclusion

The design of Matrix Multiplier was…

10. Appendix

10.1. Synthesis script

10.2. Place and Route script

10.3. Power simulation script