

Backend Tools

Place and Route

STM 65nm

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Import Design

- This step will take a while. Be patient and pick exactly the files specified in the guide.
- It is possible to save/load settings using the Save button.
 Do this to avoid browsing for all files multiple times.
 This applies both to Design Import and Create Analysis Configuration.
- It is important that all files are included and in the correct order.
 Look for possible errors in the command prompt.
- If you need to re-import your design the tool needs to be restarted.



Import Design

- File -> Import Design
- You should enter:
 - Netlist + Top Cell
 - LEF files
 - IO file
 - Power
 - MMMC definition file (Use Create Analysis Configuration).

| Des | ign Impert (on khalid.fransg) _ 🗆 × |
|------------------------------|-------------------------------------|
| Netlist: | 20 |
| Verilog | |
| Files: | |
| | Top Cell: 🔾 Auto Assign 💿 By User: |
| ○ OA | |
| Library: | |
| Cell: | |
| View: | |
| Technology/Physical Librarie | s: |
| ● OA | |
| Reference Libraries: | |
| Abstract View Names: | |
| Layout View Names: | |
| C LEF Files | |
| Floorplan | |
| IO Assignment File: | <u></u> |
| Power | |
| Power Nets: | |
| Ground Nets: | |
| CPF File: | 6 |
| Analysis Configuration | |
| MMMC View Definition File: | 6 |
| | Create Analysis Configuration) |



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Import Design – LEF files

Folder for backend files:

Text

LEFs - Physical information (pins and Metal Layers)

TECH/cmos065_7m4x0y2z_AP_Worst.lef - Header LEF

 CORE65<ProcessVToption>_5.1/CADENCE/LEF/ CORE65<ProcessVToption>_soc.lef

 CLOCK65<ProcessVToption>_3.1/CADENCE/LEF/ CLOCK65<ProcessVToption>_soc.lef

- PRHS65_7.0.a/CADENCE/LEF/PRHS65_soc.lef

– IO65LPHVT_SF_1V8_50A_7M4X0Y2Z_7.0/CADENCE/LEF/ IO65LPHVT_SF_1V8_50A_7M4X0Y2Z_soc.lef

- IO65LP_SF_BASIC_50A_ST_7M4X0Y2Z_7.2/CADENCE/LEF/ IO65LP_SF_BASIC_50A_ST_7M4X0Y2Z_soc.lef NHAW SIGIL

Import Design – Timing Files

• Folder for backend files:

Text

• Libs:

Clock dir: DESIGN_KIT_ROOT/CLOCK65<ProcessVToption>_3.1/lib

Core dir: DESIGN_KIT_ROOT/CORE65<ProcessVToption>_5.1/lib

Variation key for timing libraries

- <LibraryName>65<ProcessVToption>_<corner>_<Voltage>_<temperature>_<age>.lib
- LibraryName: CORE, CLOCK
- ProcessVToption: LPHVT, LPSVT, LPLVT, GPHVT, GPSVT, GPLVT (use same for all libraries)
- Corners: Worst Case (wc), nominal (nom), Best Case (bc),
- Voltage: 0.90V (wc) 1.30V (bc)
- Temperature: -40°C (m40C) to 125°C (125C)
- Age: 10 years aging (10y)
- CORE65LPHVT_wc_1.05V_m40C_10y.lib

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Import Design - Memories

• Memories are found in memory directory.

*.lef files in LEF directory

*.lib files in lib directory



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Import Design

- After you have entered:
 - Netlist + Top Cell
 - LEF files
 - IO file
 - Power
- It should look something like this.
- First: Click Save.
- Afterwards: Click on Create Analysis Configuration

| 🖲 Verilog | |
|---------------------------|---|
| Files: | /././median_filter/netlists/medfilt.v |
| | Top Cell: 🔾 Auto Assign 🥑 By User: MEDIANFILTER_N8 |
| OA 🔾 | |
| Library: | |
| Cell: | |
| View: | |
| Technology/Physical Libr | aries: |
| O OA | |
| Reference Libraries: | |
| Abstract View Names: | |
| Layout View Names: | |
| LEF Files | 'SHLD130_128X32X1BM1.lef ./././mem2015/SPLD130_512X14BM1A.lef |
| Floorplan | |
| IO Assignment File: | //median_filter/soc/MedFilt.io |
| Power | |
| Power Nets: | vcc 📐 |
| Ground Nets: | |
| CPF File: | |
| Analysis Configuration — | |
| MMMC View Definition File | e [|
| | 11 ⁻ |

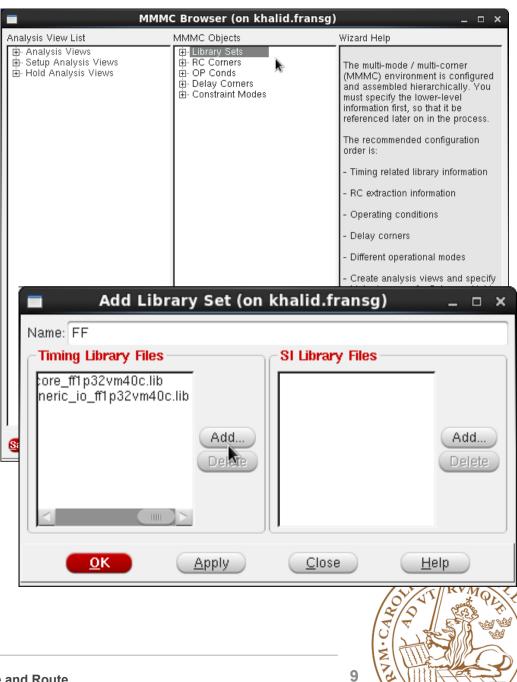


- The empty configuration looks like this.
- Feel free to read the wizard about Multi-mode-multi-corner.
- The idea is to analyze the designed chip in multiple environments at different manufacturing process variations. To make sure the fabricated chip works in all cases.
- We will now pupulate elements in the MMMC viewer.

| M M | MMC Browser (on khalid.fran | 1sg) _ 🗆 |
|--|--|---|
| Analysis View List | MMMC Objects | Wizard Help |
| ⊕- Analysis Views ⊕- Setup Analysis Views ⊕- Hold Analysis Views | ⊕- Library Sets ⊕- RC Corners ⊕- OP Conds ⊕- Delay Corners ⊕- Constraint Modes | The multi-mode / multi-corner (MMMC) environment is configured and assembled hierarchically. You must specify the lower-level information first, so that it be referenced later on in the process. |
| | | The recommended configuration order is: |
| | | - Timing related library information |
| | | - RC extraction information |
| | | - Operating conditions |
| | | - Delay corners |
| | | - Different operational modes |
| | | Create analysis views and specif which views are for Setup vs. Hold analysis |
| | | The wizard will take you through each of these required steps in the order shown above. |
| | | Press Next to being specifying timing library information. |
| | | |
| | | Prev |
| Save&Close | Delete Reset Preferences) | <u>W</u> izard Off <u>C</u> lose <u>H</u> elp |



- Start by right clicking on Library set and select New.
- Create one set FF for best case timing
 - Add the best case timing libraries.
 - Shown on Previous slide, don't forget the memory files (not shown in figure).
- Create a similar set SS for worst case timing.



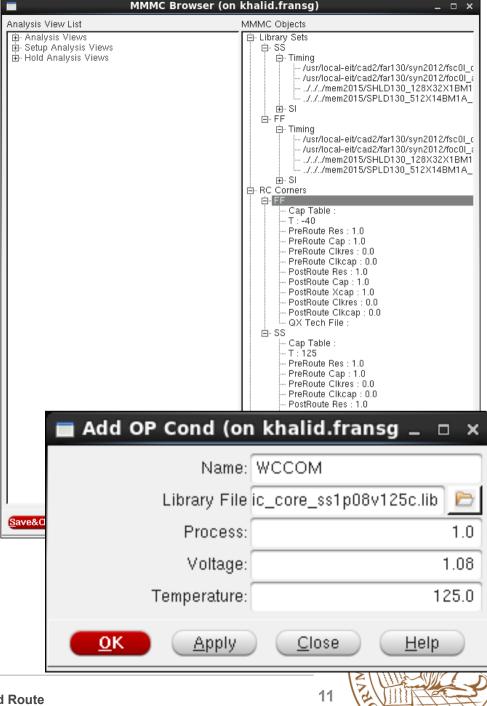
Anal

- Continue to create two RC corners.
- Create one FF for best case timing
 - Change Temperature to -40°C.
- Use 125°C for Worst Case (SS).

| | MMMC Browser (on khalid.fransg) | _ = × |
|---|---|--|
| ysis View List Analysis Views Setup Analysis Views Hold Analysis Views | | ocal-eit/cad2/far130/syn2012/fsc0l_c ocal-eit/cad2/far130/syn2012/foc0l_s /mem2015/SHLD130_128X32X1BM1 /mem2015/SPLD130_512X14BM1A_ ocal-eit/cad2/far130/syn2012/fsc0l_c ocal-eit/cad2/far130/syn2012/foc0l_s /mem2015/SHLD130_128X32X1BM1 /mem2015/SPLD130_512X14BM1A_ |
| e&Close | Edit RC Corner (on khali Name: Cap Table Temperature: PreRoute Resistance Scale Factor: PreRoute Cap Scale Factor: PreRoute Clock Resistance Scale Factor: PostRoute Resistance Scale Factor: PostRoute Resistance Scale Factor: PostRoute Cap Scale Factor: PostRoute Xcap Scale Factor: PostRoute Clock Resistance Scale Factor: PostRoute Clock Resistance Scale Factor: PostRoute Clock Cap Scale Factor: QRC Technology File | ÷ |

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- Create two OpConds.
- Name them: WCCOM – (SS) Worst Case BCCOM – (FF) Best Case
- These are operating conditions defined in the lib files, and therefore, named different.
- Use the Voltage and Temperature for the specific library.



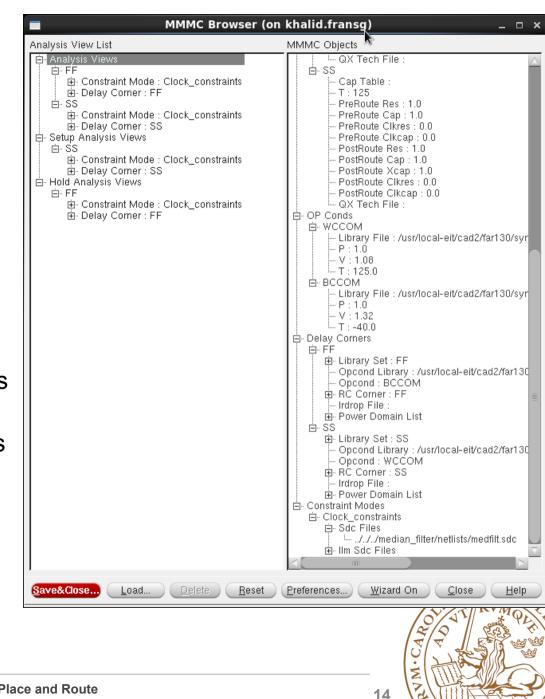
- Add two delay corners. FF, and SS.
- Choose the existing RC corner and corresponding Library Set.
- Enter the OpCond and copy the Opcond Lib from the previous OpCond dialog.

| | Edit Delay Corne | r (on khalid.frantg) 🛛 🗆 🛪 🔤 |
|--|--|--|
| | Name: FF | |
| Analysis View List | Power Domain List | Туре |
| i ⊕- Analysis Views i ⊕- Setup Analysis Vie | default | ○ On Chip Variation ● Single/BcWc //fsc0 //foc0 |
| ⊞. Hold Analysis Vie | | Attributes |
| | | RC Corner: FF |
| | | Library Set: FF |
| | | OpCond Lib: generic_core_ff1p32vm40c.lib |
| | | OpCond: BCCOM |
| | | IrDrop File: |
| | | Early |
| | Add | Library Set: |
| | Delete | OpCond Lib: |
| | | OpCond: |
| | | IrDrop File: |
| | | Late |
| | | Library Set: |
| | | OpCond Lib: |
| | | OpCond: |
| | | IrDrop File: |
| | | |
| | <u>OK</u> <u>Apply</u> | <u>Close</u> <u>H</u> elp |
| l | | |
| | E | ⊖ OP Conds ⊖ WCCOM |
| | | Library File : /usr/local-eit/cad2/far130/syr P : 1.0 |
| | | V : 1.08 |
| | | □ |
| | | - Library File : /usr/local-eit/cad2/far130/syr |
| | | P : 1.0 V : 1.32 |
| | | L - T:-40.0 ⊕ Delay Corners |
| | | ⊡ Constraint Modes |
| ļ | K | |
| Save&Close | ad <u>D</u> elete <u>R</u> eset <u>P</u> r | references) <u>W</u> izard On <u>C</u> lose <u>H</u> elp |
| | | N S KVMO |
| | | A A A A A A A A A A A A A A A A A A A |
| | | AL TELE |
| | | |
| | | 3 |
| lace and Route | | |
| | | |

 Now add the clock constraints from the SDC file (created during synthesis).



- Now it is time to combine all this information.
- Create two Analysis views using the existing Delay corner and Constraint Mode.
- Select to SS Analysis View as Setup Analysis View
- Select to FF Analysis View as Hold Analysis View
- The design should look like the screenshot.
- Do not forget to save the MMMC file.

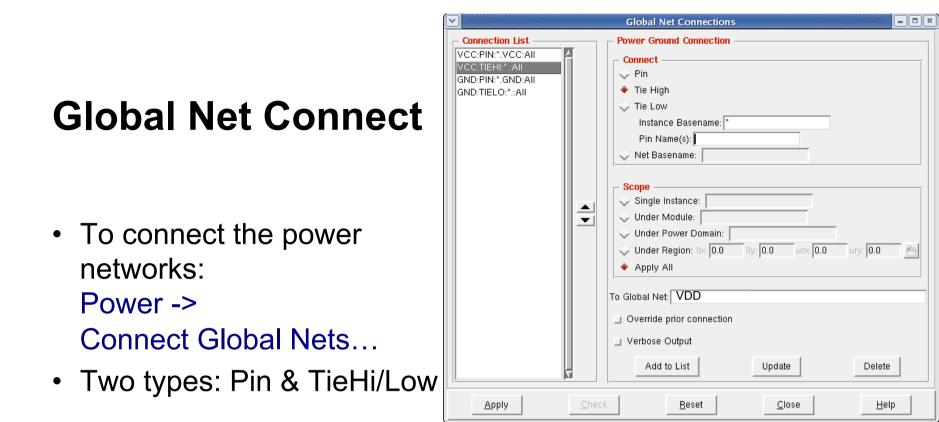


Import Design

- It should now look something like this.
- First: Click Save.
- Afterwards: Click on OK
- Next time you can use Load instead, and skip browsing for all files.

| | Design Import (on khalid.fransg) _ 🗆 🗆 |
|--------------------------|--|
| Netlist: | |
| 🖲 Verilog | |
| Files: | |
| | Top Cell: 🔾 Auto Assign 💿 By User: MEDIANFILTER_N8 |
| OA OA | |
| Library: | |
| Cell: | |
| View: | |
| Technology/Physical Lib | raries: |
| O OA | |
| Reference Libraries: | |
| Abstract View Names: | |
| Layout View Names: | |
| LEF Files | SHLD130_128X32X1BM1.lef ./././mem2015/SPLD130_512X14BM1A.lef |
| Floorplan | |
| IO Assignment File: | |
| Power | A. |
| Power Nets: | VDD |
| Ground Nets: | GND |
| | |
| CPF File: | |
| | |
| Analysis Configuration - | e://far130/far130_mmmc.view |





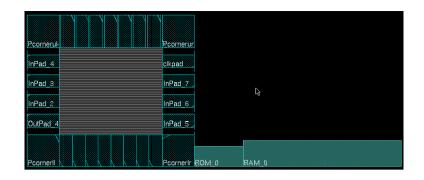
- Power network, e.g., VDD connect to TIEHI, Pin VDD
- Ground network, e.g., GND connects to TIELO, Pin GND.
- Scope: Apply All

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Floorplan

- Resize floorplan to fit memories
- Floorplan -> Specify Floorplan
- The size of memories can be measured with the ruler tool.
- To zoom use the zoom buttons:
 Q Q Q
- Zoom in (z), Zoom out (shift+z), Fit to screen (f)
- Also right-click and drag a square to zoom in a to a desired area.



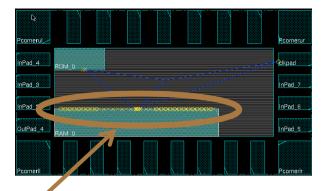


| Specify Floorp | lan | |
|-------------------------------------|-----------------------------|-----|
| Basic Advanced | | |
| – Design Dimensions – | | |
| Specify By: 🔶 Size 🕹 Die/IO/Core Co | pordinates | |
| 🔶 Core Size by: 🐳 Aspect Ratio: | Ratio (H/W): 0.84279835 | |
| | Core Utilization: 0.590363 | |
| | Cell Utilization: 0.028826 | |
| Dimension: | Width: 1000.0 | |
| | Height: 400.0 | |
| 🔷 Die Size by: | Width: 790.0 | |
| | Height: 713.6 | |
| Core Margins by: 🔶 Core to IO Bound | dary | |
| 🕹 Core to Die Bour | ndary | |
| | Core to Top: 20 | |
| Core to Right: 20 | Core to Bottom: 20 | |
| Die Size Calculation Use: 🔶 Max | < IO Height 🔶 Min IO Height | |
| Floorplan Origin at: 🔶 Low | • | |
| | Unit: Micr | ron |
| <u>ок</u> | <u>C</u> ancel <u>H</u> elp | |



Place and rotate memories

- Need to rotate memories to have pin connections inside the core.
- Rotate memories by edit proporties for selected object by pressing "q".
- Orientation set to R180 for 180 degree rotation.
- Afterwards change to normal pointer by selecting the arrow next to or press "a".



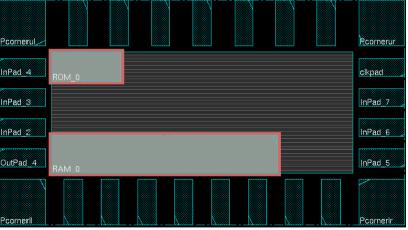
| | Attribu | te Editor | | | × |
|------------------------|-------------------|----------------------|---------------|-------------|---|
| Object Type: Block | < | | | | |
| N | ame | Value | Ту | pe | |
| Name | RAM_0 | | | String | |
| No. of Terminals | 75 | | | Integer | |
| Cell Type | SHUD130_128X32> | (1BM1 | | String | |
| Cell Width | 750.0 | | | Double | |
| Cell Height | 124.0 | | | Double | |
| Location | X: 1574.4 | Y: 0.0 | è | Location | |
| Location Origin | Lower Left 🛁 | | | Origin | |
| Orientation | <u>R0</u> | | | Orientation | |
| Status | UNPLACED 🛁 | | | Enumerate | |
| Routing Halo | None | | | String | |
| InstGroup | None | | | String | |
| | | | | | |
| <u> </u> | | | | | |
| <u>OK</u> <u>Apply</u> | A <u>d</u> d Prop | D <u>e</u> lete Prop | <u>C</u> lose | Help | |



Add Halo

- Floorplan -> Edit Floorplan -> Edit Halo
- To create a ring around the memory macro, where no standard cells can be placed.
- Routing is still possible
- Be sure to specify a distance, e.g. 10 μm.

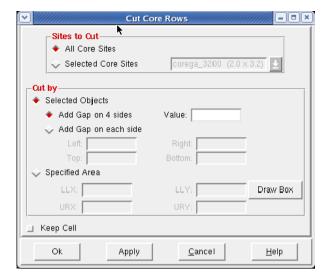
| Edit Halo |
|---|
| Specify Halo For ◆ All Blocks ◇ Selected Blocks/Pads ◇ Design |
| 🕹 Routing Halo |
| ♦ Add/Update |
| Halo Value: 0 um |
| Bottom Layer: M1 🛁 Top Layer : M8 🛁 |
| 🕹 Remove |
| Placement Halo |
| Add/Update Block Halo |
| Top: 10 μ um Bottom: 10 um |
| Left: 10 um Right: 10 um |
| 🗸 Remove Block Halo |
| <u>O</u> K <u>Apply</u> <u>Cancel Help</u> |

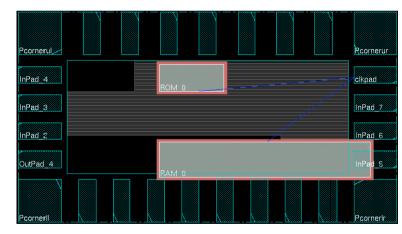




Cut Rows

- Floorplan -> Row -> Cut Core Row
- Deletes core rows beneath memories.
- NOTE: Be sure to select memories before cutting.
- Now is a good time to save the design:
 File -> Save Design Data Type: Encounter
- To restore:
 File -> Restore Design
- By moving memories, the cut rows are shown.
- Use undo to move back.





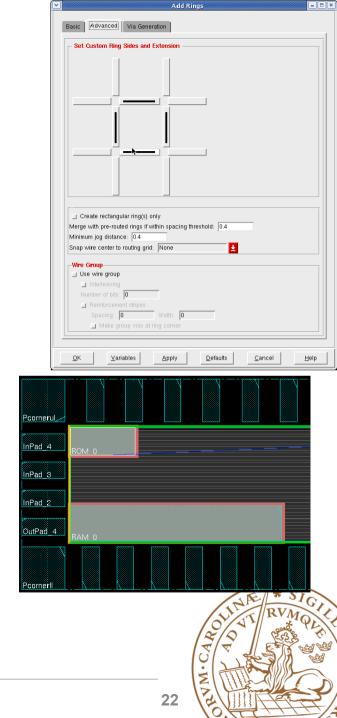


- Power -> Power Planning -> Add Rings
- To add Power rings around core specify Width: 2, Spacing: 2, Offset 2.
- Use metal3 for Horizontal wires and metal4 for Vertical wires.

| Net(s): | GND VCC | | | | _ | | |
|----------|-----------------------|-------------|-----------|---------------|--------|----------|---------------------|
| ., | 1. | | | | | | |
| Ring Ty | pe ring(s) contour | na | | | | | |
| | round core bou | - | - 21 | Along I/O bou | Indarv | | |
| | kclude selected | | ¥ . | | , | | |
| | k ring(s) around | ĺ. | | | | | |
| ↓ E | ach block | | | | | | |
| ↓ E | ach reef | | | | | | |
| 🔶 S | elected power (| domain/fend | ces/reefs | | | | |
| | ach selected bl | | | | | | |
| * | lusters of selec | | | roups of core | | | |
| I | With shared r | ing edges | | | | | |
| 🔶 User | defined coordir | lates: | | | | N | <u>/l</u> ouseClick |
| • | Core ring | 🔶 Block i | | | | | |
| Ring Co | nfiguration — | | | | | | |
| | Top: | Bottom | | Left: | Right: | | |
| .ayer: | metal3 H | → metal3 | | metal4 V | metal4 | v[| |
| Width: | 2 | 2 | | 2 | 2 | <u> </u> | |
| | | 2 | _ | 2 | 2 | _ | Update |
| Spacing: | , | 1 | | 1- | 14 | | Obgare |
| Offset: | ♦ Center in c | | Species | · | | | |
| | 2 | 2 | 2 | 2 | | | |
| | Set | | | | | | |
| Option | | | | | | 1 | |
| | ption set: | | | FCM | | | |



- Make sure that an entire ring is visible under the advanced tab.
- If applied correctly your design should look like this.



- Select the memory macros and select as in the figure.
- This will create a block ring around the memory block.
- Used to connect VDD and GND for memory.
- If memories are placed along the border of the die, some powerrouting can be re-used.

| Net(s): | |
|-------------------------------------|--|
| | GND VCC |
| Ring Ty | pe |
| 🔶 Core | e ring(s) contouring |
| - 🔶 / | Around core boundary 🔷 Along I/O boundary |
| | xclude selected objects |
| Bloc | k ring(s) around |
| - 🔶 E | Each block |
| - 🔶 E | Each reef |
| \sim : | Selected power domain/fences/reefs |
| 🔶 E | Each selected block and/or group of core rows |
| | Clusters of selected blocks and/or groups of core rows |
| | ■ With shared ring edges |
| 🔷 Usei | r defined coordinates: MouseClick |
| • | Core ring V Block ring |
| | |
| Ring C | onfiguration |
| | Top: Bottom: Left: Right: |
| Layer: | metal3 H 🔟 metal3 H 🔟 metal4 V 🔟 metal4 V 🚽 |
| Width: | 2 2 2 |
| | 2 2 2 2 Update |
| | i c i c i c i c i c i update |
| Spacing | |
| Spacing | ✓ Center in channel ◆ Specify |
| Spacing Offset: | |
| Spacing Offset: | Center in channel Specify |
| Spacing Offset: Option | Center in channel Specify |



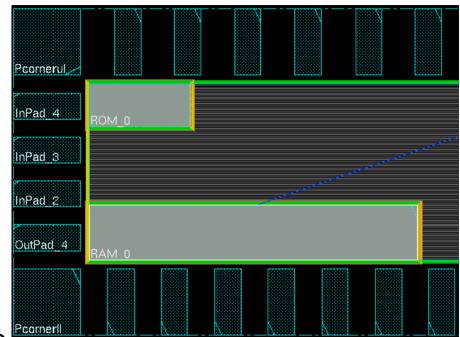
• For the upper memory no extra power routes are necessary for the top and left sides.

| | | | Add Ri | ngs | | | |
|----------------|-----------------------------|----------------|-----------|------------|------------|------|--|
| Basic A | dvanced v | a Generation | | | | | |
| | | | | | | | |
| C Set Cu | tom Ring Sid | es and Exten | sion — | | | | |
| | | | | | | | |
| | e rectangular i | | pacing th | reshold: 0 |).4 | | |
| Minimum | jog distance: | 0.4 | | | | | |
| Snap wire | e center to rout | ting grid: Nor | ie | | - ± | | |
| | vire group terleaving | | | | | | |
| | | | | | | | |
| Num | er of bits: 0 | | | | | | |
| Numi | einforcement s | | 1. D | | | | |
| Numi R S | einforcement s pacing: 0 | Wid | | | | | |
| Numi R S | einforcement s | Wid | | | | | |
| Numi R S | einforcement s pacing: 0 | Wid | | | | | |

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- If successfull the design should look like the picture.
- If not, type the command: "deleteAllPowerPreroutes", use Tab key to autocomplete.
- This command clears all power routing.



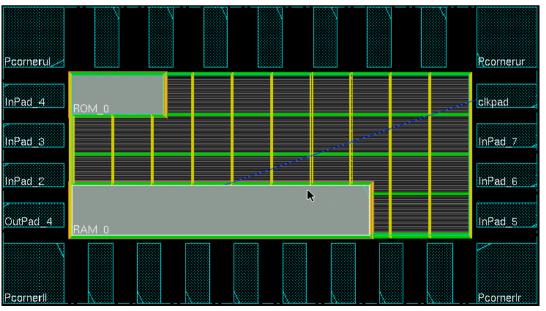
| ¥ | eit-oae@ylva:~/test/soc | * |
|---|------------------------------|---|
| <u>F</u> ile <u>E</u> dit <u>V</u> iew <u>T</u> erminal | Ta <u>b</u> s <u>H</u> elp | |
| deleteFP0bject | deleteSdp0bject | • |
| deleteFiller | deleteSelectedFromFPlan | |
| deleteHaloFromBlock | deleteShield | |
| deleteInst | deleteSpareModule | |
| deleteInstFromInstGroup | deleteTSV | |
| deleteInstGroup | deleteTieHiLo | |
| deleteInstPad | deleteWhatIfTimingAssertions | |
| deleteIoFiller | delete_path_category | |
| deleteIoInstance | | |
| deleteIoRowFiller | | |
| velocity 3> deleteAll | | |
| deleteAllCellPad | deleteAllPtnCuts | |
| deleteAllDensityAreas | deleteAllPtnFeedthroughs | |
| deleteAllFP0bjects | deleteAllRouteBlks | |
| deleteAllInstGroups | deleteAllScanCells | |
| deleteAllMsConstraints | deleteAllSignalPreroutes | |
| deleteAllPartitions | | 1 |
| deleteAllPowerPreroutes | ъ. П | 1 |
| velocity 3> deleteAllPow | erreroutes [] | * |
| | | |

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Power stripes

- Power -> Power Planning -> Add Stripes
- Select metal4 for vertical and metal3 for horizontal



| asic Adva | nced Via Generation |
|--|--|
| - Set Config | uration |
| Net(s): | GND VCC |
| Layer: | metal4 🛁 |
| | ◆ Vertical 🕹 Horizontal |
| Width: | 2 |
| Spacing: | 2 Update |
| Set Patter | n, |
| ♦ Set-to-s | et distance: 100 |
| 🔶 Number | of sets: 1 |
| 🔶 Bumps | ◆ Over 💊 Between |
| 🔶 Over P/ | G pins Pin layer: Top pin layer 🛁 🔟 Max pin width: 0 |
| 🔶 Mas | er name: 🔤 🕹 Selected blocks 🕹 All blocks |
| ◇ Design I ◇ Each se ◇ All doma ◇ Specify | √ Inner Outer boundary Create pins lected block/domain/tence ins rectangular area rectlinear area |
| First/Last | Stripe |
| | : ◆ left ↓ right from core or selected area. |
| Relative X from I | |
| Absolute | |
| 0 | |
| Option Se | |
| Use optio | m set: Update Basic |
| | |
| ок | Variables Apply Defaults Cancel Help |
| 21 | Telanto Cancel Dela |



Place well taps

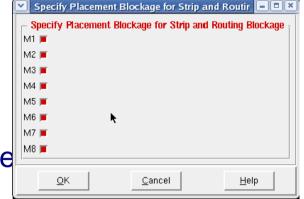
- Place -> Physical Cell -> Add well Tap
- Adds contacts for well and substrate.
- Use cell FILLER4ELD
- Use a spacing of 25µm.
- Prefix WELLTAP

| 🔳 Add Well Tap Instances (on khalid.fransg) 💷 🛪 | : |
|---|---|
| Cell Name FILLER4ELD Select |) |
| Distance interval between Cells along Row 25 |] |
| Offset from Start of Row for First Cell in Row 0.0 |] |
| Number of Site Rows to Skip for Next Row of Cells 0 |] |
| Row Number to Start Adding Cells 1 | 1 |
| Prefix WELLTAP | 1 |
| Power Domain: | |
| Fill Area Draw | |
| lix liy | 1 |
| urx ury | |
| OK <u>Apply</u> <u>Cancel</u> <u>H</u> elp | |

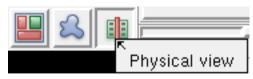




Place -> Specify -> Placement Blockage



- Place -> Place Standard cells
- Change from "Floorplan view" to "Physical view" to see placed cells:



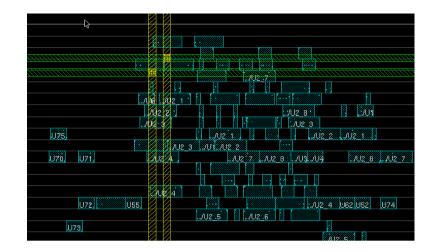
| | | Pla | <u>se</u> | | |
|---------------|-----------------|-------------------|---------------|------------------|----------------|
| 🔶 Run Ful | Placement 🗸 | Run Incremental I | Placement 🔶 F | lun Placement In | Floorplan Mode |
| - Optimizatio | n Antions | | | | |
| | Pre-Place Optin | nization | | | |
| | | | | | |
| Include I | n-Place Optimi: | zation | | | |
| Number of Thr | ead(s): 1 | Set Multiple CPU | | | |
| ок | Apply | Mode | Default | Cancel | Help |

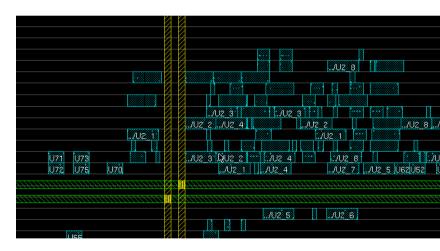


28

Place standard cells

- Zoom in close to a crossing of two metal stripes in the middle of the die.
- Hide signal wires by expanding "Net" in the right hand control "Layer Control" and untick "Net".
- You should see that no cells are placed underneath metal stripes.
- Like in the lower figure.
- Now show the nets again.





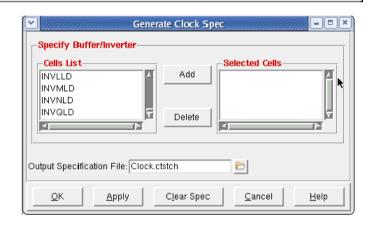


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Design Clock

- Clock -> Synthesize Clock
- Click on Gen Spec and add all cells
- Second time use the (...) button to open your .CTSTCH file.

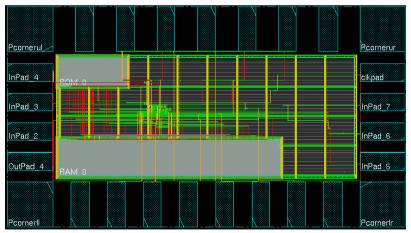
| Basic Advanced | \ |
|---|--------------|
| Clock Specification Files: Results Directory: Clock_report | Gen Spec |
| | |
| | |



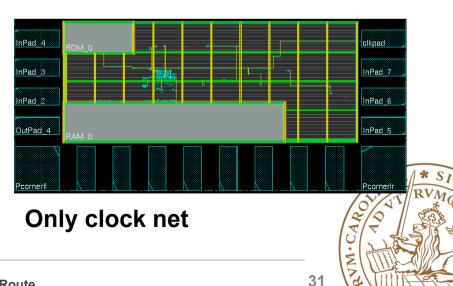


Design Clock

- Now the synthesized clock with clock buffers and including a trial route of the remaining signals nets is shown.
- Type "deleteTrialRoute" to delete the trial route and only show the clock net.

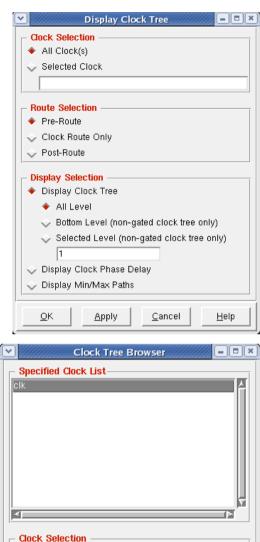


With trial Route



Design Clock

- It is possible to highlight the clock tree: Clock -> Display -> Display Clock Tree...
- Choose all clocks and All Level
- Clear it with Clock -> Display -> Clear Clock Tree Display.
- To see which buffers and inverters are used in the clock tree, use the clock tree Browser: Clock -> Browse Clock Tree



Select

<u>H</u>elp

Clock: clk

<u>o</u>k

Route Selection —
 ♦ Pre-Route
 ♦ Clock Route Only
 ♦ Post-Route

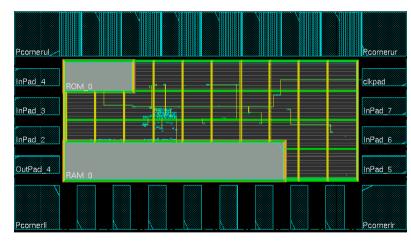
Apply

32

Cancel

IO Filler cells

- Before placeing IO-fillers the pads need to be aligned on a 0.4µm x 0.4µm grid. As the width of minimum filler is 0.4µm.
- Select all pads in the top row except the right corner pad.
- Floorplan -> Edit Floorplan -> Space
- Enter a spacing value similar to the current spacing (Use ruler "k" to measure).
- Choose "Horizontal Spacing" and "Fix Left". For Right and Left side use "Vertical spacing".
- Verify with ruler that distance is a multiple of 0.4µm.





IO Filler cells

 Place -> Physical Cells -> Add I/O Filler

I/O Filler cells:

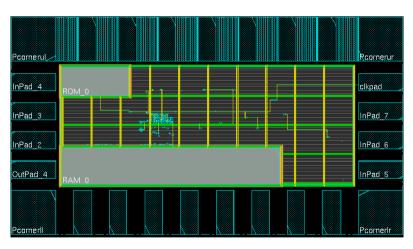
- Use IOFILLER<1, 2, 4, 8, 16, 32, 64>_ST_SF_LIN

Filler cells:

– Use FILLERPFOP<8, 9, 12, 16, 32, 64> – And HS65_L(H|S|L)_FILLERPFP<1-4>

- Prefix: IO_FILLER
- Select which side to add to: Top/Bottom/Right/Left.
- The screen does not auto-refresh (press "f").
- Add to all sides.

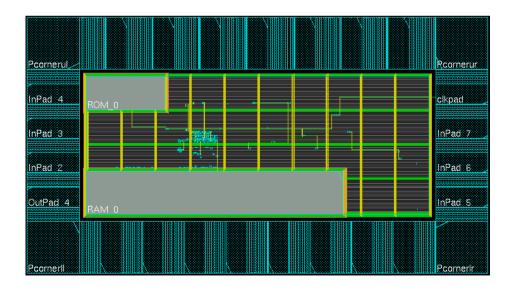
| | Add IO Fi | ller | //// = = × |
|-----------------|---------------|----------------|--------------|
| Cell Name: EN | 1PTY16LB EMPT | Y8LB EMPTY4 | LB EMPTY2LE |
| Prefix: IO_FILL | ER | | |
| The Row Num | per: | | |
| Side Top 🗕 | 4 | | |
| 🔲 Fill Any G | ap | | |
| 🔲 Use Small | lo Height | | |
| 🔲 Fill Area | Draw | | |
| | | | lly |
| | urx | | iry |
| <u>o</u> k | Apply | <u>C</u> ancel | <u>H</u> elp |





IO Filler cells

• If successfull design should look as in picture.





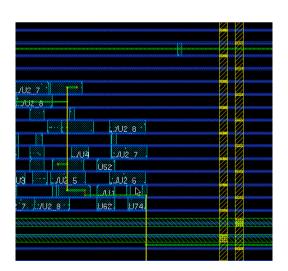
HIVM CANNOL AND CANNOL

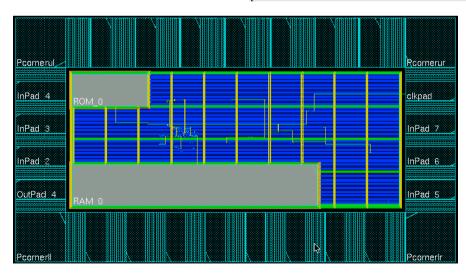
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Special Route

- Route -> Spceial Route
- Routes GND and VDD net for powering of standard cells.

| (s): GND VCC | <u>.</u> |
|--|---|
| ite | |
| | Pins ■ Pad Rings ■ Standard Cell Pins ■ Stripes (unconnected) |
| | |
| iting Control ——— yer Change Control – | |
| p Layer: metal8 🛁 | Bottom Layer: metal1 🔜 |
| Allow Jogging | Allow Layer Change |
| | |
| j Area | |
| X1: | V1: Draw |
| X2: | Y2: |
| Connect to Targ | et Inside The Area Only |
| | |
| 」Delete Existing Route 」Generate Progress № | |
| Extra Config File: | |







Route normal nets

- Route -> Nanoroute -> Route
- Run with default options.

| | | | Nanc | oRoute | | | |
|------|--|-------------------------------|---------------|-----------------|---------|-----------------|-------|
| Rou | iting Phase | | | | | | |
| | Global Route | | | | | | |
| | Detail Route | Start Iteration | 0 | End Iteration | default | | |
| Post | Route Optimization 🔲 | Optimize Via 🔲 | Optimize Wire | | | | |
| Con | current Routing Featu | ires | | | | | |
| | Fix Antenna | 🔲 Insert Dio | des | Diode Cell Name | | _ | |
| | | | Congestion | Timing | , | | |
| | Timing Driven | Effort 5 | | | | S.M.A.R.T. | |
| | SI Driven | | | | | | |
| | Post Route SI | SI Victim File | | | | | |
| | Litho Driven | , | | | | _ | |
| | Post Route Litho Repa | dr | | | | | |
| | i <mark>ting Control</mark> Selected Nets Only ECO Route | Bottom Layer | default | Top Layer | default | | |
| | Area Route | Area | | | è | Select Area and | Route |
| Job | Control | | | | | | |
| | Auto Stop | | | | | | |
| lumb | ber of Thread(s) For Mu | ultiple Threaded: 1 | | | | | |
| N | lumber of Thread(s) For | ^r Superthreaded: 1 | | | | | |
| | Number of Hest(s) For | r Superthreaded: 0 |) | | | | |
| | Set Multiple CPU | | | | | | |
| | OK Apply | Attribute | Mode | Save | Load | Cancel | Help |

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Analyze Timing

- Before adding fillers we need to make sure that we meet timing, both setup and hold.
- Timing -> Report Timing
- Choose which design stage we are in, at this point Post-Route.
- Select both Setup and Hold, one after each other.

| ⊻] | Timing Analysis |
|----|---|
| | Basic Advanced |
| | Use Existing Extraction and Timing Data |
| | <mark>Design Stage</mark> ◇ Pre-Place ◇ Pre-CTS ◇ Post-CTS ◆ Post-Route ◇ Sign-Off |
| | Analysis Type |
| | ◆ Setup → Hold |
| | - Reporting Options |
| | Number of Paths: 50 |
| | Report file(s) Prefix: MEDIANFILTER_N8_pos |
| | Output Directory: timingReports |
| | |
| | QK <u>Apply</u> <u>Cancel Help</u> |



Analyze Timing cont'd

- Make sure that we have no setup nor hold violations.
- WNS stands for Worst Negative Slack
- TNS stands for Total Negative Slack.
- If we do we need to run optimize timing, to solve this issue.

| optDesign | Final | Summary |
|-----------|-------|---------|
| | | |

| Setup mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
|---|------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------------|
| WNS (ns): TNS (ns): Violating Paths: All Paths: | 0.000 0 | 5.242 0.000 0 75 | 15.707 0.000 0 8 | N/A N/A N/A N/A | N/A N/A N/A N/A | N/A N/A N/A N/A |
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | + clkgate |
| +WNS (ns): | -0.019 | -0.019 | 0.074 | N/A | N/A | + N/A |



Fix Timing Violations

- Optimize -> Optimize Design
- Select your design stage, Post-Route.
- Select which violation you which to fix, such as Hold.
- Make sure to fix Max Cap,¹
 Max Tran and Max Fanout as well.
- TIP: Do not run all things at once.

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|-------------------------------------|-------------|-----------------|
|-------------------------------------|-------------|-----------------|

| | Optimization | | |
|---------------------|-----------------|--------------------------------|--------------|
| -Design Stage | | | |
| 🔷 Pre-CTS | 🔷 Post-CTS | Post-Route | |
| -Optimization Type- | | | |
| 👅 Setup | | Hold | |
| 🔷 Incremental | | | |
| 🔶 Design Rules Vio | lations | | |
| 📕 Max Cap | | | |
| 📕 Max Tran | | | |
| 🔲 Max Fanout | | | |
| Include SI SI O | ptions | | |
| | | | |
| | ly <u>M</u> ode | <u>D</u> efault <u>C</u> lose | <u>H</u> elp |
| <u> </u> | | | |



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Fix Timing Violations cont'd

- Make sure that all violations are fixed.
- If not re-run optimize timing, and select the method to fix.
- If running only setup time make sure to run analyze timing for hold violations afterwards.

| optDesign Final S | ummarv | | | | | | |
|---|--|---|--|--|--|---|---|
| | | | | | | | |
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | + clkgate | + |
| WNS (ns): TNS (ns): | | 5.049 0.000 | 15.699 0.000 | N/A N/A | N/A N/A | N/A N/A | + |
| Violating Paths: All Paths: | | 0 | | N/A N/A | N/A N/A | N/A N/A | |
| + | + | + | ·+ | + + | ·+ | + | + |
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | clkgate | |
| WNS (ns): TNS (ns): Violating Paths: All Paths: | 0.000 | 0.008 0.000 0 | 0.077 0.000 0 8 | N/A N/A N/A N/A | N/A N/A N/A N/A | N/A N/A N/A N/A | |
| - | Setup mode Setup mode WNS (ns): TNS (ns): Violating Paths: All Paths: Hold mode WNS (ns): TNS (ns): | WNS (ns): 5.049 TNS (ns): 0.000 Violating Paths: 0 All Paths: 83 Hold mode all WNS (ns): 0.008 TNS (ns): 0.000 Violating Paths: 0 | Setup mode all reg2reg WNS (ns): 5.049 5.049 TNS (ns): 0.000 0.000 Violating Paths: 0 0 All Paths: 83 75 Hold mode all reg2reg WNS (ns): 0.008 0.008 TNS (ns): 0.000 0.000 | Setup mode all reg2reg in2reg WNS (ns): 5.049 5.049 15.699 TNS (ns): 0.000 0.000 0.000 Violating Paths: 0 0 0 All Paths: 83 75 8 Hold mode all reg2reg in2reg WNS (ns): 0.008 0.077 TNS (ns): 0.000 0.000 Violating Paths: 0 0 | Setup mode all reg2reg in2reg reg2out WNS (ns): 5.049 5.049 15.699 N/A TNS (ns): 0.000 0.000 0.000 N/A Violating Paths: 0 0 0 N/A All Paths: 83 75 8 N/A Hold mode all reg2reg in2reg reg2out WNS (ns): 0.008 0.0077 N/A N/A WNS (ns): 0.000 0.000 0.000 N/A WNS (ns): 0.000 0.000 N/A N/A | Setup mode all reg2reg in2reg reg2out in2out WNS (ns): 5.049 5.049 15.699 N/A N/A TNS (ns): 0.000 0.000 0.000 N/A N/A Violating Paths: 0 0 0 N/A N/A Hold mode all reg2reg in2reg reg2out in2out WNS (ns): 0.008 0.077 N/A N/A WNS (ns): 0.000 0.000 N/A N/A Violating Paths: 0 0 0.077 N/A N/A WNS (ns): 0.000 0.000 N/A N/A WNS (ns): 0.000 0.000 N/A N/A WNS (ns): 0.000 0.000 N/A N/A | Setup mode all reg2reg in2reg reg2out in2out clkgate WNS (ns): 5.049 5.049 15.699 N/A N/A N/A WNS (ns): 0.000 0.000 N/A N/A N/A Violating Paths: 0 0 0 N/A N/A N/A Hold mode all reg2reg in2reg reg2out in2out clkgate WNS (ns): 0.008 0.007 N/A N/A N/A WNS (ns): 0.000 0.008 0.077 N/A N/A N/A WNS (ns): 0.000 0.000 N/A N/A N/A Violating Paths: 0 0 0 N/A N/A |



Fix Timing Violations cont'd

- If no reg2out, in2reg paths are found, input delay and/ or output delay are missing.
- See synthesis slides.

| d/ | | | | | | | |
|----------------------|--|------------|---------------------------------|---------------------------|--------------------------------|---------------------------------|--|
| | optDesign Final S | Summary | | | | | |
| + | Setup mode | all | + reg2reg | in2reg | reg2out | + in2out | ++ clkgate |
| + | ۲۰۰۰ WNS (ns): TNS (ns): Violating Paths: All Paths: | 0.000 0 | 5.049 0.000 0 75 | 15.699 0.000 0 8 | N/A N/A N/A N/A | N/A N/A N/A N/A N/A | ++ N/A N/A N/A N/A |
| + | Hold mode | all | + reg2reg | in2reg | reg2out | in2out | ++ clkgate |
| + | WNS (ns): TNS (ns): Violating Paths: All Paths: | 0.000 0 | 0.008 0.000 0 75 | 0.077 0.000 0 8 | N/A N/A N/A N/A | N/A N/A N/A N/A | N/A N/A N/A N/A |



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Another note on Timing Violations

- If timing violations are still seen after multiple runs with a larger design, what to do?
- Run Optimize Timing after each design stage, i.e.
 - After placement (before Clock Tree Synthesis) Pre-CTS
 - After Clock Tree Synthesis Post-CTS
 - After Routing Post-Route
- Try using incremental optimization for hold after the setup optimization.
- Reduce clock speed.
- Increase die size, i.e., have a lower die utilization.

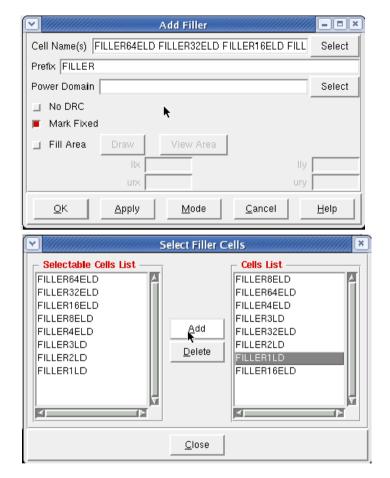




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Add Filler cells

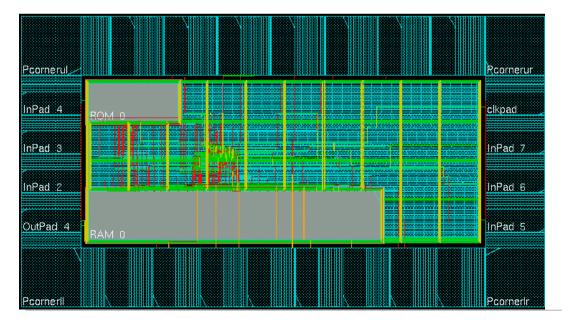
- Place -> Physical Cells -> Add Filler.
- Be sure to select the largest fillers first to use them when possible





Add Filler cells

 Final design should look as in picture if Metal 1 is set to not visible in the drawer in the right hand side of Encounter.



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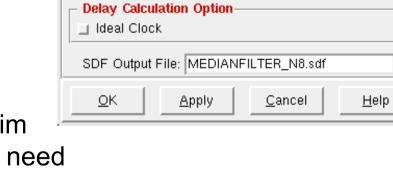
45

Export Netlist and SDF

- To simulate your design in Modelsim with correct timing annotation, you need to export a netlist (your design) and SDF (Synopsys Delay Format, timing annotation).
- Timing -> Write SDF
- Be sure to untick Ideal Clock
- This dialog runs the "write_sdf" command in the background. However, to avoid errors in ModelSim, use this "write_sdf" command in your script:

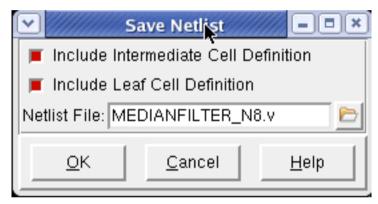
write_sdf -version 2.1 -interconn nooutport file.sdf

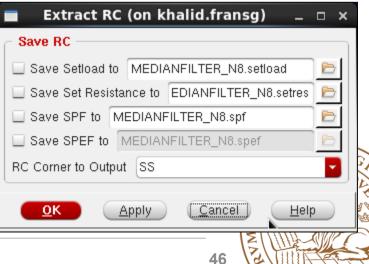
- File -> Save -> Netlist
- It is also possible to save SPF, SPEF for further use in Power and Timing analysis.
- Timing -> Extract RC (Chose which RC corner to output.)



Calculate Delay

- 0





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Save Design and Restore Design

- To save and restore your design use:
- Save
 - File -> Save Design
- Restore
 - Design -> Restore Design



Re-run entire placement

- When developing a chip, placement might be run many times and each indiviual step may take a long time, and a few hours is not uncommon.
- To avoid waiting for each step to finish running a script is easier.
- Enounter saves all commands entered in a file called encounter.cmd with an added digit for every run, i.e. encounter.cmd23 if you you are running for the 23rd time in the same directory.
- **IMPORTANT!** Don't re-run this file directly as it contains every single change performed, including zooming in and out.
- Copy the file and remove unnecessary commands, e.g., zoom, fit.
- Type **source filename.cmd** to execute an encounter script.

