Handin Exercise 1, Low Noise Amplifiers

This exercise deals with low noise amplifiers (LNAs) and is a preparation for lab 1. A differential LNA as shown in fig. 12.10 (page 388) in the textbook is to be designed. The I_{BIAS} current source is, however, to be omitted. You will need to refer to the data sheet of the 130nm CMOS process. The following requirements and information are provided:

- Supply voltage (V_{DD}) = 1.2V
- Operating frequency = 2.1GHz
- Input impedance = 50 Ω at each side (100 Ω differentially)
- Bias current = 5mA
- Voltage gain = 30
- All transistors should be 0.4um long

1. Give two disadvantages with a differential topology compared to a single-ended one.
2. Calculate optimum width of the input transistors for minimum noise with limited power consumption.
3. Calculate overdrive voltage, transconductance and gate-source capacitance of the input transistors.
4. Calculate L_s so that the resistive part of the differential input impedance becomes 100 Ω.
5. Calculate L_g so that the differential input impedance becomes resistive at 2.1GHz. If this inductor is implemented on chip with Q=8, how much noise would this inductor contribute compared to the noise of the generator.
6. Calculate bias voltages V_{G1} (input devices) and V_{G2} (cascode devices) to keep the input device from reaching the triode region with a 200mV margin. In other words, the drain voltage should be 200mV above pinch-off. Note that this is slightly different from the figure in the textbook, where $V_{G2} = V_{DD}$. Furthermore, disregard bulk effects and assume that the cascode has the same dimensions as the input device. Observe that no tail current source is to be used.
7. Calculate the approximate capacitance presented to each output node by the cascode devices. Include both drain-gate and drain-bulk. Assume zero reverse bias, although the node is biased at V_{DD}. Assume a layout with many fingers, and with a gate to gate distance (drain finger width) of 0.4um.
8. Assume that the inductors of the output resonance circuit can each have a value of up to 10nH and a Q up to 5. Additional resistance and capacitance can be put in parallel to tune the resonance frequency and gain. Design the RLC circuit for maximum bandwidth and a peak voltage gain of 30 (from amplifier input to output) at 2.1GHz.