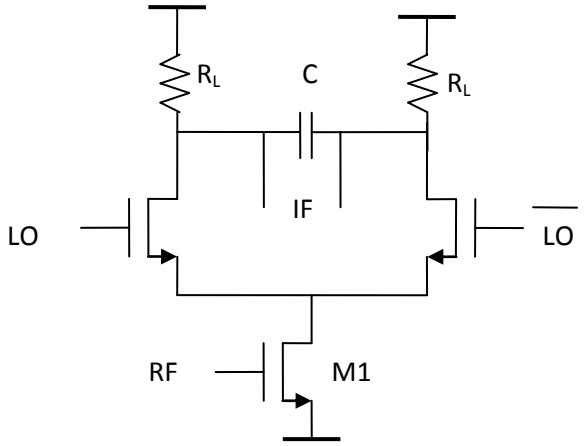
Problems for exercise 7 (Mixers)

1. A single balanced active mixer for a Bluetooth low-IF receiver is to be designed according to the figure below:



Vdd=1.2V
Idc=2mA
f_{LO}=2.4GHz
IF=3MHz
V_{LO}=0.5V_{pp}/side
Use 130-nm CMOS datasheet

   a. Assume for a start that no parasitic capacitances exist and that the switches are ideal. Determine parameters and operating points for M1, RL and C so that G_{cv}=8dB, the bandwidth at the output exceeds 10MHz, the LO leakage to the IF port is less than 5mV_{pp} per side, and the output voltage can be up to 0.6V_{pp} per side. The switches are assumed ideal as long as the output nodes are at least 0.6V above ground, than they enter the triode region.
   Which will have largest influence on the compression point in this case, the non-linearities at the input or the output?

   b. Calculate the dimensions of the switch transistors so that V_{ov}=0.15V in the switching instant (V_{LO}=0). If there is a 10% mismatch in c_{gs} between the switch transistors, how large will the LO to RF leakage be? The impedance at the RF port is 500Ω. C_{gs1} is assumed to be in resonance with an inductor and can therefore be neglected. Make necessary simplifying assumptions.

2. A mixer for an X-band heterodyne receiver is to be designed in 130-nm CMOS. The IF is in this case high, so a double-balanced (active) mixer is used to minimize the LO to IF feedthrough and thereby simplify the output filtering. Inductors with L=4nH and Q=6 at IF are used as loads. Capacitors are put in parallel to make the load resonate at IF.

   Given: f_{RF}=10GHz, f_{LO}=13GHz, V_{LO}=0.6V_{pp}/side, G_{cv}=10dB, Vdd=1.2V, $V_{in,max}$=400mV_{pp}/side

   Assume the switches to be ideal except that they enter the triode region when the output voltage is 0.5V above ground potential.
   Determine the dimensions of the input transistors
   Design the switch transistors so that they conduct simultaneously for less than 20% of the time.

   Hint:
   The switches are on simultaneously when the differential LO magnitude is less than V_{ov}*sqrt(2). Picture the LO signal as a sinusoid, with LO voltage on the y-axis and degrees on the x-axis. At which angle ϕ must the transistors stop conduct to fulfill the 20% requirement? With ϕ known, an equation can then be formulated to calculate V_{ov}:
   $V_{ov}=V_{LOpk(diff)}$*sin(ϕ)/sqrt(2)

3. A mixer for a direct conversion receiver for WCDMA is to be designed in 130-nm CMOS. Because of its low 1/f noise a passive mixer is chosen. The load is a 500fF capacitance.
   Given: $f_{RF}=f_{LO}$= 2.14GHz, G_{cv}>-5dB, V_{LO}=1.2V_{pp}/side square wave, F<10dB, BW>20MHz

   Solved by the teacher.

4. Problem 13.5a & 13.6 (passive mixer with resistive load)

   Hint: in 13.6c use the equation: $P=CV^2f$
   (if inductors are used to tune out the capacitances, P can be Q times smaller)