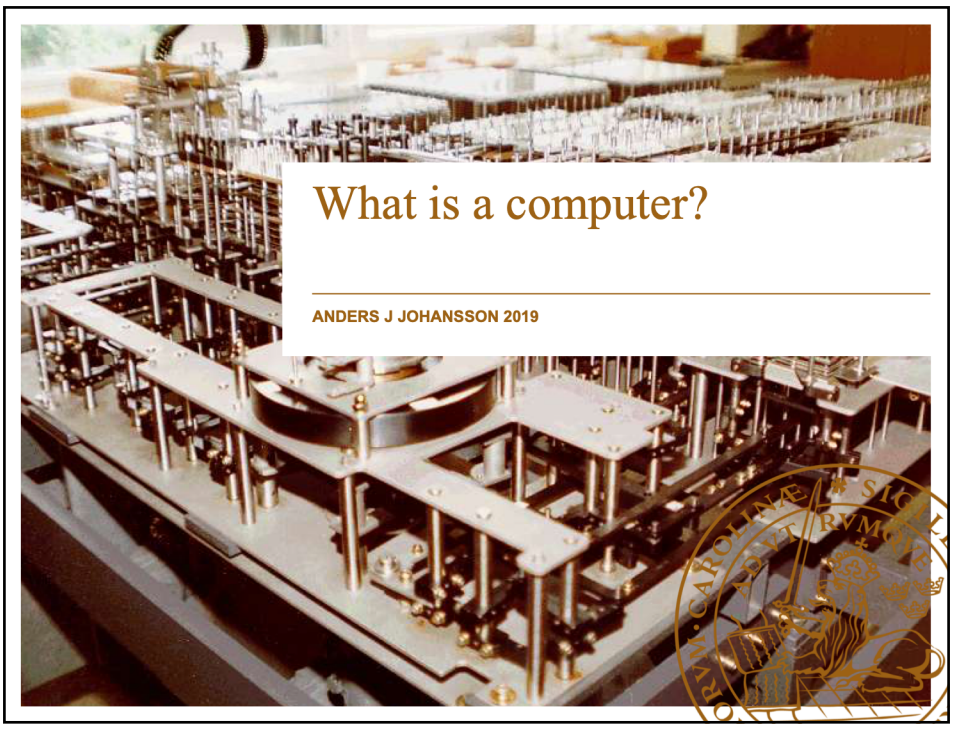

What is a computer?

ANDERS J JOHANSSON 2019

What was a computer?

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Annie Easley, human computer, NASA 1955

Later FORTRAN programmer, such as code for the Centaur rocket which delivered Cassini to space.

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Photo: www.nasa.gov

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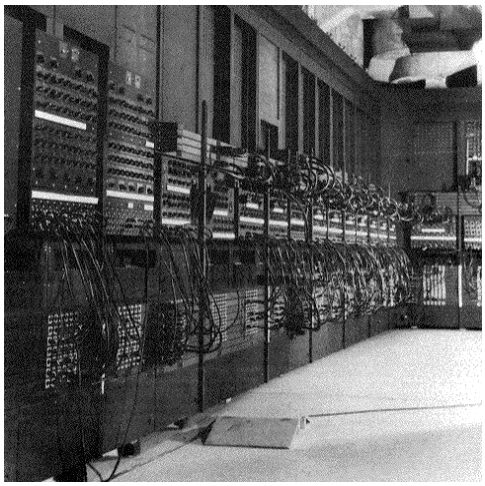
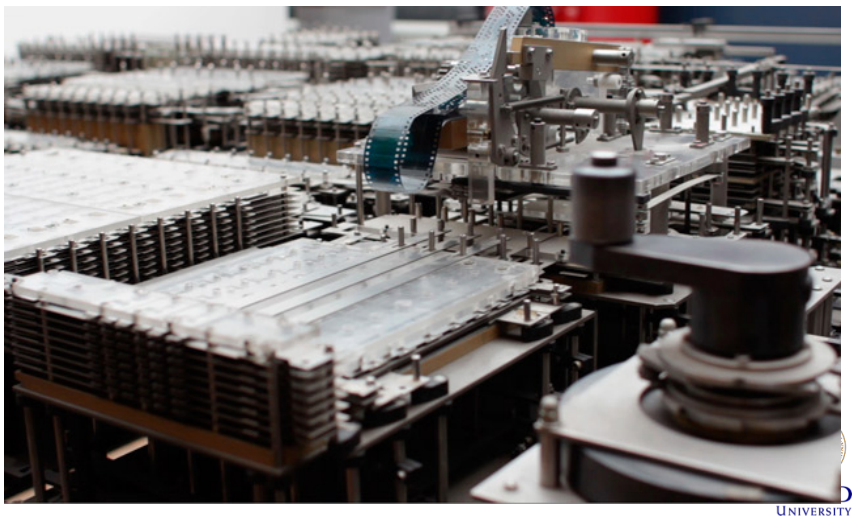
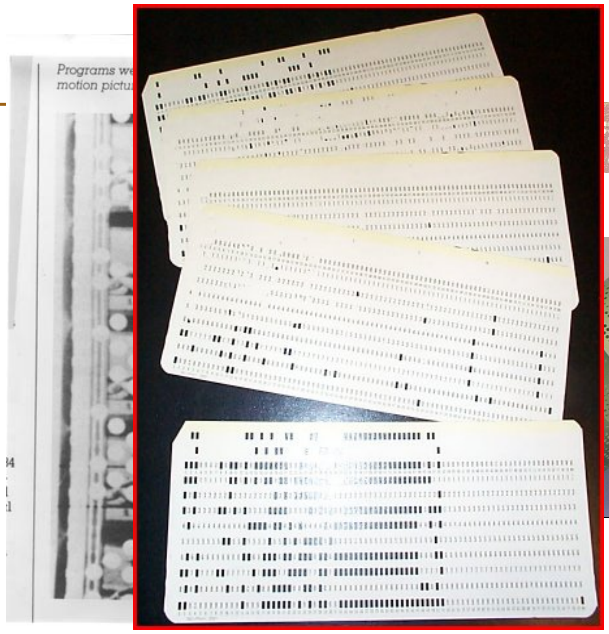
Which one is the first computer machine?

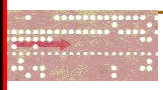


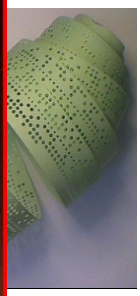
ENIAC

Z1 Replica









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Jacquardloom (1801)

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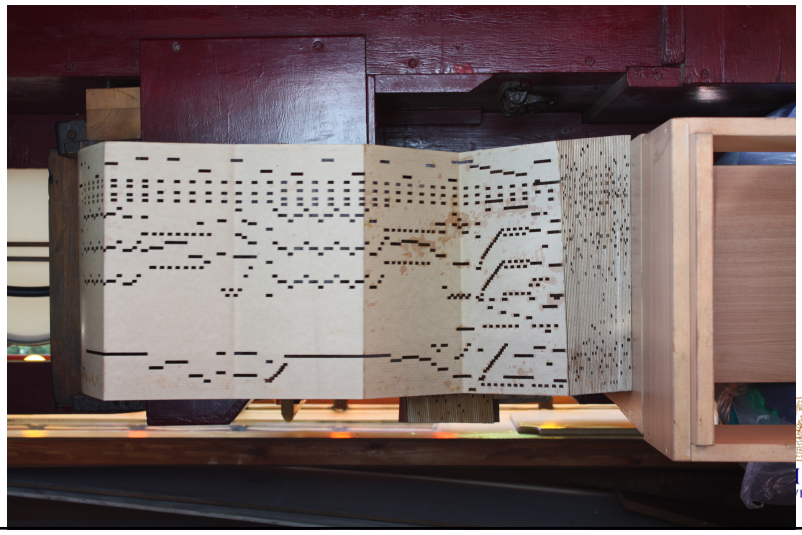
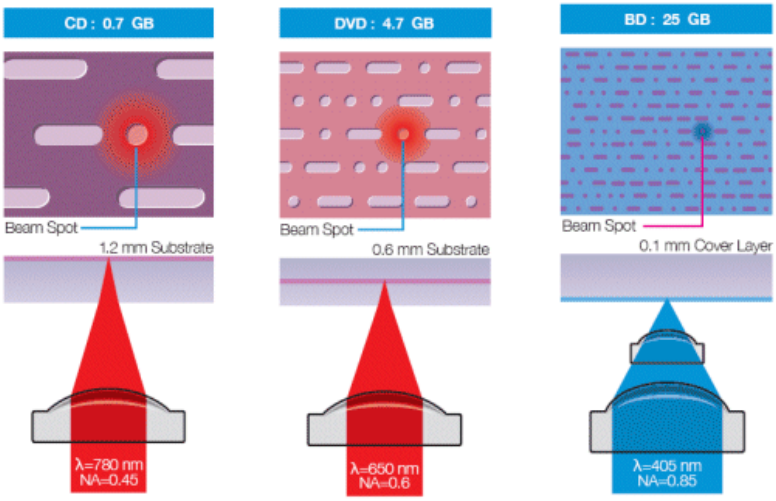
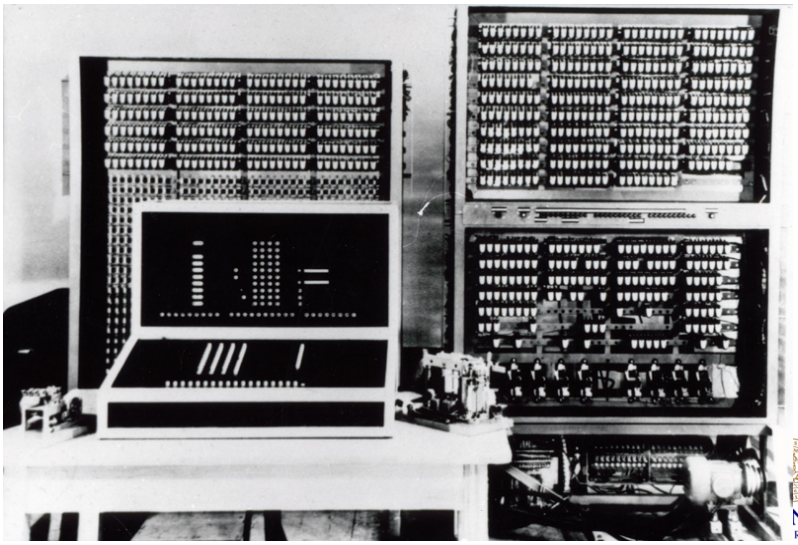
Automatic music



Today: still holes in plates!



Z3



Plankalkül

```
P1 max3 (V0[:8.1],V1[:8.2],V2[:8.1]) => R0[:8.1]
max(V0[:8.5],V1[:8.4]) => Z1[:8.3]
max(Z1[:8.6],V2[:8.2]) => R0[:8.2]
END
P2 max (V0[:8.6],V1[:8.3]) => R0[:8.1
V0[:8.0] => Z1[:8.4]
(Z1[:8.0] < V1[:8.3]) -> V1[:8.2] => Z1
Z1[:8.3] => R0[:8.2]
END
```

Number of Operation	Nature of Operation	Variables acted upon	Variables receiving results	Indication of change in the value on any Variable	Statement of Results	Data								
						${}^1V_1$	${}^1V_2$	${}^1V_3$	${}^0V_4$	${}^0V_5$	${}^0V_6$	${}^0V_7$	${}^0V_8$	${}^0V_9$
						○	○	○	○	○	○	○	○	○
						0	0	0	0	0	0	0	0	0
						0	0	0	0	0	0	0	0	0
						1	2	4	0	0	0	0	0	0
						1	2	n						
1	$\times$	${}^1V_2 \times {}^1V_3$	${}^1V_4, {}^1V_5, {}^1V_6$	${}^1V_2 = {}^1V_2$, ${}^1V_3 = {}^1V_3$	$= 2n$	.....	2	n	$2n$	$2n$	$2n$			
2	$-$	${}^1V_4 - {}^1V_1$	${}^2V_4$	${}^1V_4 = {}^2V_4$, ${}^1V_1 = {}^1V_1$	$= 2n - 1$	1	.....	.....	$2n - 1$					
3	$+$	${}^1V_5 + {}^1V_1$	${}^2V_5$	${}^1V_5 = {}^2V_5$, ${}^1V_1 = {}^1V_1$	$= 2n + 1$	1	.....	.....	.....	$2n + 1$				
4	$\div$	${}^2V_5 \div {}^2V_4$	${}^1V_{11}$	${}^2V_5 = {}^0V_5$, ${}^2V_4 = {}^0V_4$	$= \frac{2n-1}{2n+1}$	.....	.....	.....	0	0	.....	.....	.....	.....
5	$\div$	${}^1V_{11} \div {}^1V_2$	${}^2V_{11}$	${}^1V_{11} = {}^2V_{11}$, ${}^1V_2 = {}^1V_2$	$= \frac{1}{2} \cdot \frac{2n-1}{2n+1}$	.....	2	.....	.....	.....	.....	.....	.....	.....
6	$-$	${}^0V_{13} - {}^2V_{11}$	${}^1V_{13}$	${}^2V_{11} = {}^0V_{11}$, ${}^0V_{13} = {}^1V_{13}$	$= -\frac{1}{2} \cdot \frac{2n-1}{2n+1} = A_0$	.....	.....	.....	.....	.....	.....	.....	.....	.....
7	$-$	${}^1V_3 - {}^1V_1$	${}^1V_{10}$	${}^1V_3 = {}^1V_3$, ${}^1V_1 = {}^1V_1$	$= n - 1 (= 3)$	1	.....	n	.....	.....	.....	.....	.....	.....
8	$+$	${}^1V_2 + {}^0V_7$	${}^1V_7$	${}^1V_2 = {}^1V_2$, ${}^0V_7 = {}^1V_7$	$= 2 + 0 = 2$	.....	2	.....	.....	.....	.....	2		
9	$\div$	${}^1V_6 \div {}^1V_7$	${}^3V_{11}$	${}^1V_6 = {}^1V_6$, ${}^0V_{11} = {}^3V_{11}$	$= \frac{2n}{2} = A_1$	.....	.....	.....	.....	.....	$2n$	2	.....	.....
10	$\times$	${}^1V_{21} \times {}^3V_{11}$	${}^1V_{12}$	${}^1V_{21} = {}^1V_{21}$, ${}^3V_{11} = {}^3V_{11}$	$= B_1 \cdot \frac{2n}{2} = B_1 A_1$	.....	.....	.....	.....	.....	.....	.....	.....	.....
11	$+$	${}^1V_{12} + {}^1V_{13}$	${}^2V_{13}$	${}^1V_{12} = {}^0V_{12}$, ${}^1V_{13} = {}^2V_{13}$	$= -\frac{1}{2} \cdot \frac{2n-1}{2n+1} + B_1 \cdot \frac{2n}{2}$	.....	.....	.....	.....	.....	.....	.....	.....	.....
12	$-$	${}^1V_{10} - {}^1V_1$	${}^2V_{10}$	${}^1V_{10} = {}^2V_{10}$, ${}^1V_1 = {}^1V_1$	$= n - 2 (= 2)$	1	.....	.....	.....	.....	.....	.....	.....	.....
13	$-$	${}^1V_6 - {}^1V_1$	${}^2V_6$	${}^1V_6 = {}^2V_6$, ${}^1V_1 = {}^1V_1$	$= 2n - 1$	1	.....	.....	.....	.....	$2n - 1$			
14	$+$	${}^1V_1 + {}^1V_7$	${}^2V_7$	${}^1V_1 = {}^1V_1$, ${}^1V_7 = {}^2V_7$	$= 2 + 1 = 3$	1	.....	.....	.....	.....	.....	3		
15	$\div$	${}^2V_6 \div {}^2V_7$	${}^1V_8$	${}^2V_6 = {}^2V_6$, ${}^2V_7 = {}^2V_7$	$= \frac{2n-1}{3}$	.....	.....	.....	.....	.....	$2n - 1$	3	$\frac{2n-1}{3}$	
16	$\times$	${}^1V_8 \times {}^3V_{11}$	${}^4V_{11}$	${}^1V_8 = {}^0V_8$, ${}^3V_{11} = {}^4V_{11}$	$= \frac{2n}{2} \cdot \frac{2n-1}{3}$	.....	.....	.....	.....	.....	.....	.....	0	.....
17	$-$	${}^2V_6 - {}^1V_1$	${}^3V_6$	${}^2V_6 = {}^3V_6$, ${}^1V_1 = {}^1V_1$	$= 2n - 2$	1	.....	.....	.....	.....	$2n - 2$			

Charles Babbage

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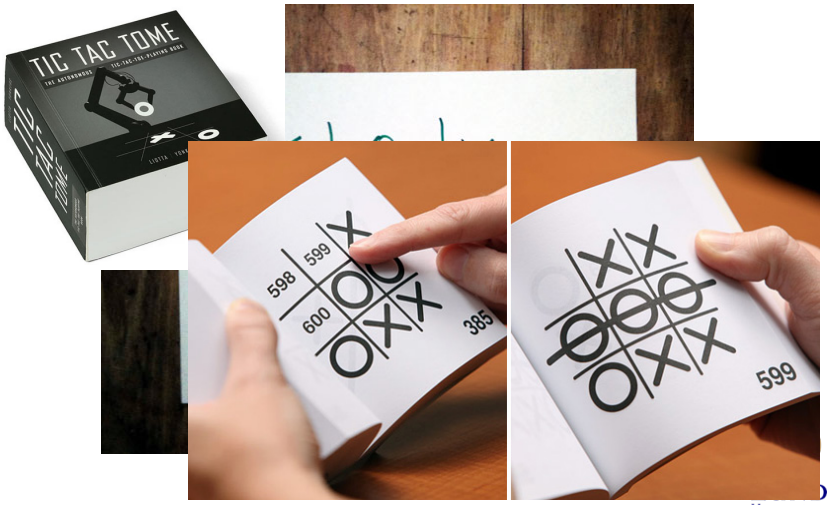
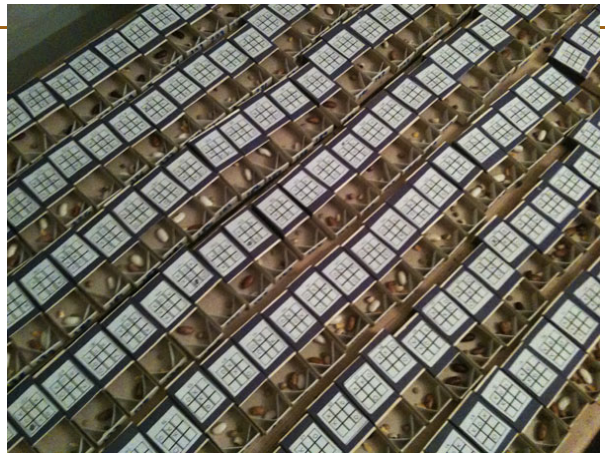
What is necessary to play a game?



What is necessary to learn a game?

Selflearning?



AI?

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Thanks to:

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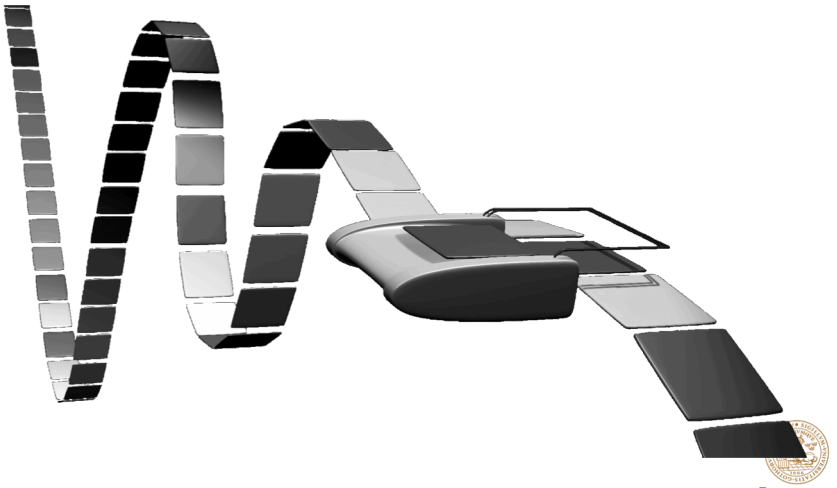
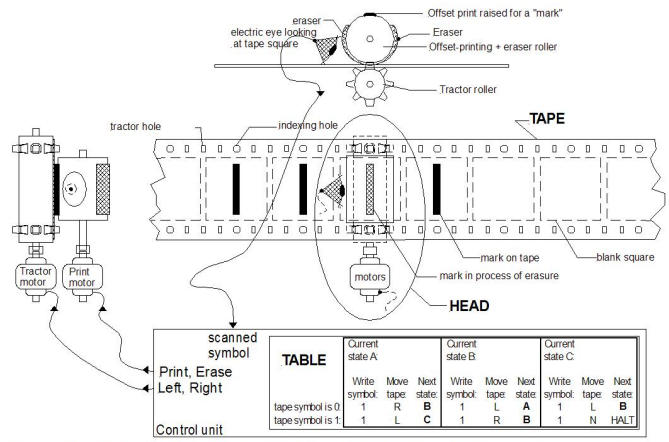
Youtube video

- standupmaths :
  - MENACE: the pile of matchboxes which can learn
- https://www.youtube.com/watch?v=R9c-_neaxeU

Turing machine

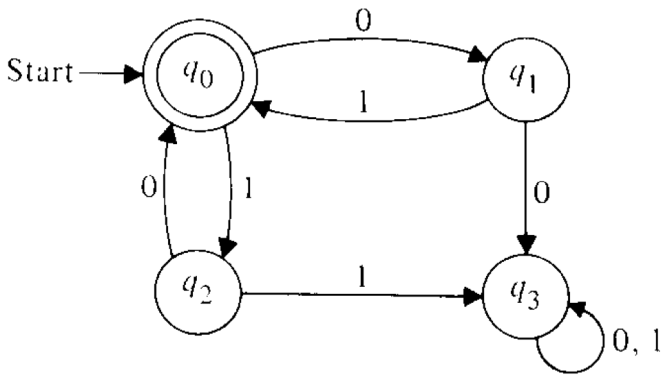


Turing machine



A fanciful mechanical Turing machine's TAPE and HEAD. The TABLE instructions might be on another "read only" tape, or perhaps on punch-cards. Usually a "finite state machine" is the model for the TABLE.

State machine



aturingmachine.com

Church-Turing Hypothese

"The evidence seems to indicate that every algorithm for any computing device has an equivalent Turing machine algorithm ."

aturingmachine.com

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Development driven by increased demands.

- Mechanics -> Electromechanics -> Valves -> discrete semiconductors (Transistors) -> Integrated circuits)
- Driving forces: Speed, reliability, weight
  - Decyphering
  - Defense industry
  - Space industry
  - Commercial applications
  - etc.

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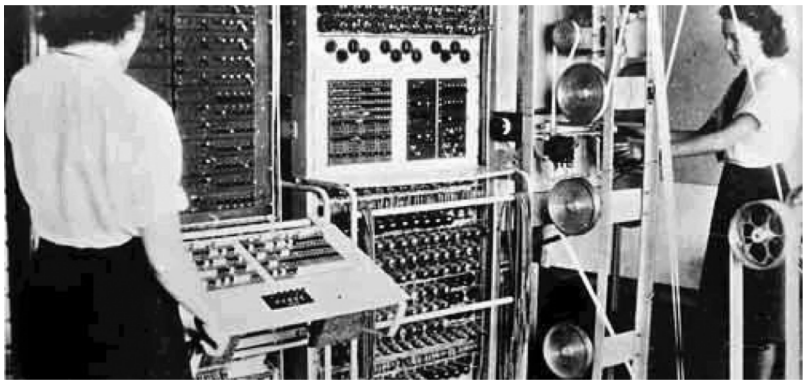
Collossus: First electronic digital programmable computer



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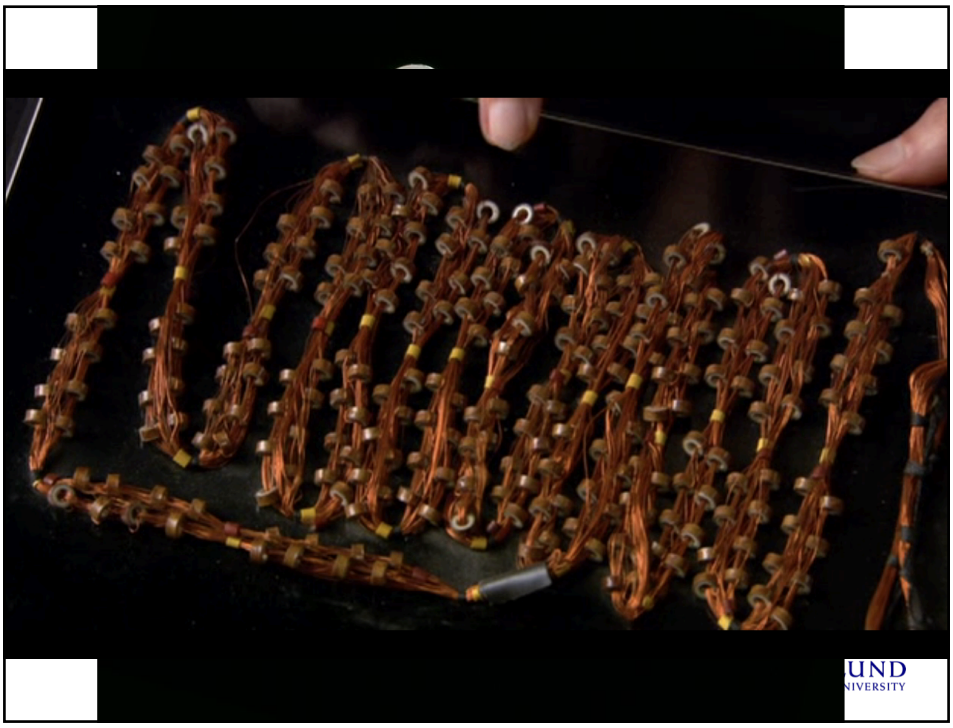
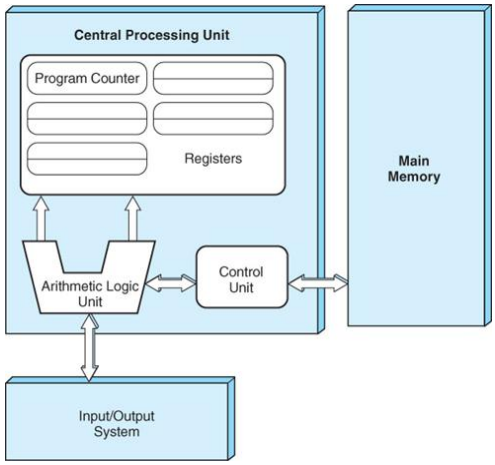
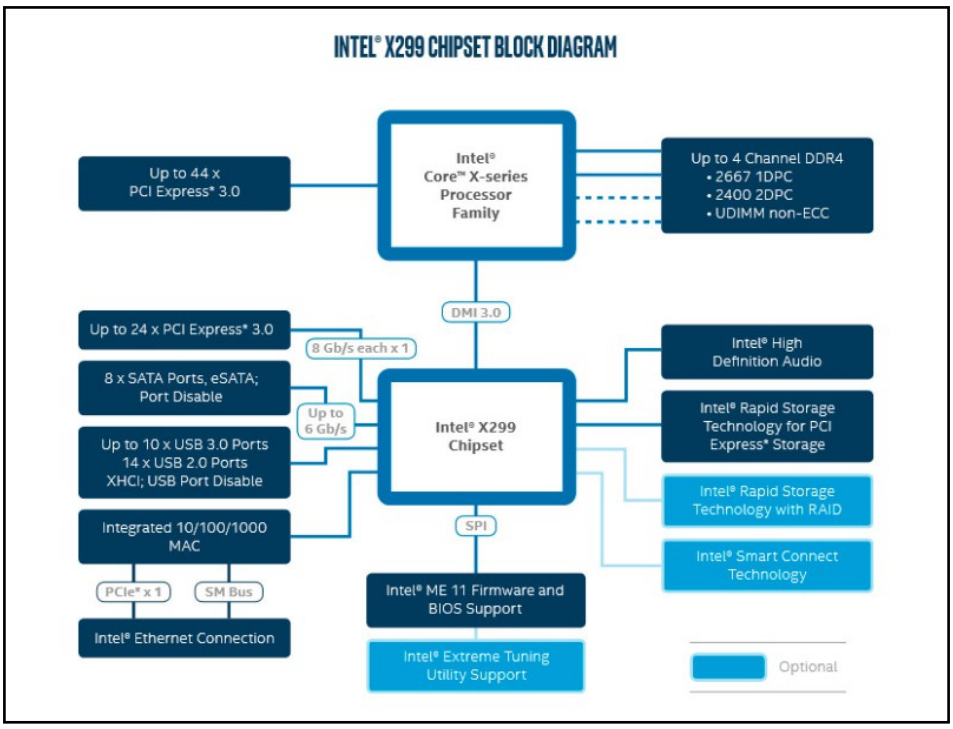
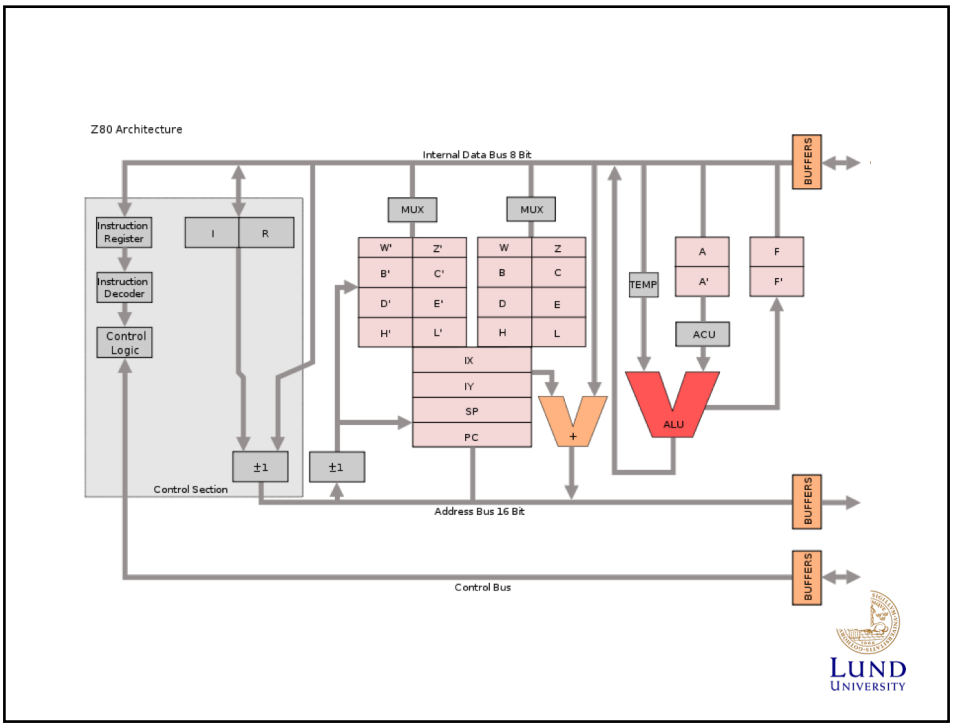


“Real” computers

von Neumann architecture




INTEL® X299 CHIPSET BLOCK DIAGRAM
Up to 44 x PCI Express* 3.0
Intel® Core™ X-series Processor Family
Up to 4 Channel DDR4
• 2667 1DPC
• 2400 2DPC
• UDIMM non-ECC
DMI 3.0
Up to 24 x PCI Express* 3.0
8 Gb/s each x 1
8 x SATA Ports, eSATA; Port Disable
Up to 6 Gb/s
Up to 10 x USB 3.0 Ports
14 x USB 2.0 Ports
XHCI; USB Port Disable
Integrated 10/100/1000 MAC
Intel® X299 Chipset
Intel® High Definition Audio
Intel® Rapid Storage Technology for PCI Express* Storage
Intel® Rapid Storage Technology with RAID
Intel® Smart Connect Technology
SPI
PCIe* x 1
SM Bus
Intel® Ethernet Connection
Intel® ME 11 Firmware and BIOS Support
Intel® Extreme Tuning Utility Support
Optional


Z80 Architecture
Internal Data Bus 8 Bit
BUFFERS
Instruction Register
Instruction Decoder
Control Logic
I
R
MUX
MUX
W'
Z'
B'
C'
D'
E'
H'
L'
W
Z
B
C
D
E
H
L
IX
IY
SP
PC
TEMP
A
A'
F
F'
ACU
ALU
±1
±1
Control Section
Address Bus 16 Bit
BUFFERS
Control Bus
BUFFERS
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ZiLOG
Z84C0010FEC
Z80 CPU
0450 C3
PAC-MAN
READY!
Nintendo GAME BOY
SELECT
START


ZiLOG
Z84C0010FEC
Z80 CPU
0450 C3
Texas Instruments TI-82
Texas Instruments TI-86
Hello Wikipedia!
e^(i*π)+1
Done
(0,0)
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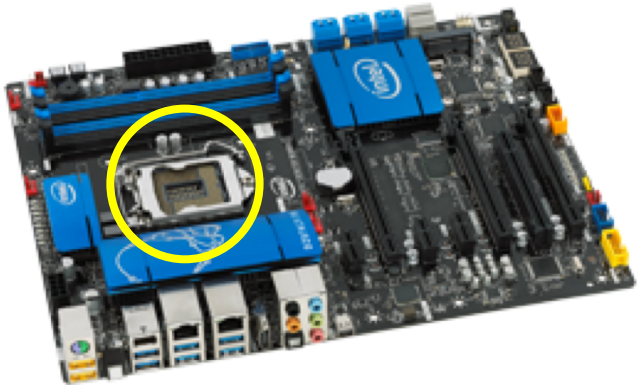
Motherboard



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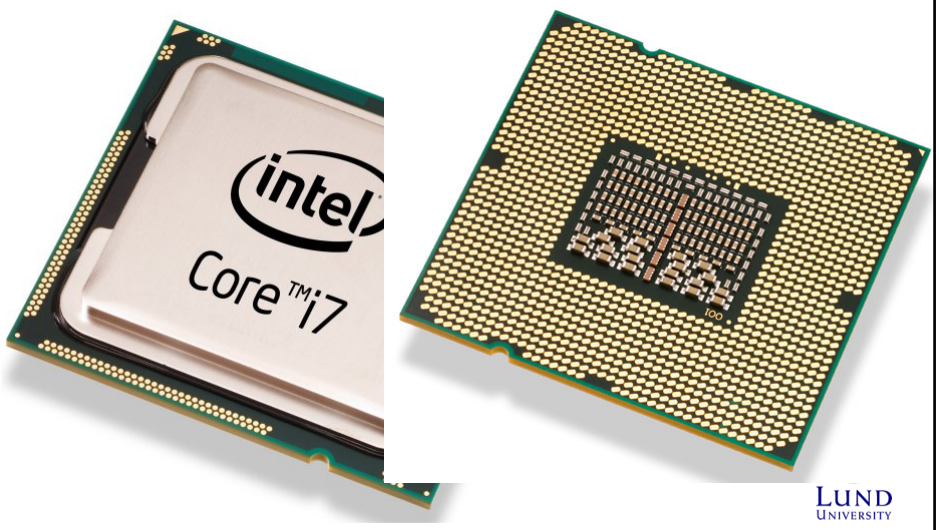
Microprocessor



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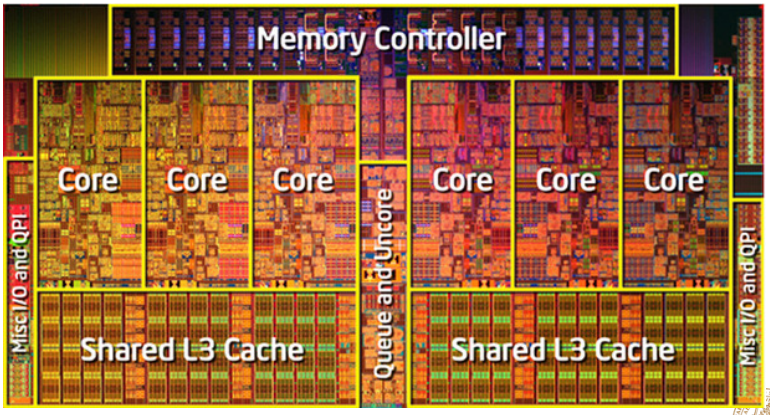
Inel i7 chip photo



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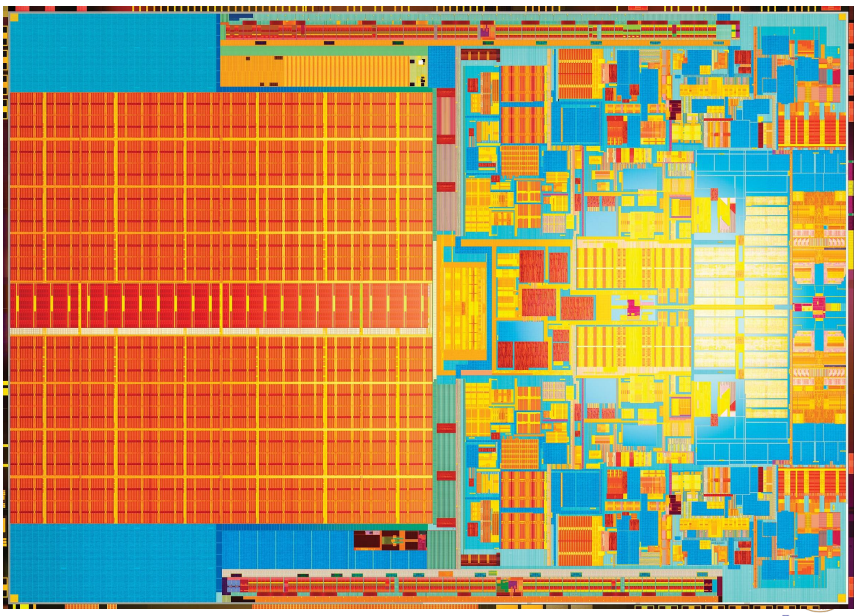

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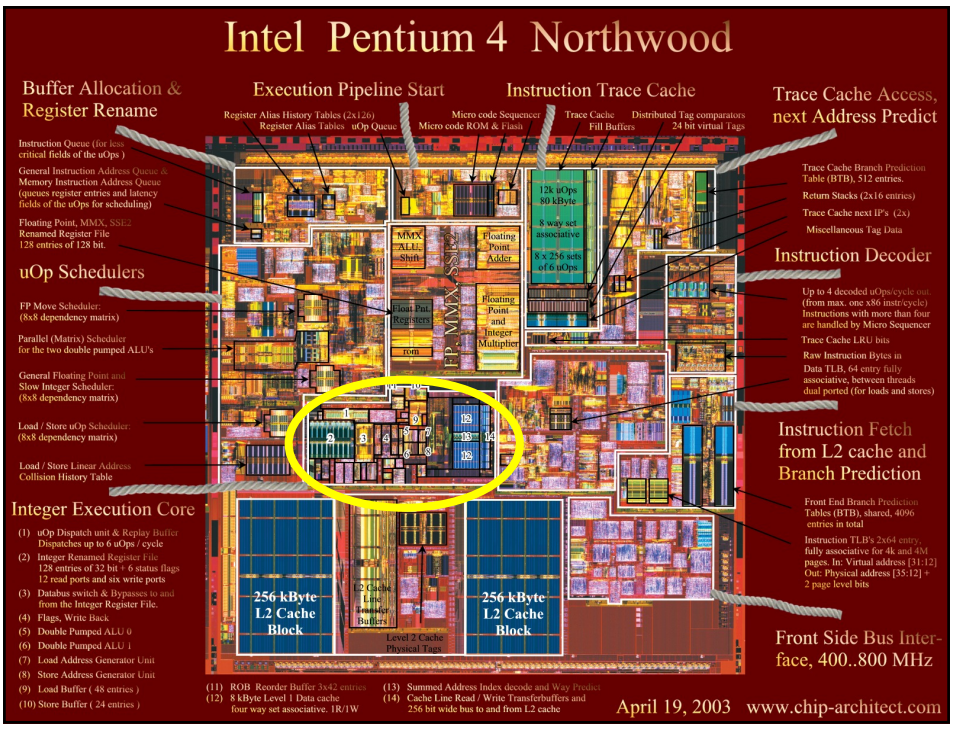


Integer Execution Core

(1) uOp Dispatch unit & Replay Buffer
Dispatches up to 6 uOps / cycle

(2) Integer Renamed Register File
128 entries of 32 bit + 6 status flags
12 read ports and six write ports

(3) Databus switch & Bypasses to and from the Integer Register File.

(4) Flags, Write Back

(5) Double Pumped ALU 0

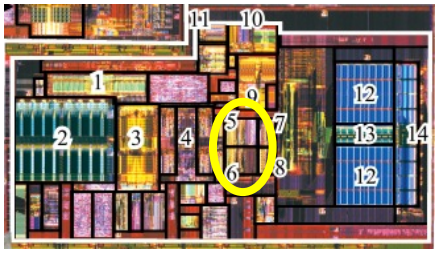
(6) Double Pumped ALU 1

(7) Load Address Generator Unit

(8) Store Address Generator Unit

(9) Load Buffer (48 entries)

(10) Store Buffer (24 entries)



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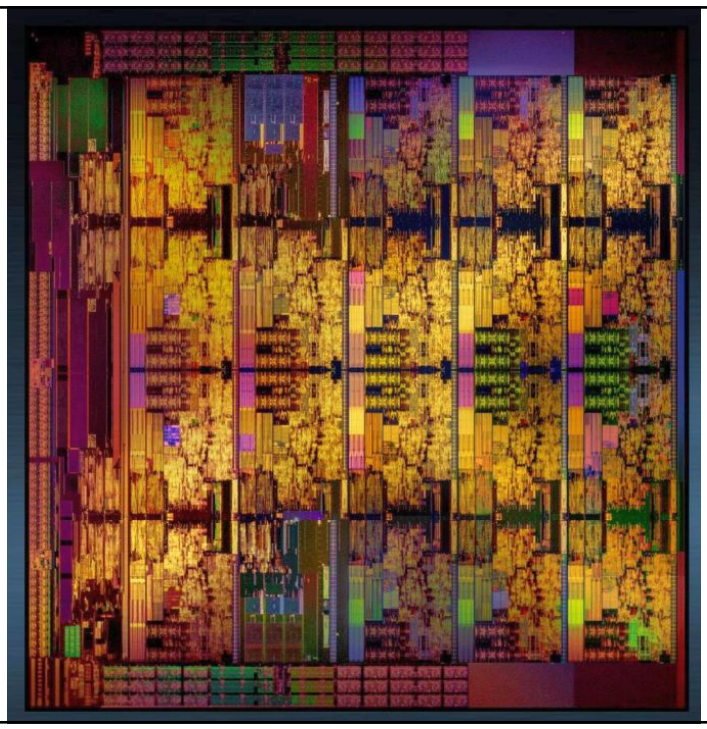
Intel i9



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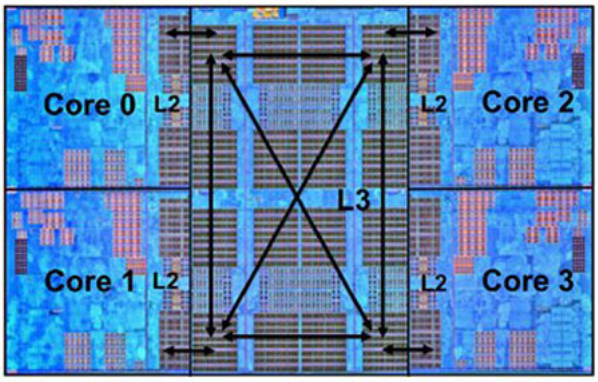
AMD Ryzen

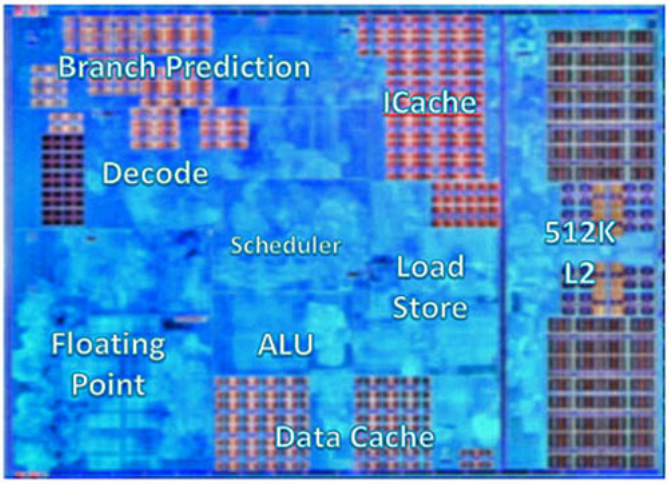
Core Complex (CCX)

- Core and L3 flexibility
- High-bandwidth low-latency data transfer
- Utilize upper level metals for high frequency data transfer
- Design for reuse
- Potential variants



AMD Ryzen
Core Functional Units

- 64KB IC
- 32KB DC
- ~20 tiles, <0.7m instances
- ROM for uCODE
- 5 L1 RAM variants

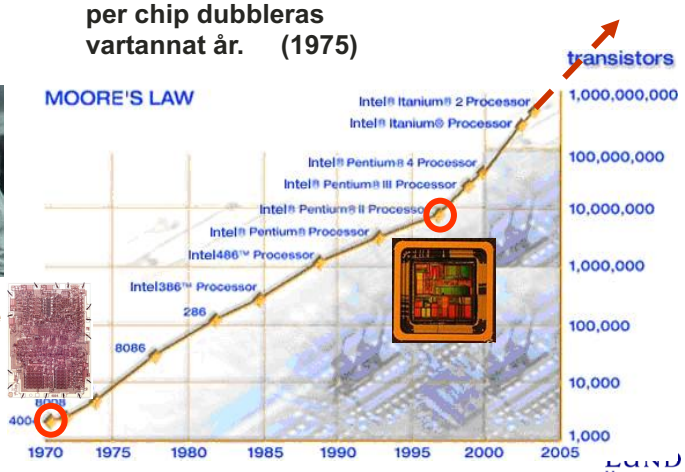


Moores Law

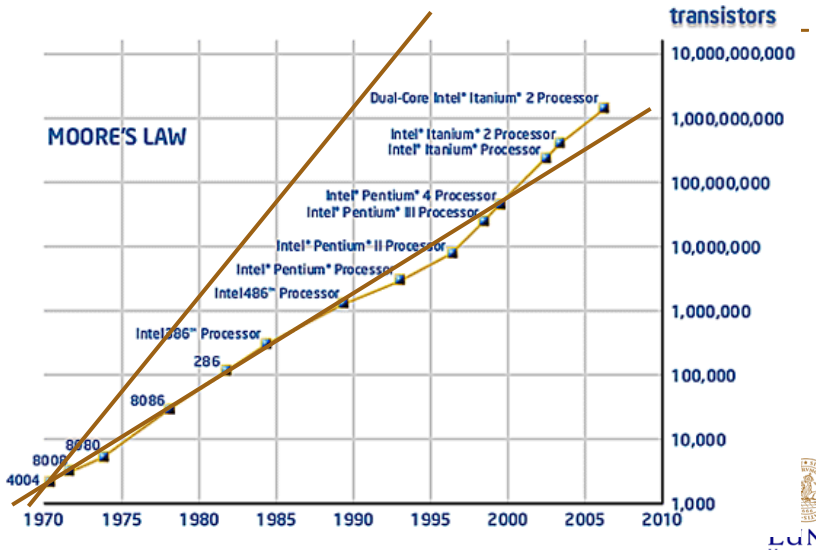
Antalet transistorer per chip dubbleras varje år. (1965)

Antalet transistorer per chip dubbleras vartannat år. (1975)

Gordon Moore
En av Intels grundare



Moores lag: uppdatering



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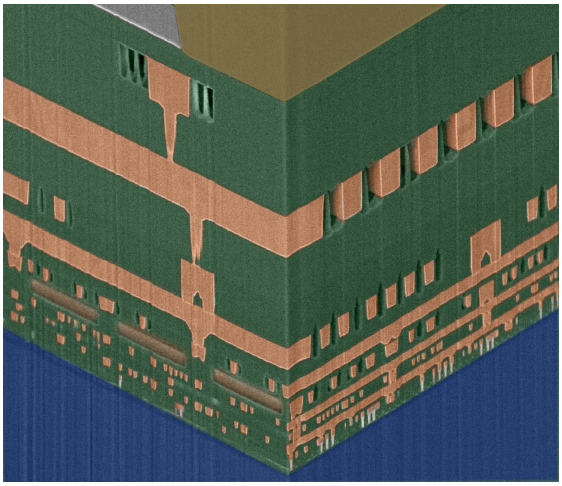
New processes



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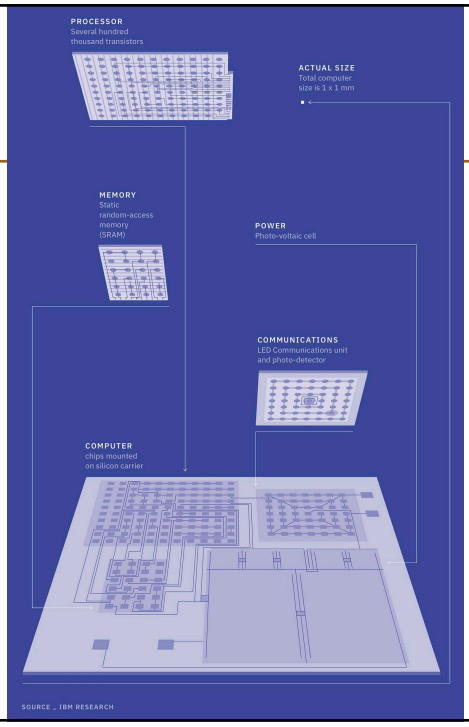

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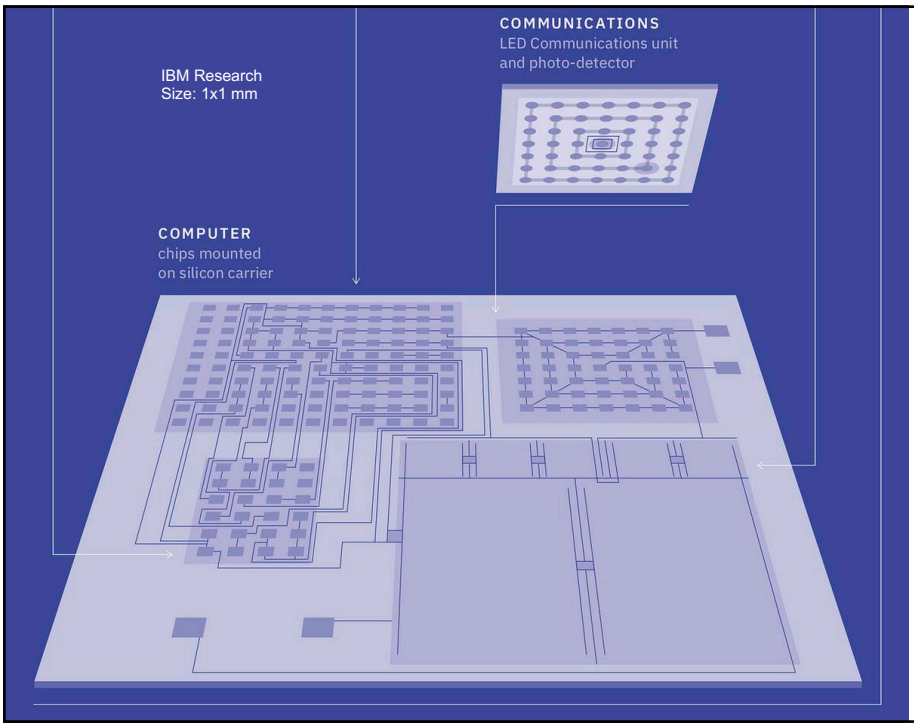
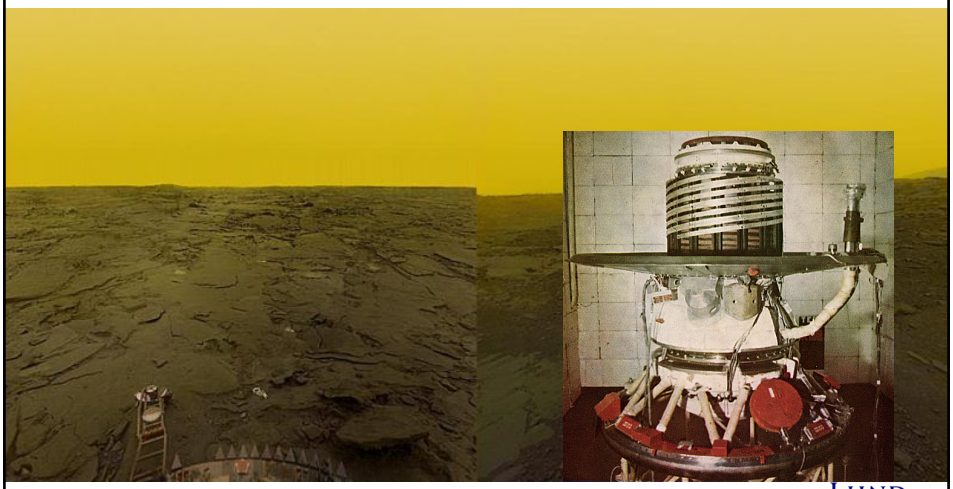


Venus



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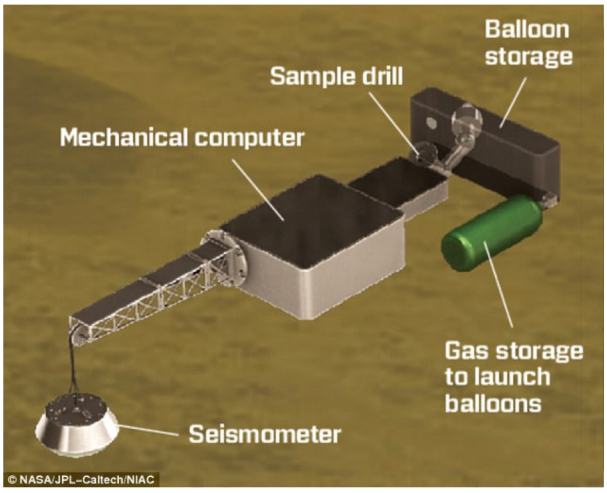
NASA Venus rover



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END

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