Oversampling and low order Delta-Sigma Modulators

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Overview

- Introduction
- Overview of Data Converters
- Quantization errors
- Oversampling
- First order noise shaping
- Second order noise shaping
- Generalization
- Non-ideal effects
- Multi stage noise shaping
- Multi bit quantizers in noise shaping converters
- Decimation

Speed – Accuracy of ADCs

A few applications of Delta-Sigma Converters

- Consumer electronics (for example audio)
- Communications
- Medical
- Sensor systems
- Instrumentation
- Computing
### Nyquist Rate Converters

- **A/D Converter**
  - AAF (Analog anti alias filter)
  - x\(x(t)\)
  - Samping with frequency \(f_s\)
  - Quantizer with R bit resolution
  - x\([k]\) R bits @ \(f_s\)

- **D/A Converter**
  - x\([k]\)
  - Analog low pass filter
  - \(x(t)\)
  - Continuous time

### Oversampling Converters with Noise Shaping

- **A/D Converter**
  - AAF
  - x\(x(t)\)
  - \(\Delta \Sigma\) modulator
  - x\([k]\)
  - \(x(t)\)
  - Decimation
  - \(x(k)\)
  - M bits @ \(f_s/\text{OSR}\)

- **D/A Converter**
  - x\([k]\)
  - Interpolation
  - \(\Delta \Sigma\) modulator
  - x\([k]\)
  - DAC
  - \(x(t)\)
  - Continuous time

### Static Quantizer Characteristics

- **Sampler**
  - x\(x(t)\)
  - Quantizer
  - x\([k]\)
  - Ideal DAC
  - LP filter
  - d\((t)\)

- The quantization error \(e[k] = x[nT] - x[k]\) is NOT a noise-like signal
- For deterministic ADCs, \(e[k]\) is a function of \(x(t)\)
- In other words: \(e[k]\) is HARMONIC DISTORTION of \(x(t)\)

### Quantization Error Noise Model

- If the input signal is a broad-band, noise-like signal we may reasonably assume that \(e[k]\) is a noise signal with uniform power spectral density.

  **SIGNAL VARIANCE**
  - Assuming a test tone with amplitude \(A_0\) as the input signal, we get a signal variance
  - \(\sigma_s^2 = \frac{A_0^2}{2}\)

  **QUANTIZATION NOISE VARIANCE**
  - Assuming uniform distribution on the errors, we get a variance on the quantization error (R bit quant.)
  - \(\sigma_q^2 = \frac{\Delta_n^2}{12} = \frac{(2A_n)^2}{12 \times 2^2 R}\)

  The best we can do to get a high SNR is to set the dynamic range of the quantizer, \(V_{max}\) and \(V_{min}\) to \(-V\) and \(V\) (the max and min amplitudes of the test tone).

  Our resulting signal-to-noise ratio (SNR) becomes:

  \[
  \text{SNR} = \frac{\sigma_s^2}{\sigma_q^2} = \frac{V^2/2}{(V - (-V))^2/12} = \frac{3}{2} \times 4^R
  \]

  or

  \[
  \text{SNR} = 1.76 + 6.02R \text{ dB}
  \]

  We gain 6.02 dB in SNR for each bit in our quantizer.
Oversampling

\[ \text{Oversampling ratio, OSR: } \quad OSR = \frac{f_s}{2f_B} \]

\[ \text{in-band noise power: } \quad v_q^2 = \frac{2}{f_s} \int_0^{f_s} \sigma_q^2 \, df = \frac{\sigma_q^2}{OSR} \]

Doubling the OSR increases SNR by 3 dB (0.5 bit / octave)

First-order noise shaping (1)

\[ \text{Signal transfer function: } \quad STF = \frac{v[k]}{u(t)} = \frac{H(z)}{1 + H(z)} = z^{-1} \]

\[ \text{Noise transfer function: } \quad NTF = \frac{v[k]}{q[k]} = \frac{1}{1 + H(z)} = 1 - z^{-1} \]

First order high pass filter

First Order Noise Shaping (2)

\[ \text{Magnitude of STF: } |STF|^2 = |z^{-1}|^2 = 1 \]

\[ \text{Magnitude of NTF: } |NTF|^2 = \left| \frac{z^{-1}}{1} \right|^2 = \left| \frac{1 - \cos \Omega - j \sin \Omega}{1 - \cos \Omega + j \sin \Omega} \right|^2 \]

\[ \Omega = 2\pi \frac{f_s}{f_s} \Rightarrow |NTF|^2 = \left( \frac{1 - \cos \Omega}{2} \right)^2 + \sin^2 \Omega = 2 - 2 \cos \Omega = \left( 2 \sin \frac{\Omega}{2} \right)^2 \]

Without noise shaping

First Order Noise Shaping (3)

\[ \text{In-band noise power: } \quad v_q^2 = \frac{1}{\pi} \int_0^{\pi} \frac{\sigma_q^2}{\Omega^2} |NTF|^2 \, d\Omega = \frac{\sigma_q^2 \gamma}{\pi} \int_0^{\gamma/2} \left( 2 \sin \frac{\Omega}{2} \right)^2 \, d\Omega \]

\[ = \frac{\sigma_q^2}{\pi} \left( \frac{\gamma}{2} \right)^2 \]

\[ = \frac{\sigma_q^2 \gamma^2}{3 \cdot OSR^2} \]

\[ \text{Compare to only oversampling} \]

Doubling the OSR increases SNR by 9 dB (1.5 bit / octave)
First Order Single-Bit Delta-Sigma ADC

First Order Delta Sigma DAC

Time Domain Simulation

Frequency Domain Simulation
Input Amplitude Sweep

Second-order noise shaping (1)

Signal transfer function:

\[ \text{STF} = \frac{v[k]}{u[l]} = z^{-2} \]

Noise transfer function:

\[ NTF = \frac{v[k]}{q[k]} = \frac{1}{1 + H(z)} = (1 - z^{-1})^2 \]

NTF magnitude:

\[ |NTF|^2 = \left(4 \sin^2 \left(\frac{\Omega}{2}\right)\right)^2 \]

2\textsuperscript{nd} order noise shaping (2)

\[ v_q^2 = \frac{\sigma_q^2 \pi^4}{5OSR^5} \]

Noise Shaping Generalization (1)

- The noise power within the band of interest \((0-f_B)\) decreases as the noise shaping order increases.
- The out-of-band noise increases for the high order noise shaping which has to be compensated by better digital filters.

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Data Converters Oversampling and low-order ΣΔ modulators

Non-Ideal Effects (1)

• In theory, to get a high SNR:
  - Increase the number of bits in the quantizer (M)
  - Increase the order of the noise shaping filter (L)
  - Increase the oversampling ratio (OSR)

• In practice, there are non-ideal effects to take into account:
  - Quantization noise is not the only noise source
  - Quantization noise is not truly white (tones, limit cycles)
  - The Noise Transfer Function is not ideal (clock jitter, finite amplifier gain & BW etc.)

• And the following deserve special attention:
  - DAC with M > 1 causes linearity problems (but is easier to stabilize)
  - L > 2 causes stability problems

Data Converters Oversampling and low-order ΣΔ modulators

Noise Shaping Generalization

• Inband noise power:
  \[ N_{q}^2 = \frac{\sigma_q^2 \pi^{2L}}{(2L+1) \cdot OSR^{2L+1}} \]

• Maximum SNR:
  \[ SNR_{\text{max}} = 6.02N + 1.76 + (20L + 10) \log_{10}(OSR) - 10 \log_{10} \left( \frac{\pi^{2L}}{2L+1} \right) \]

<table>
<thead>
<tr>
<th>OSR</th>
<th>SNR in bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>L=1</td>
</tr>
<tr>
<td>128</td>
<td>L=2</td>
</tr>
<tr>
<td>13</td>
<td>L=3</td>
</tr>
</tbody>
</table>

OSR = 64. SNR in bits: OSR = 128. SNR in bits: OSR = 128. SNR in bits:

<table>
<thead>
<tr>
<th>N</th>
<th>L=1</th>
<th>L=2</th>
<th>L=3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8.6</td>
<td>13.3</td>
<td>17.9</td>
</tr>
<tr>
<td>2</td>
<td>9.6</td>
<td>14.3</td>
<td>18.9</td>
</tr>
<tr>
<td>3</td>
<td>10.6</td>
<td>15.3</td>
<td>19.9</td>
</tr>
</tbody>
</table>

Note! Multi-bit quantizers are more linear \(\rightarrow\) More aggressive loop filter possible

Non-Ideal Effects (2) – Idle Tones (1)

• MOD1 simulation with full-scale single tone input

Non-Ideal Effects (3) – Idle Tones (2)

• MOD1 amplitude sweep for different input frequencies

Figures from [Schreier, Temes “Understanding Delta-Sigma Data Converters”]
Non-Ideal Effects (4) – Idle Tones (3)

- Simulated IBN power for different DC input levels

Non-Ideal Effects (5) – Idle Tones (4)

- Example of MOD1 idle tones from DC excitation

\[ y[n] = y[n-1] + w - v[n-1] \]

\[ v[n] = \text{sign}(y[n]) \]

\[ y[n] = y[n-1] + w - \text{sign}(y[n]) \]

- For \( u = 0.01 \),
  tones at \( fs/200 \)!

Non-Ideal Effects (6) – Idle Tones (5)

- Limit cycles appear for DC or slow varying input signals, if the input voltage is a rational fraction of \( V_{REF} \).

\[ u = \frac{n}{m} V_{REF} \]

...which cause the output to repeat itself with a certain period.

- If the frequency of repetition falls inband, the SNR can be severely degraded.

Non-Ideal Effects (7) – Idle Tones (6)

- Idle tones are caused by correlation with input signal \( u \).
- The amplitude of the idle tones increase with frequency and amplitude of input signal \( u \), and decrease with the order \( L \) of the modulator.

- One way to prevent limit cycles and idle tones is to add random noise (dither) at the input of the quantizer:

\[ \text{dither} \]

\[ q[k] \]

\[ y[k] \]

\[ v[k] \]

- Another way is to use a higher order system, where idle tone behavior is less likely.
Non-Ideal Effects (8) – op-amp offset

The offset of the first integrator and of the DAC are added to the input signal and cause equal offsets at the output.

The offset of the second integrator is referred to the input by dividing it by the gain of the first integrator, which is very large at DC, negating impact.

The ADC offset is also divided by the gain of one or more integrators when it is referred to the input, negating impact. This opens up the possibility of positioning the ADC thresholds at optimal voltage levels.

Non-Ideal Effects (9) – finite amplifier gain (1)

The DC gain of the op-amp is not infinite, so we obtain:

\[ \frac{V_{out}}{V_{in}} = C_1 \left( \frac{A_0}{1+A_0} \right) \left( 1 + \frac{1}{A_0} \right) - \frac{V_{out}}{V_{in}} \left( \frac{1}{A_0} \right) \]

\[ \frac{V_{out}}{V_{in}} = C_1 \left( 1 + \frac{A_0}{1+A_0} \right) - \frac{V_{out}}{V_{in}} \left( \frac{1}{A_0} \right) \]

\[ z^{-1} = \frac{(1+A_0)/(1+A_0+C_1/C_2)}{C_1+(1+A_0)C_2} \]

\( \rightarrow \) gain error of \( A_0/(1+A_0) \), and pole inside the unit circle:

\[ z_p = (1+A_0)/(1+\omega_0+G_0) \]

Non-Ideal Effects (10) – finite amplifier gain (2)

Simulations on a 2nd-order single-bit \( \Sigma \Delta \) modulator with op-amps with \( A_0=100 \) and sampling frequency of 2MHz, corner frequency at 3kHz, in very good agreement with theory.

Further, as long as the condition \( \pi(1+A_0) = 320 \) or OSR is verified, no SNR penalty is paid, compared to having \( A_0=100k \); however, 10dB are lost if OSR=250.

Assuming an ideal SC integrator, an input step of \(-V_{in}\) would result in an output step of \( \Delta V_{out} = V_{in}C_1/C_2 \) - in contrast, a real op-amp has a slewing time of \( t_{slew} = \frac{\Delta V_{out}}{SR} \).

At \( t_{slew} \), the output voltage differs from the final value by \( \Delta V = SR \cdot \tau \), and evolves exponentially in the remaining fraction of \( T/2 \); at \( T/2 \), the error on the output voltage is

\[ \varepsilon_{off} = \Delta V e^{-\frac{\tau}{2T}} \]

Thus, also in this case the error depends on the step itself, possible impact on linearity.

All these equations can be used in a behavioral simulator to enormously speed up the study of the combined impact of finite bandwidth and finite slew rate for the op-amp.
Non-Ideal Effects (12) - Amp. slew-rate and bandwidth

Ideal simulations show that the maximum changes at the output of the 1st and 2nd integrators are 0.749V and 3.21V with an $f_s$ of 50MHz, we have

$$SR_1 > \Delta V_{ref}/(T/2) = 75V/\mu s \quad SR_2 > \Delta V_{ref}/(T/2) = 321V/\mu s$$

Ideally, SNR=72dB with op-amp's $\beta_f=100MHz$, OSR=64, $f_o=160kHz$.

If $SR_1 = 325V/\mu s$, $SR_2 = 78V/\mu s$, the SNR does not change significantly; if $SR_1 = 73V/\mu s$, the SNR is not much affected, but the non-linear output response gives rise to harmonic tones – finally, simulations show (as expected) that a performance degradation on the 2nd integrator has a lower impact than on the 1st.

Non-Ideal Effects (13) – DAC linearity

- Single-bit DAC (N=1) is always linear.
- Multi-bit DAC (N>1) is as linear as its analog circuit elements (typically max. 10-12 bit).

In general, the linearity of a $\Delta\Sigma$-modulator is no better than linearity of its feedback DAC.

Non-Ideal Effects (14) - Improving DAC Linearity

- DAC element calibration
  - During fabrication (e.g. Laser trimming) – expensive, not effective for long term process variations (temperature, aging etc.)
  - During operation – can be performed periodically, but increase analog design complexity
- Dynamic element matching (DEM)
  - Randomise usage of circuit elements, so that systematic DAC errors are spread to random noise
  - Many different flavors are available (barrel-shifting, individual level averaging, data-weighted averaging, tree-structure etc.)
  - Works well, but requires a rather high OSR
- Digital estimation and correction of DAC errors
  - Digital Correction based method: Works for any OSR. Benefit from CMOS scaling.

Stability (1)

- Linear model calculations (as above) assume that the quantizer is linear and has a gain, $k_Q=1$.
- But the quantizer is a nonlinear block. The average gain is not well defined, especially not for the single-bit case.
- If the order, $L>2$, the feedback loop can be unstable for low values of $k_Q$. 
Stability (2)

- \( k_Q \) will be small if the input to the quantizer is large, that is:
  - if the input signal to the modulator is too strong
  - if the quantization noise is too high

- The out-of-band magnitude of the NTF (the NTF gain at \( f_s/2 \)) must be limited to reduce the quantization noise amplitude. (Lee’s rule)

- A commonly used rule-of-thumb is to use out-of-band gain of 1.5 for higher order systems, but it is neither a necessary, nor sufficient stability criterion.

- In practice, system level simulations with various realistic input signals is recommended to investigate the maximum stable input range!

Summary and Conclusions

- Delta Sigma Modulators can achieve a high SQNR without the need for accurately matched components
- Oversampling more effective when combined with noise shaping
- Oversampling relax anti-alias filtering considerably
- Large part of the filtering can be done using robust digital filters
- Scaling of CMOS technology can be used to trade increased speed for exponentially increased resolution by increasing OSR.
- Scaling of CMOS reduces size and power consumption of decimation filters
- Higher order loop filters and multi-bit quantizers can be used to increase performance, but requires careful attention to stability and linearity.