Data Converters

Specifications for Data Converters

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Overview

- Conditions of operation
- Type of converter
- Converter specifications
  - Static specifications
  - Dynamic specifications
- Digital and switching specifications

Conditions of operation

- The behavior of a data converter depends on the experimental set-up and the operational environment that influence its performance (which is true for all circuits, especially analog ones)
  - Process: the converter should work properly for all acceptable “corners” of the technology used (e.g., fast-fast, fast-slow, slow-fast, slow-slow MOS transistors, etc)
  - Supply voltage: should be allowed to fluctuate ±5% or even more
  - Temperature: from -20º C to 85º C in consumer applications, from -55º C to 125º C in military applications
  - The three variations above are collectively referred as PVT variations
- Maintaining performance over a wide range of PVT variations is difficult, especially for high-resolution converters. For example, a 14-bit converter requires accuracies as good as 600ppm/V (5V supply) or 0.3ppm/ºC (consumer applications)

Testing and characterization

- The operational conditions of data converters are critical for achieving (or measuring) the desired specifications
- Inaccurate measurement set-up or printed circuit board (PCB) limitations can totally mask an otherwise excellent converter performance
- Some good pieces of advice for PCB design are:
  - Connect to separate pins for analog and digital supplies to the single well-filtered supply generator on the PCB
  - Use on-chip voltage regulators to separate different voltage domains (especially analog/digital)
  - Enforce good V_{DD}/GND terminations by minimizing the length of the connecting leads and PCB paths
  - Avoid ground loops (e.g. between two sides of the PCB) especially for RF frequencies
  - Ensure high-level signal integrity with multi-layer boards with separate ground and power planes

More on PCB design and testing

- Control carefully the routing of the master clock and reference voltages through the PCB
- Use clock generators with low jitter, but also preserve the low jitter in the on-chip phase generator
- The PCB traces carrying the clock must be short with a solid ground plane underneath, in order to form a microstrip transmission line and enable impedance matching
- When low-speed converters use external references, utilize a clean voltage generator whose output impedance is low enough to avoid internal fluctuations greater than a fraction of LSB
- Check that the signal generator does not generate too high harmonic tones; otherwise, filter the signal from its harmonics with a high-quality passive low-pass filter

Converter specifications

- Specifications are used to interpret and understand the products available in catalogues of data converters, and to facilitate their use and characterization
- Specifications are divided into the following general classes:
  - General features
  - Static specifications
  - Dynamic specifications
  - Digital and switching specifications

General features – I

- Type of analog signal
  - Single ended → referred to a common ground, connected to the analog ground of the converter
  - Pseudo-differential signals → symmetrical with respect to a fixed reference voltage that may differ from the analog ground
  - Differential signals → not necessarily symmetrical with respect to a reference: the relevant signal is the difference of the two inputs (or outputs), regardless of their common-mode level
- Resolution
  - # of bits that an A/D uses to represent the analog input; # of bits at the input of a D/A
  - Together with the reference voltage, determines the minimum detectable change in the input voltage (A/D) and the minimum change in the output variable (D/A)

General features – II

- Dynamic range
  - Ratio (in dB) between the largest signal level the converter can handle and the noise level; determines the maximum SNR
- Absolute maximum ratings
  - Limit values beyond which the circuit capability may be impaired; functionality not necessarily deteriorated, but reliability may be affected
  - Electrical: typically, maximum supply voltage
  - Environmental: temperature range, maximum chip temperature, maximum soldering time, etc
- Electro-static discharge (ESD) notice
  - Human body and test equipment can store electrostatic voltages as high as 4 kV, which may discharge through the device
  - All ICs have protection circuits, but one should be very careful and follow all precautions recommended by the manufacturer

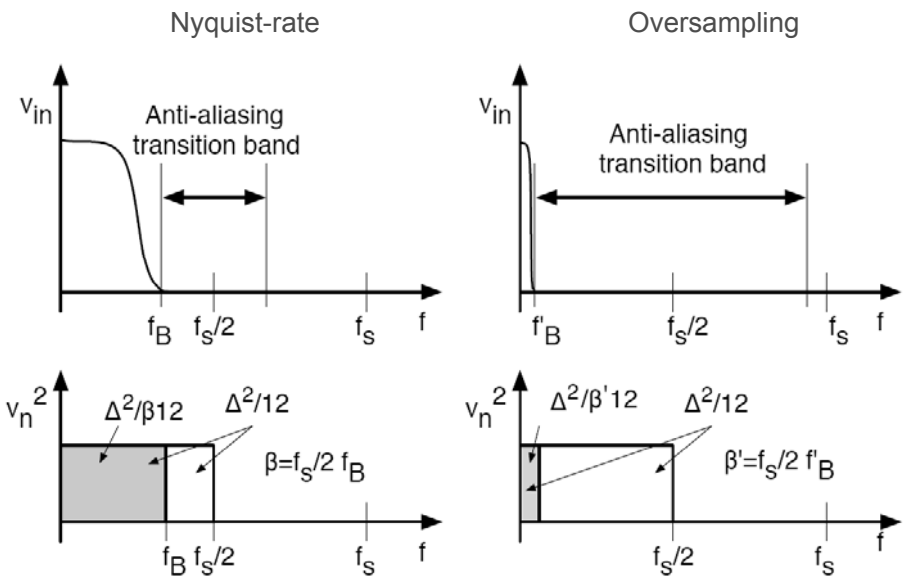
General features – III

- Pin function description and pin configuration
  - Table containing the number of each pin, together with name and performed function; a drawing of the package also provides the pin configuration
- Warm-up time
  - Amount of time for reaching thermal steady state after power-up
- Drift
  - Change in a parameter value vs. temperature and voltage
  - Commonly expressed in ppm/ºC and ppm/V

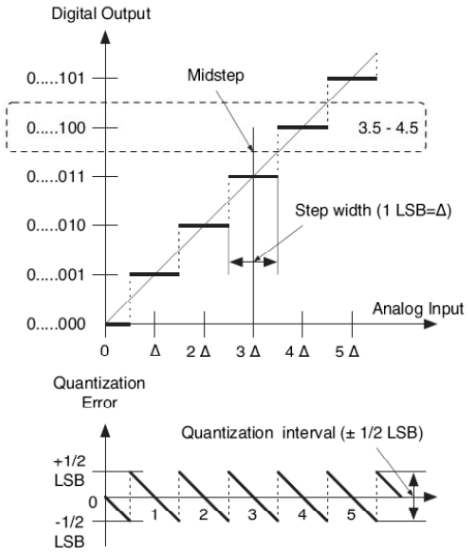
Type of converter

- The conversion algorithm normally provides this kind of information – e.g., we have flash, sub-ranging, ΔΣ converters (and several others)
- Converter are divided in two main categories: Nyquist-rate and oversampling
  - Nyquist rate: the input occupies a large fraction of the available bandwidth (Nyquist range)
  - Oversampling: the input occupies only a small fraction of the Nyquist range → easier anti-alias filter design, less quantization noise! (but higher sampling rate, of course)
- The ratio between the Nyquist limit and the signal band, $f_s/2f_B$, is called the oversampling ratio (OSR). Converters with a large OSR are called oversampling converters, whereas Nyquist-rate converters have a small OSR (typically less than 8)
- **Important**: when we talk about oversampling converters, we usually intend converters making use of so-called quantization-noise shaping as well → ΔΣ converters

Nyquist-rate and oversampling



Recall the ideal A/D transfer function



We have already seen this in the Introduction (if the first and last step are Δ/2 large, the full scale range is divided by 2^n-1 rather than by 2^n)

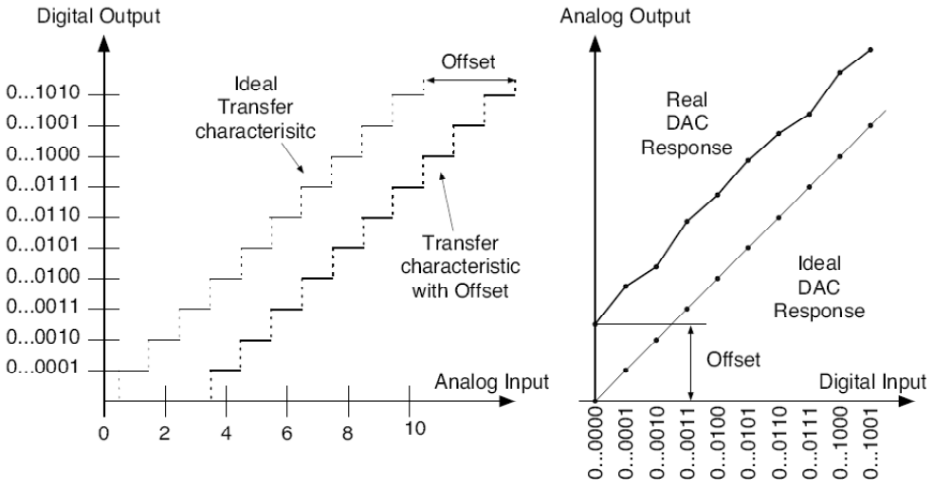
As known, the quantization error is confined between ±Δ/2, and is zero at mid-step

Real converters differ from this simplified picture

Static specifications – I

- Analog resolution
  - Smallest analog increment corresponding to a 1LSB code change (e.g., if N=16 and X_{FS}=1, the resolution is 15.26μ)
- Analog input range
  - Single-ended or differential peak-to-peak input that generates a full-scale response (peak differential signal → difference between the two 180º out-of-phase signal terminals; peak-to-peak differential signal → computed by rotating the phases of the inputs by 180º, taking the peak again, and subtracting it from the initial peak measurement)
- Offset
  - A shift for zero input → all quantization steps are shifted by the offset
  - Measured in LSB, absolute voltage/current, or as % or ppm of the full scale
- Zero scale offset
  - Difference between the ideal input voltage (1/2 LSB) and actual input voltage that causes the transition (0..00) – (0..01)

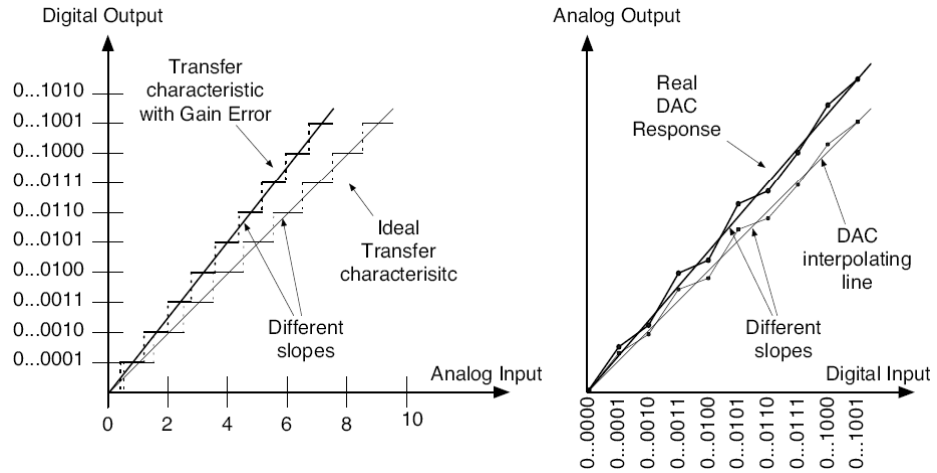
Offset error in ADC and DAC



Static specifications – II

- Common-mode error
  - Applies to ADCs with differential inputs → how the output changes when the input common-mode changes (usually measured in LSBs, ideally zero)
- Full-scale error
  - How far the last transition of an ADC is from the ideal top transition immediately below the reference voltage (measured in LSBs)
- Bipolar zero offset
  - Applies to DACs with bipolar outputs → when a DAC is loaded with (10...0), the deviation of the analog output from the ideal mid-scale value is called bipolar zero offset
- Gain error
  - Error in the slope of the straight line interpolating the transfer curve of an ADC or DAC
  - Ideally, this slope is D_{FS}/X_{FS}, where D_{FS} is the full-scale digital code. Since D_{FS} represents X_{FS}, this slope is ideally 1

Gain error in ADC and DAC



Differential non-linearity (DNL)

- Differential non-linearity error (DNL)
  - Deviation of the step size from the ideal Δ. Assuming that X_k is the transition between codes *k-1* and *k*, the width of the k^{th} bin is $\Delta_r = X_{k+1} - X_k$, and the DNL(*k*) is

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta}$$

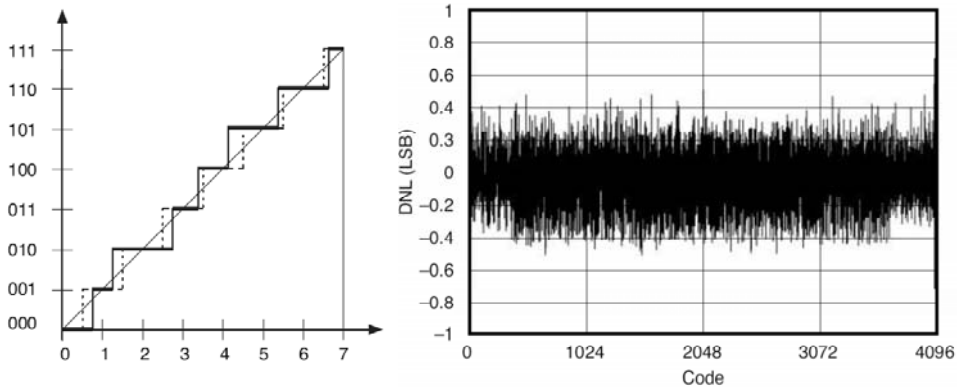
  - Most often the maximum value of the absolute value of DNL(*k*) is simply referred to as the DNL of the converter
  - An additional specification is the root-mean-square of the DNL, defined as

$$DNL_{rms} = \sqrt{\frac{1}{2^N - 2}\sum_{1}^{2^N-2} DNL^2(k)}$$

Example of DNL

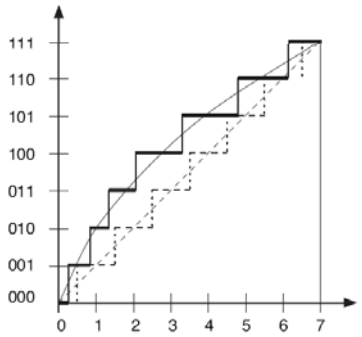
Here, the successive $\Delta_r(k)$ are uncorrelated → variation almost random, the interpolation curve is still a straight line from zero to full scale

Notice that, in this case, all DNL(*k*) are below ½ LSB



Integral non-linearity (INL)

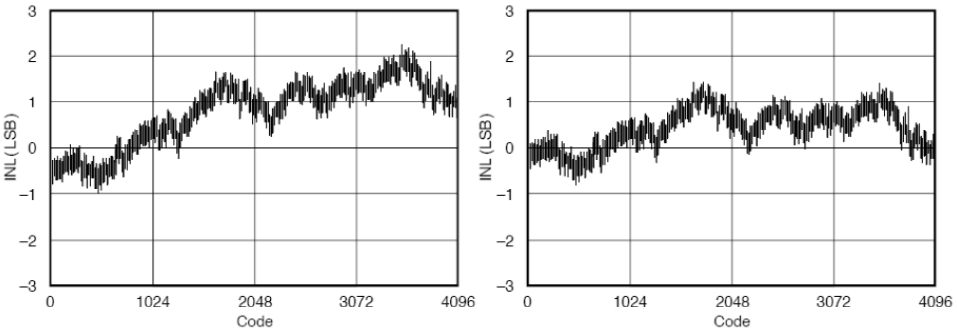
- Integral non-linearity error (INL)
  - Deviation of the transfer function from the ideal interpolating line.
  - Alternatively, deviation from the endpoint-fit line, which corrects for offset and gain errors. This definition is the standard one, since it is the relevant one for estimating harmonic distortion (we assume offset/gain corrections have been performed in the figure below)



Examples of INL

Same transfer function, without (left) and with offset/gain error correction

Notice that the left curve does not start from 0 and climbs up, and has a larger INL (> 2 LSB) than the corrected curve (1.3 LSB)



Gain and offset correction

With gain and offset correction, we have

$$X'(k) = \left(X(k) - v_{off}\right)(1+G)$$

with G=gain error, v_{off} = offset (in LSB). The DNL becomes

$$DNL(k) = \frac{\left(X'(k) - X'(k-1)\right) - \Delta}{\Delta} = \frac{\left(X(k+1) - X(k)\right)(1+G) - \Delta}{\Delta}$$

We can express $X'(k)$ in terms of DNL(k):

$$X'(k) = X'(k-1) + \Delta\left(1 + DNL(k)\right)$$

and, by iteration:

$$X'(k) = \Delta\left(k + \sum_1^k DNL(i)\right)$$

INL expression

Since the INL is a measure of the deviation of the transfer function from the ideal interpolating line, we have by definition

$$INL(k) = \frac{X'(k) - k\Delta}{\Delta}$$

which, with the previous expression for $X'(k)$ in terms of DNL, becomes

$$INL(k) = \sum_1^k DNL(i)$$

which shows that INL(k) is the running sum of the DNL (with all X(k) corrected for the gain error).

DNL vs. INL

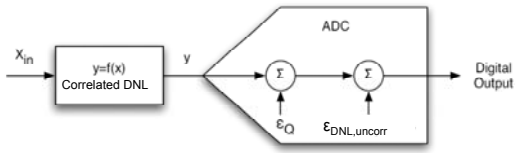
DNL and INL provide info with different consequences on the noise/distortion spectrum

The running sum of the *correlated* part of the DNL is the main source of INL

If the INL is few LSB over the entire range, the correlated part of the DNL is in the order of INL divided by the number of bins → looking at the DNL plot, it is impossible to predict the INL

The *uncorrelated* part of the DNL looks like noise and can be added to the quantization noise (i.e., increases the noise level)

The running sum of the *correlated* part of the DNL can be viewed as a non-linear block in front of the ADC, and causes harmonic distortion



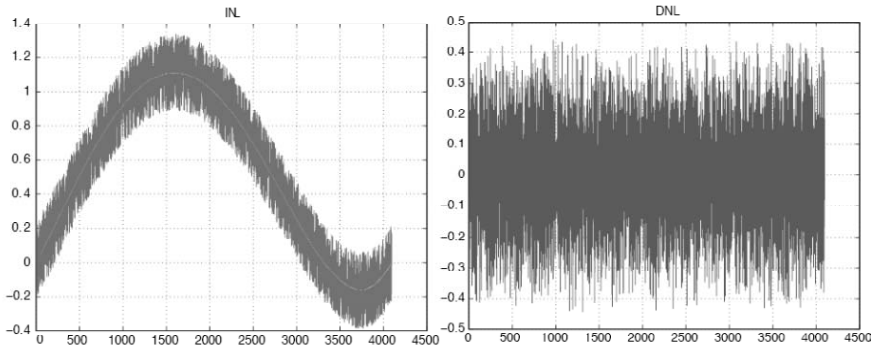
Example INL/DNL – I

Random variation of the INL within ±0.45 LSB, plus correlated variation described (in LSBs) by

running bin

$$y = 800\left(x + ax^2 + bx^3 + cx^4\right); \quad x = \left(n - 2^{N-1}\right)/2^N \quad (-0.5 \le x \le 0.5)$$

$$a = -0.01; \quad b = 0.01; \quad c = 0.02$$

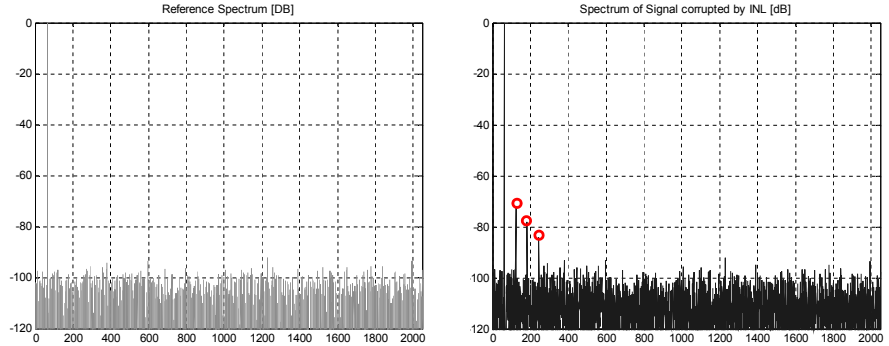


Example INL/DNL – II

N=12; 61-period sine wave (2^{12} samples); average noise floor: -107.1dBc (SNR_{max}= 12·6.02+1.76=74.0dB, processing gain=10·log(2^{12}/2)=33.1dB)

Since the uncorrelated part of the INL is so small, the noise floor increases only by a fraction of an LSB

However, the correlated component of INL creates 2nd harmonic distortion at -72dBc (X_{FS}=1, V_{in}=0.5+0.5sin(ωt))



Static specifications (end)

- Monotonicity
  - The ADC output increases (decreases) for increasing (decreasing) inputs
- Hysteresis
  - Dependence of the output code on the direction of the input signal
- Missing code
  - Certain digital codes never appear at the ADC output → corresponding quantization interval is zero → DNL = -1 LSB
- Power dissipation
  - Power consumed during normal operation or stand-by (or power-down)
- Temperature range
  - Ensuring the proper operation of the converter
- Thermal resistance
  - Capability to dissipate the consumed power, measured in ºC/W

Dynamic specifications – I

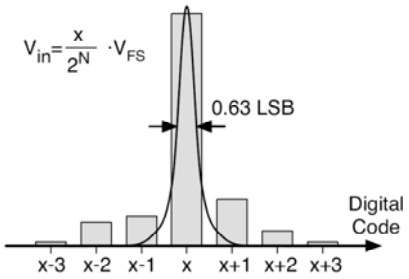
- Analog input bandwidth
  - Frequency for which a full-scale input of an ADC leads to an output 3dB below its low frequency value
  - This definition differs from what is used for amplifiers, where small-amplitude inputs are used
- Input impedance
  - Ideally, infinite for voltage inputs, and zero for current inputs
- Load regulation or output impedance
  - The load regulation measures the ability of the output stage of a DAC to maintain its rated voltage accuracy → describes the change per mA in the output voltage, and is expressed in LSB/mA
  - The output impedance is obtained from the load regulation by replacing the LSB with its value in mV, and is of course expressed in Ω
- Settling time
  - Time after which the step response of a DAC remains within a specified error range

Dynamic specifications – II

- Cross-talk
  - Measures the energy that appears in a signal because of undesired couplings with other signals
  - A poor PCB layout (e.g., critical signals running in parallel on the same layer) may cause crosstalk
- Clock jitter (aperture uncertainty)
  - Standard deviation of the sampling time
  - It is usually assumed that the jitter is a noise with a white spectrum
- Digital-to-analog glitch impulse
  - Amount of signal injected from the digital input to the analog output when the input changes → integral of the glitch area, in V·sec or A·sec
  - Usually maximum at half scale, when the DAC switches around the MSB and many switches change state, from (01...1) to (10...0)
  - Largely avoided with thermometer codes

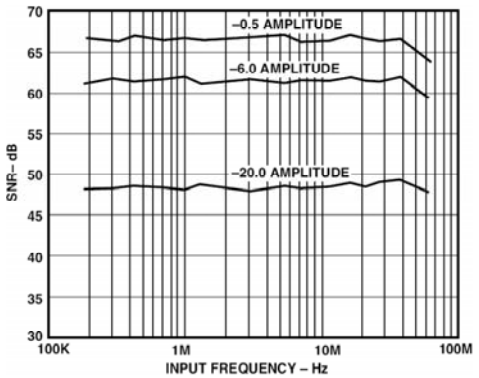
Dynamic specifications – III

- Glitch power
  - As before, but more general → may be caused by timing mismatches, etc
- Equivalent input referred noise
  - Measure of the electronic noise produced by the circuit in the ADC → for a constant DC input, the output is not fixed but shows a distribution of codes centered around the nominal code → the code histogram is approximately Gaussian, and its standard deviation defines the equivalent input referred noise, in LSB or V_{rms}. Below, this noise is 0.63 LSB.



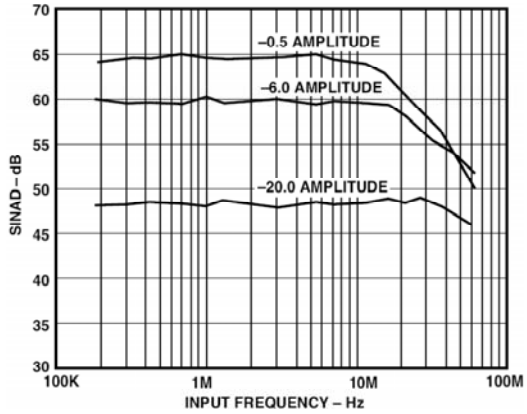
SNR

- Signal-to-noise ratio (SNR)
  - Ratio between the power of the signal (normally a sinusoid) and the total noise produced by quantization and other noise sources over the whole Nyquist interval
  - The SNR decreases with decreasing amplitude of the input, and usually decreases at high frequencies (non much in the example below)



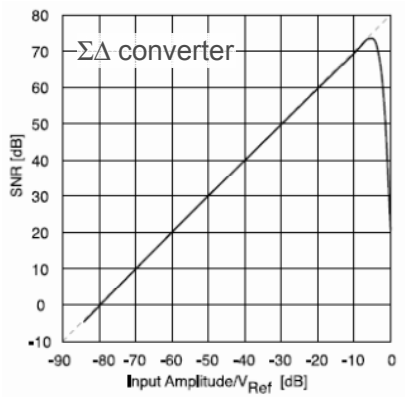
SNDR (SINAD)

- Signal-to-noise-and-distortion ratio (SNDR, SINAD)
  - Same as SNR, but taking into account distortion terms as well
  - root-sum-square of the harmonic components plus noise
  - Distortion usually increases with frequency



Dynamic range

- Dynamic range
  - Value of the input at which the SNR (or SINAD) is 0 dB
  - Useful (?) for converters that do not achieve maximum SNR/SNDR at 0 dB_{FS} (typically, sigma-delta converters)
  - Distortion usually increases with frequency



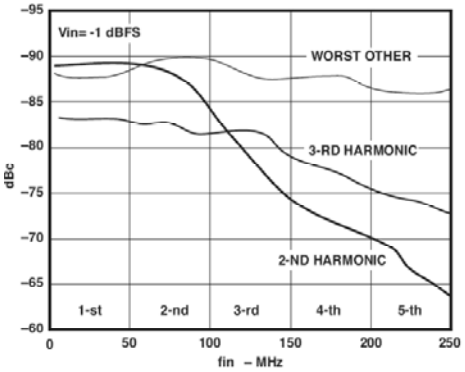
  - In this case, the maximum SNR is 74 dB, while the dynamic range is 80 dB → maximum SNR for input of -6 dB_{FS} (somewhat typical in these converters)

Harmonic distortion (HD)

- Harmonic distortion
  - Ratio between the *rms* value of the input and the *rms* value of harmonic components, including aliased frequencies; the n^{th} harmonic is at frequency

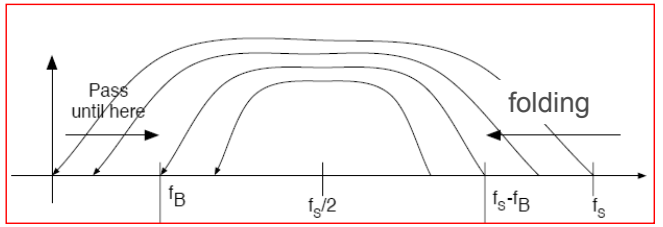
$$f_n = \left| \pm n f_{in} \pm k f_s \right|$$

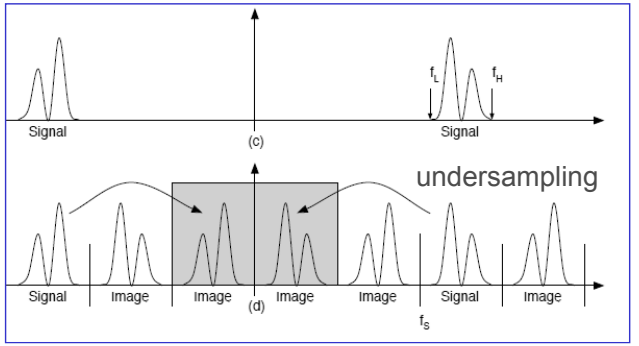
with *k* a suitable constant



  - 2^{nd} and 3^{rd} harmonic usually dominate
  - 2^{nd} harmonic is largely suppressed in differential designs (amount of suppression decreases for increasing frequencies)

Remember folding and undersampling?

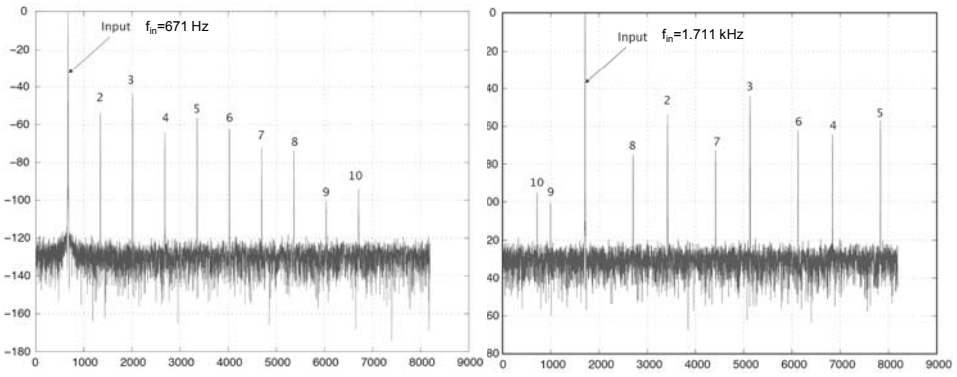




Example of harmonic distortion + folding

Length=1s, 2^{14} samples → $f_s \cong 16.4$kHz; with f_{in}=671Hz, 10^{th} harmonic at 6.71kHz, just below Nyquist ($f_s/2$=8.192kHz)

With f_{in}=1.711kHz, the 5^{th} is a 8.555kHz, higher than Nyquist → folded at $f_s - 5f_{in}$=7.829kHz; the 10^{th} at 17.11kHz is folded at $10f_{in} - f_s$=726Hz



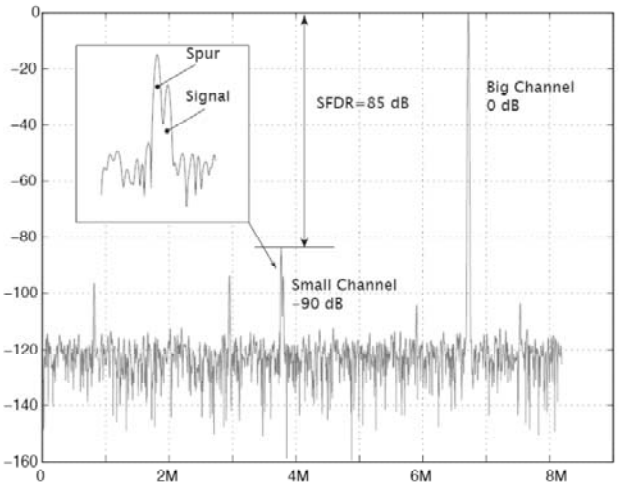
Total spurious distortion

- Total harmonic distortion, THD
  - Root-sum-square of the spurious components in the spectral output of the ADC (the input being a sine wave), expressed in dB, using as reference the *rms* value of the output at the input frequency
- Spurious-free dynamic range
  - Ratio of the input to the highest spurious spectral component in the first Nyquist zone
  - At high input amplitudes, the highest spurious tone is a harmonic of the signal; at low values, other tones caused by the time-variant nature of the converter may become dominant
  - Important in communication systems, where a small desired signal and large undesired signals are often present → a spurious tone generated by a large signal may fall close to the desired signal, masking it
  - SFDR is generally plotted as a function of the input amplitude

Example of SFDR

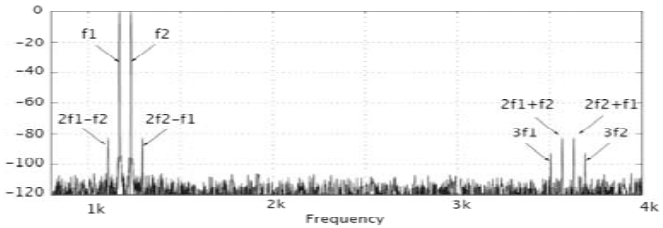
f_{big}=6.72MHz, f_{small}=3.8MHz, f_{clock}=16.4MHz

3rd harmonic of f_{big} folded at 3.76MHz, only 40kHz away from f_{small}



Intermodulation distortion

- Intermodulation distortion (IMD)
  - Harmonic tones generated by non-linearities with a multiple-tone input signal; in simulations/measurements, the input contains two closely-spaced tones of equal amplitude, which leads to
- Two-tone intermodulation distortion
  - Ratio of the rms value of either input tone, to the worst second-order or third-order intermodulation product (IMD2 and IMD3, respectively)
  - If the input tones have frequencies f_1 and f_2, the second-order tones appear at f_1-f_2 and f_1+f_2, while third order tones appear at $2f_1$-f_2, $2f_2$-f_1, $2f_1$+f_2, $2f_2$+f_1, $3f_1$, $3f_2$. Notice that the terms $2f_1$-f_2 and $2f_2$-f_1 fall very close to the input frequencies, i.e., “in band” in radio applications

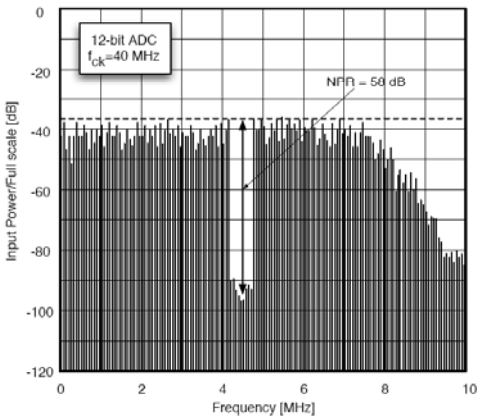


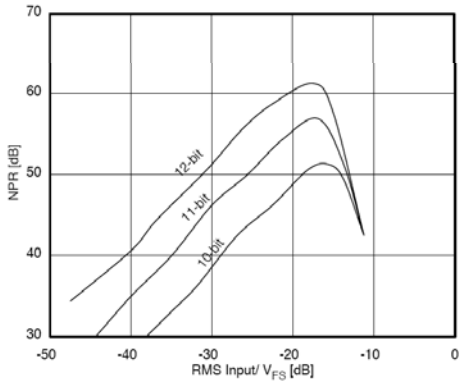
Dynamic specifications (cont’d)

- Multi-tone power ratio (MTPR)
  - Specific for converters in communication systems, defines distortion in multi-tone transmission systems
  - A sequence of tones is placed at frequencies that are multiple of a fundamental; a few such tones are left out
  - Harmonic distortion produces spurious tones at the missing tones frequencies
  - MTPR is the ratio of the amplitude of each input tone to the amplitude of the spurious tones
- Noise-power ratio (NPR)
  - Similar to MTPR, most commonly used in power amplifiers, but applies to ADCs as well, where it describes the linear performance of ADCs in frequency division multiplexed (FDM) links
  - Signals in an FDM system have different amplitudes and phases, and the overall signal looks like white noise passed through a BP filter

NPR (cont’d)

- If one channel is removed, the spectrum shows a deep notch, which is filled by the ADC noise and distortion
- The depth of the notch after the ADC gives the NPR
- For low input levels, quantization and thermal noise are dominant; for high input level, distortion becomes dominant (see plot on the right)





Dynamic specifications (cont'd)

- Effective resolution bandwidth (ERBW)
  - Defines the analog input frequency at which the SNDR drops by 3dB compared to its low-frequency value
  - Gives the maximum bandwidth the converter can handle, and should be well above the Nyquist limit
- Figure of merit (FoM)
  - Formula used in publications to measure the power efficiency of an ADC (BW=signal bandwidth, P_{tot}=total power consumption)

$$FoM = \frac{P_{tot}}{2^{ENOB} \cdot 2BW}$$

  - The FoM assumes that all power is consumed because of BW and ENOB (sometimes ERBW replaces BW)
  - Unfortunately, this FoM does depend on ENOB and BW (besides the technology used), so it is not very solid; nevertheless, it is used very often
  - Good converters show FoMs below 1pJ/conversion

Digital and switching specifications

- Logic levels
  - Set of non-overlapping ranges of amplitudes used to represent the logic states. Ensures compatibility between e.g. CMOS and TTL
- Clock rate
  - Range of allowed clock frequencies (may vary by more than one decade)
  - Good practice is to operate at 25% of maximum specification
- Clock timing
  - Specifies the features of the external clock, which is usually regenerated internally with edge-triggered flip-flops
  - A 50% duty cycle is normally best for optimal performance
- Clock source
  - A crystal clock provides the best jitter performance
- Sleep mode
  - Specify power-down mode, minimizes power consumption
  - It may take a few μs to go into sleep mode, and a few *ms* to power up again