Data Converters

Circuits for Data Converters

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Overview

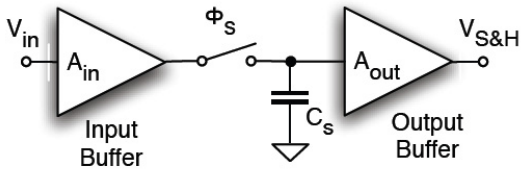
- Sample-and-Hold (S&H)
- Diode bridge S&H
- Switched emitter follower
- BJT S&H
- CMOS S&H
- CMOS switch with low supply voltage
- Folding amplifiers
- Voltage-to-current converters
- Clock generation

Sample-and-Hold

The S&H uses two phases → one for sampling, one for retaining and making the signal available to the following circuits (hold phase)

The input buffer reduces the input load, and the output buffer avoids discharging the sampling capacitance

If the output is available during the sampling period, we have a track-and-hold (T&H)

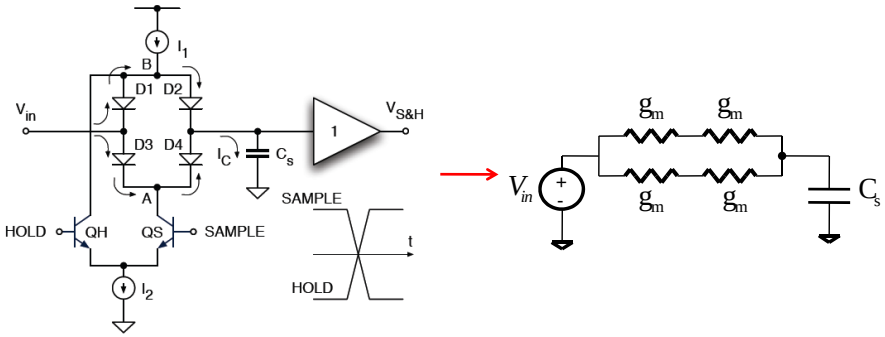


Diode bridge S&H

Schottky diodes → very fast → multi-GHz rates, medium resolution

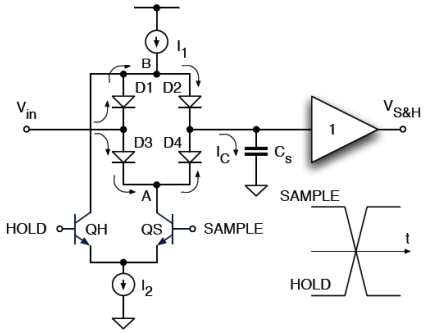
During sampling (tracking, actually), $I_1=I_2$ flows into the diode bridge, and V_{in} is copied onto C_s – if the current from V_{in} is small compared to I_1, we can use the small-signal linear circuit of the diode bridge as below → if g_m/C_s is much larger than the signal frequency, $V(C_s)= V_{in}$

During hold, no current flows through the bridge, and C_s stores the sampled signal – a unity-gain buffer is then cascaded as usual



Diode bridge – non-idealities

If $I_1 > I_2$ → current difference flows into the signal source during sampling, but during hold brings I_1 towards triode → voltage at B increases, D2 can enter conduction and corrupt the sampled signal → it is important to have $I_1 < I_2$, which brings node B down and does not cause any harm

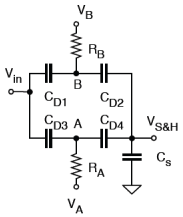


Other non-idealities

Aperture distortion → error in the switching-off time, caused by the derivative of the input signal → a varying input voltage delivers a current $I_C = 1/C_s \cdot dV_{in}/dt$ to C_s → a positive derivative makes the (total) current through D1 and D4 lower than in the other pair, leading to an asymmetrical bridge current → non-linear error in the switching instant

Track-mode distortion → caused by the non-linear impedance of the input buffer driving the bridge → since the non-linear voltage drop is proportional to the current , i.e. voltage derivative, this distortion increases with frequency

Hold pedestal → given by the (non-linear) charge injected by the diodes from *on* to *off*

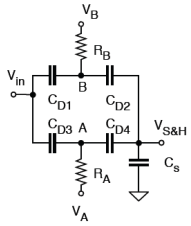


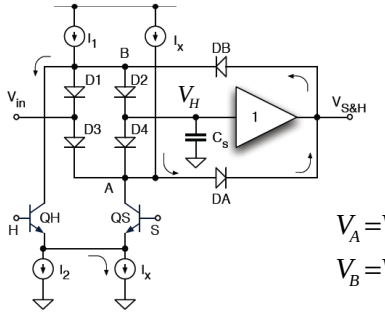
Hold feed-through → caused by parasitic coupling between input and output during hold (diodes are par. caps when off)

Improved diode bridge

The two extra diodes DA and DB are reverse-biased (by D2 and D4 conducting) during Tracking, but are turned on by the two I_x during Hold, clamping B and A at $\pm V_D$ (≈ ±0.7V) → constant biasing of D1 and D2 results in constant hold pedestal

A and B are biased through the load impedance of the buffer, and the conducting diodes DA and DB have a low impedance of $1/g_m$ → R_A and R_B are much reduced → decoupling of input from C_S → much reduced feedthrough





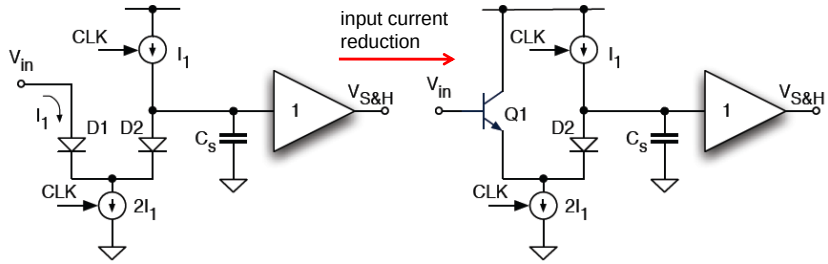
$$V_A = V_H + V_D$$
$$V_B = V_H - V_D$$

Simplified diode bridge / switched emitter follower

Reduced requirements from power supply (0.7V saved); circuit on the right diminishes the input current load by the BJT gain

Major drawback → requires simultaneous switching-off of both current sources to prevent spur injection into C_S (1ps delay with 1pF and 1mA → 1mV offset)

Impossible to align very well the two clock signals → Self synchronization required

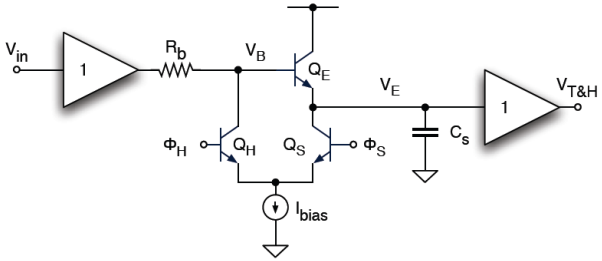


Improved version

Q_E is an emitter follower during sampling; when Φ_H goes high and Φ_S low, I_{bias} flows through R_b and V_B is pulled down, but the emitter of Q_E is kept high by C_S → Q_E is switched off

The voltage on C_S is a shifted replica of the input → usually not a problem, as the DC component is not interesting

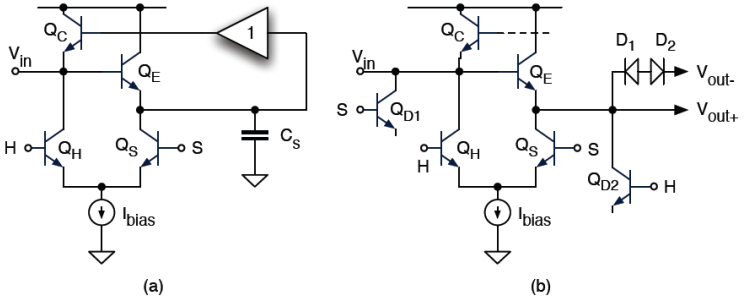
However, C_{BE} in Q_E causes a hold pedestal that depends on the reversed V_{BE} during hold → uncontrolled V_{BE}, unpredictable pedestal



Improved – II

Left: Q_C replicates the held voltage and clamps V_B during hold → constant V_{BE} = constant pedestal; during tracking Q_C goes off and does not influence operations

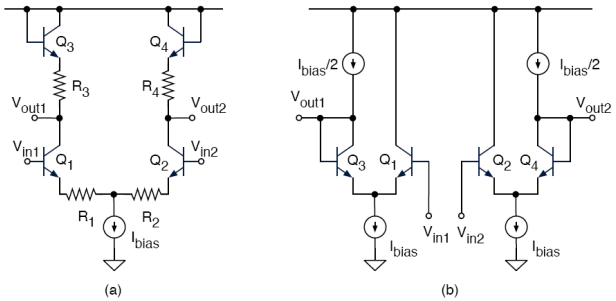
Other source of pedestal: charge injection from base and collector of Q_S and Q_H → Q_S matched by dummy transistors Q_{D1} and Q_{D2} (right) driven by complementary phases; back-to-back diode D_1 and D_2 between the differential outputs match the non-linear C_{BE} from Q_E



Input buffers

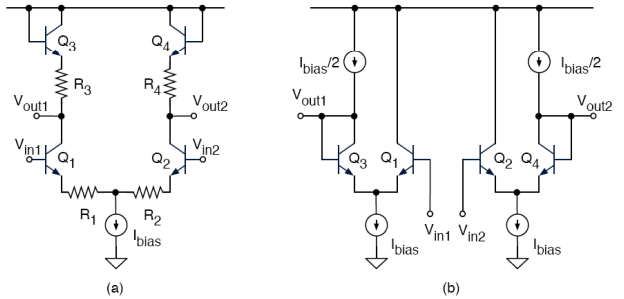
Input buffers must be linear, fast, and capable of switching quickly from Sample to Hold and vice-versa

Left: differential buffer with gain=-1 (if equal resistances and BJTs); very fast, but inverting → DC level of one output may become close to its input → small V_{CB}; in the off-state both outputs are pulled down → V_{CB} can become forward biased → collector current from the input, slowing down the next off-on transition



Input buffers – II

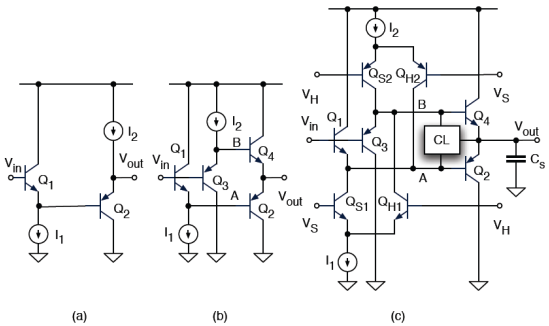
Right: pseudo-differential, each buffer is an emitter follower with a shift-up at the output to compensate for the shift-down at the input; avoids the previous problem (but x2 current for the same f_T) → if outputs are pulled down by current larger than $I_{bias}/2$, Q_3 ad Q_4 are switched off, and can quickly be switched on when the circuit goes back to tracking



Complementary BJT S&H

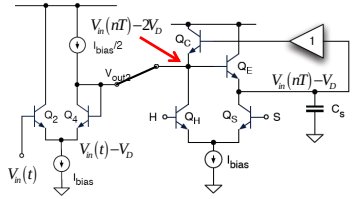
If *npn* and *pnp* have comparable f_T (however, not usual!) → circuit (a) implements the DC shift in the previous slide; (b) → push-pull implementation – with equal *npn* (*pnp*) areas and I_1=I_2, bias output current is I_1; during transients, one output transistor reduces its V_{BE}, making it available for the other; if one goes off, all current through the other transistor flows through the output (class B)

(c): switched buffer → Q_{S1}/Q_{H1} (Q_{S2}/Q_{H2}) divert I_1 (I_2) from the emitter of Q_1 (Q_3) (CL → clamping block; sources/sinks I_1/I_2 during Hold)



Features of BJT S&H

Good speed and linearity, but limited dynamic range (junctions must be kept in reverse in the off-state) – consider the buffer/S&H below:



Hold → Q_4 is in reverse; emitter of Q_4 follows the input via Q_2 → the limit to the input voltage swing is (assuming a differential input signal $\pm V_{in}$):

$$\begin{cases} V_{in}(nT)-2V_D-\left[V_{in}(t)-V_D\right]<0 & \rightarrow V_{in}(t)>V_{in}(nT)-V_D \\ -V_{in}(nT)-2V_D-\left[-V_{in}(t)-V_D\right]<0 & \rightarrow V_{in}(t)<V_{in}(nT)+V_D \end{cases} \quad \text{for} \quad nT<t<nT+T/2$$

hold instants hold period

Maximum change of full-range sine wave (at Nyquist) is V_{ref}/2 over the time T/2 → $V_{REF}/2<-V_{REF}/2+V_D$ → maximum differential input amplitude cannot exceed $2V_D$

S&H non-linearity

Depends on the non-linear V_{BE} – I_E relation $V_{BE} \approx V_{BE0}+V_T \ln\frac{I_E}{I_{bias}}$

I_E is the sum of I_{bias} and the current into C_S: $I_E \approx I_{bias}+C_S\frac{dV_{in}}{dt}$

In a pseudo-differential circuit, we have

$$V_{out+}=V_{in+}-V_{BE0}-V_T\ln\frac{I_{bias}+C_S\frac{dV_{in}}{dt}}{I_{bias}}; \quad V_{out-}=V_{in-}-V_{BE0}-V_T\ln\frac{I_{bias}-C_S\frac{dV_{in}}{dt}}{I_{bias}}$$

resulting in the error on the differential output:

$$\delta V_{out,d}=V_T\ln\frac{I_{bias}+C_S\frac{dV_{in}}{dt}}{I_{bias}-C_S\frac{dV_{in}}{dt}}$$

S&H non-linearity – II

With an input $V_{in}=A\sin(\omega_{in}t)$, we obtain

$$\delta V_{out,d}=V_T\ln\frac{I_{bias}+A\omega_{in}C_S\cos(\omega_{in}t)}{I_{bias}-A\omega_{in}C_S\cos(\omega_{in}t)}$$

odd function → only odd harmonics, with amplitude proportional to input amplitude and frequency, and sampling capacitance

To minimize → bias current should be much larger than current into sampling capacitance

Example: if C_s = 4pF, f_{in} = 200MHz, A = 1V → I_{Cs} up to 5mA

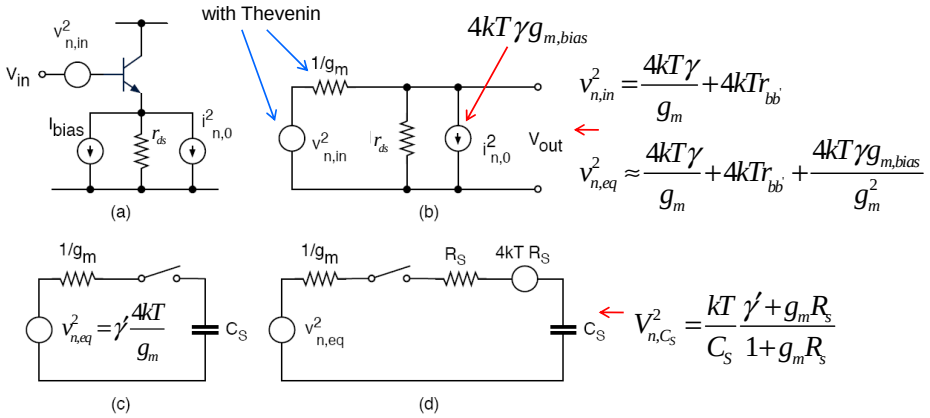
It can be shown that SFDR=100dB requires $I_{bias} \approx 8I_{Cs}$ → I_{bias} = 40mA

Noise in emitter follower

Important: this part is wrong in the book

Channel noise factor γ → 2/3 for ideal MOS, 1/2 for ideal BJT

In (d) below → a large R_S in series with switch trades reduced speed for reduced total noise power, which tends to the minimum limit of kT/C_S for $g_m R_s$ large (impact of $r_{bb'}$ and $i_{n,0}^2$ is minimized)



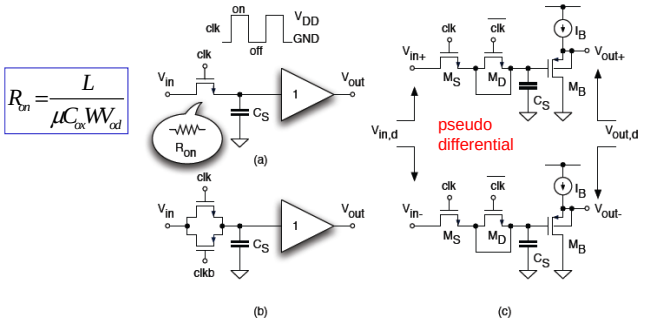
CMOS S&H

Time constant $R_{on}C_S$ → much lower than time allowed for charging C_S

If switched voltage has a large range → use nMOS and pMOS in parallel → total resistance is ideally constant over a large voltage range

Dummy M_D → clock feedthrough compensation

(c) uses a simple source follower for maximizing speed (GHz range) → bad linearity, even with B=S to avoid non-liner bulk effect (max. 70dB, compared to 100dB with BJT for the same current)

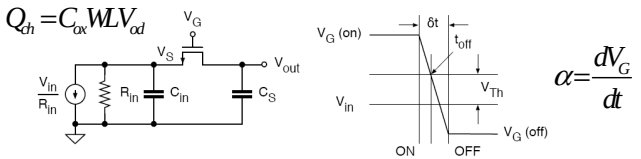


Clock feedthrough

When MOS from *on* to *off*, due to: 1) channel charge Q_{ch} flowing into C_S, and 2) clock charge injection through C_{gd}. The fraction of Q_{ch} injected into C_S depends on a) MOS parameters, b) slope of the clock phase, c) boundary conditions on both sides of the switch

Charge injection studied with simplified RC model for both gate and channel; numerical solutions as function of the switching parameter B:

$$B = V_{od}\sqrt{\frac{\mu C_{ox} W/L}{\alpha C_S}}$$

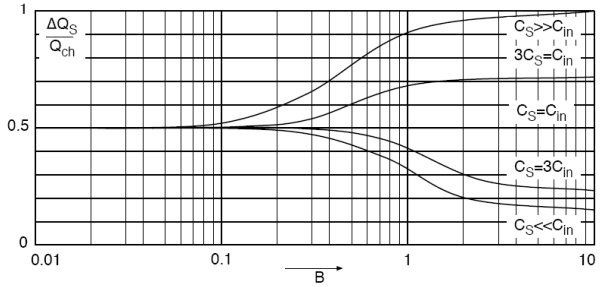


Clock feedthrough – II

low B (i.e. fast switching) → 50% of channel charge flows into sampling capacitance

large B → depends on ratio between the two capacitances → less predictable

low B is more predictable → preferred

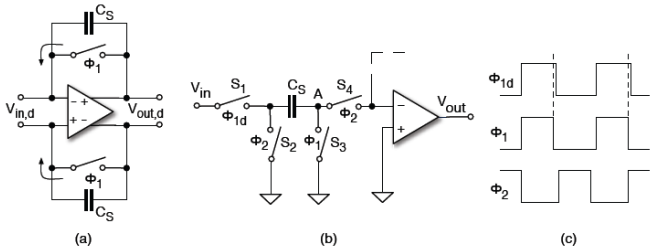


Feedthrough compensation

Dummy M_D → injects all its channel charge into C_S → should be approx. half as large as the switch → this asymmetry reduces the effectiveness of cancellation to 70-80%

In differential A/D → differential cancellation of injection → common-mode injection is suppressed by the differential topology, as in (a) below – effectiveness of 80-90%

Another approach is to accept a constant injection = constant offset, as in (b) → not an issue if there is no signal at DC

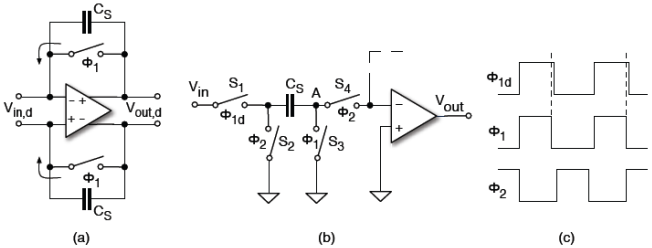


Feedthrough compensation – II

(b) → S_3 opens slightly earlier than S_1 (and S_4 slightly earlier than S_2), and some of the channel charge flows into C_S; however, node A switches between ground and virtual ground, and to the first order the channel charge in S_3 (S_4) is signal independent → DC offset only (canceled in a differential implementation), no distortion

The channel charge for S_1 (S_2) is signal dependent, but when S_1 opens C_s is already floating → no signal-dependent charge redistribution on C_S!

The C_S plate connected to ground determines the actual sampling → so-called bottom-plate sampling technique



Two-stage OTA as T&H

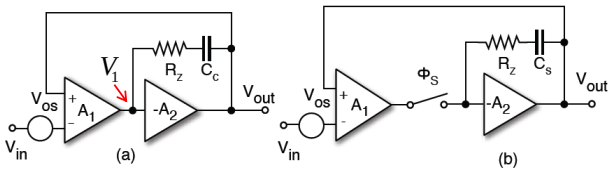
Output of a two-stage OTA in unity-gain feedback tracks the input → the 1st stage output is the input divided by the 2nd stage gain ((a) below)

Compensation capacitor in OTA can be used as sampling capacitor as well → C_C becomes C_S in (b) – voltage at the end of tracking is

$$V_{out}(nT)=\frac{(V_{in}(nT)+V_{os})A_1A_2}{1+A_1A_2} \qquad V_1(nT)=\frac{V_{out}(nT)}{A_2}\approx 0$$

V_1 is (almost) zero if A_2 large → constant channel charge → feedthrough is just an offset; 1st stage not used during Hold → offset auto-zeroing is possible (connect as unity gain buffer, store offset onto a capacitance)

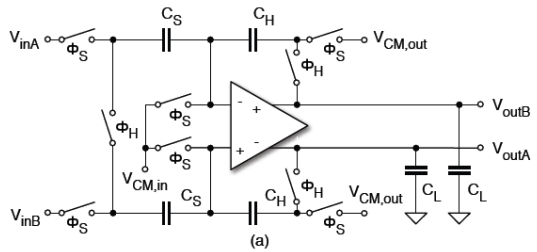
ok for medium-speed if buffering is needed; also, unity-gain configuration requires common-mode range to be the same as the input swing



Virtual ground in CMOS S&H

In general, virtual ground relieves the requirement of a large input common mode

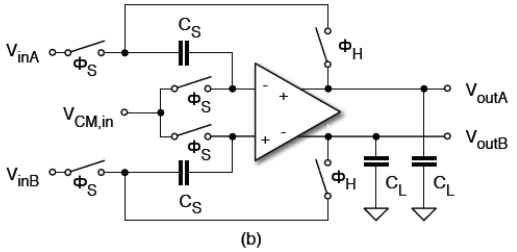
Charge-transferring S&H below: 1) during Sample → C_S are charged between V_{in} and input common mode $V_{CM,in}$, C_H between input and output common mode $V_{CM,out}$ → offset cancellation and common-mode shift if needed; 2) during Hold → C_S are connected in (anti) series and loop is closed → charge transferred to C_H, common-mode input is rejected; gain or attenuation possible



Virtual ground in CMOS S&H – II

Flip-around topology → more economic implementation: fewer caps, where C_S are first connected to the input, and then in feedback – however, only unity gain possible – however, feedback factor is 1, while it was ½ in the previous circuit → flip-around more power efficient (lower open-loop gain-bandwidth-product required for the same sampling frequency)

Neither scheme uses the op-amp during sampling → op-amp is in open-loop → output to V_{dd} or ground, long recovery time → differential output is shorted and connected to a common-mode voltage during sampling



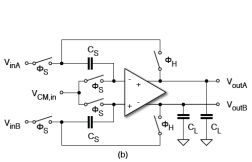
Noise analysis of flip-around S&H

Each switch has on-resistance R_{on}, and a thermal noise voltage (density) of $v_n^2 = 4kTR_{on}$. The op-amp has an equivalent input noise voltage $v_{n,op}^2$

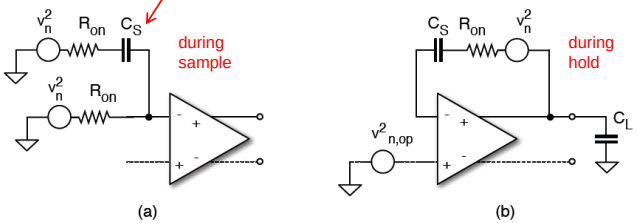
Every noise generator causes a colored noise spectrum across each capacitor; when the switches open, the sampled noise on the capacitor is given by the integral of the colored spectrum

Uncorrelated noise → adds power-wise; Correlated → adds signal-wise

During Sample, we have the situation in (a) → two switches in series with C_S → since the integrated noise is kT/C independently of R, we have



$$V_{n,sample}^2 = \frac{kT}{C_S}$$



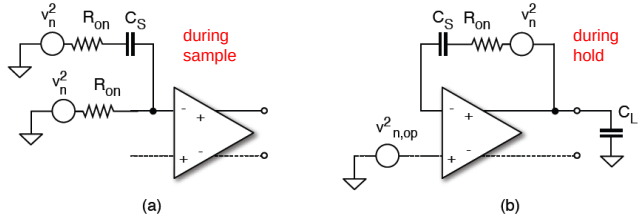
Noise analysis of flip-around S&H – II

Hold → a) the sampled noise on C_S is there also during Hold (of course)

Hold → b) because of the virtual ground, the noise from the switch in feedback is found at the output, until it rolls off because of the finite bandwidth of the op-amp

$$v_{n,out} = v_n \frac{A}{1+A} = v_n \frac{\omega_T/s}{1+\omega_T/s} = v_n \frac{1}{1+s/\omega_T}$$ "signal"

$$v_{n,out}^2 = \frac{4kTR_{on}}{1+(\omega/\omega_T)^2} \rightarrow V_{n,out}^2 = kTR_{on}\omega_T$$ power

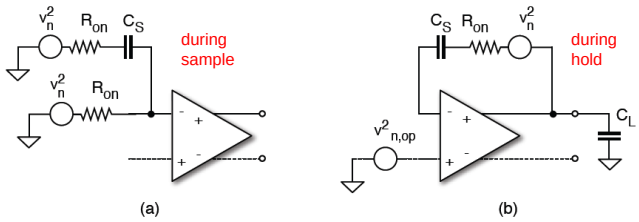


Noise analysis of flip-around S&H – III

Hold → c) The same analysis applies to op-amp noise, $v_{n,op}^2 = \frac{4kT\gamma'}{g_m}$

Assuming $\omega_T = \frac{g_m}{C_L}$, we have the total output noise power as

$$V_{n,out,flip}^2 = \frac{kT}{C_S} + g_m R_{on} \frac{kT}{C_L} + \frac{\gamma' kT}{C_L}$$



Noise analysis of flip-around S&H – IV

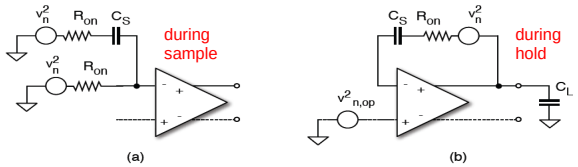
$$V_{n,out,flip}^2 = \frac{kT}{C_S} + g_m R_{on}\frac{kT}{C_L} + \frac{\gamma' kT}{C_L}$$

The sampling time constant $R_{on}C_S$ is typically lower than $1/\omega_T$, i.e.

$$R_{on}C_S << \frac{C_L}{g_m}$$

which means that the second term in the noise expression is negligible →

$$V_{n,out,flip}^2 \approx \frac{kT}{C_S} + \frac{\gamma' kT}{C_L}$$

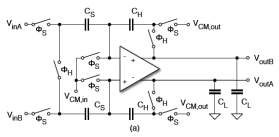


Noise analysis of charge-transfer S&H

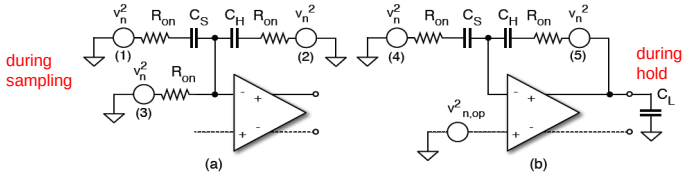
Sampling → charge on C_S is later transferred to C_H → if the charges on the two caps are correlated, linear (signal-wise) addition → assuming $C_S = C_H$, the transfer function of noise source #3 on both C_S and C_H is

$$H_{C_S}(s) = H_{C_H}(s) = \frac{1}{1+3R_{on}C_S s} = \frac{1}{1+R_{on}(3C_S)s}$$

Considering that during Hold the noise on C_S adds signal-wise to the noise on C_H, and that this is also the output noise caused by source #3, we have



$$V_{out,\#3}^2 = (1+1)^2\frac{kT}{3C_S} = 4\frac{kT}{3C_S}$$



Noise analysis of charge-transfer S&H – II

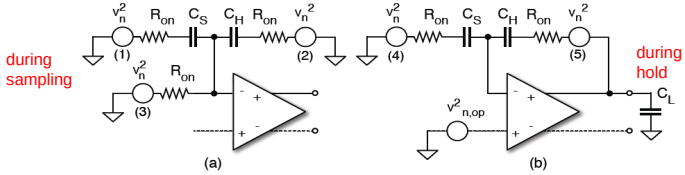
Sampling → noise source #1 (and #2) induces a noise voltage across both C_S and C_H, and noise on C_S is subtracted from noise on C_H during Hold → the relevant transfer function is therefore

$$H_{eq}(s) = H_{C_S}(s) - H_{C_H}(s) = \frac{1}{1+R_{on}(3C_S)s} \quad (\text{if } C_S = C_H)$$

Considering that the noise contributions from #1 and #2 add up power-wise, we obtain

$$V_{out,\#1+2}^2 = (1+1)\frac{kT}{3C_S} = 2\frac{kT}{3C_S}$$

Hold → contributions from #4, #5, and op-amp – #4 is found at the output with gain of -1, band-limited by βf_T (-3dB frequency of feedback loop; $\beta = 1/2$)



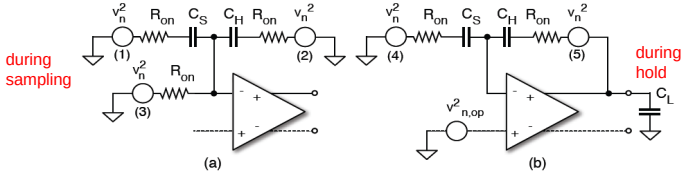
Noise analysis of charge-transfer S&H – III

Noise source #5 appears directly at the output, also limited by βf_T; noise from the op-amp is amplified *x*2, and also limited by βf_T

Overall → assuming the previous expressions for $v_{n,op}^2$ and ω_T, and considering that $\beta = 1/2$, the total noise is

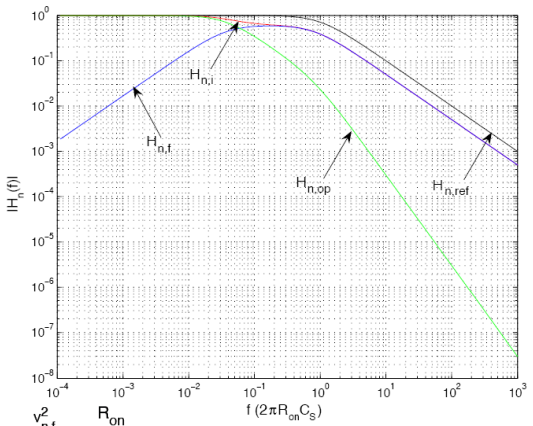
$$V_{n,out,tot}^2 = \frac{4kT}{3C_S} + \frac{2kT}{3C_S} + 2\cdot kTR_{on}\beta\omega_T + 4\frac{\gamma' kT}{g_m}\beta\omega_T$$
$$= \frac{2kT}{C_S} + g_m R_{on}\frac{kT}{C_L} + \frac{2\gamma' kT}{C_L} \approx \frac{2kT}{C_S} + \frac{2\gamma' kT}{C_L}$$

Therefore, for low noise → large capacitances, low-noise op-amp → hardly a surprise!

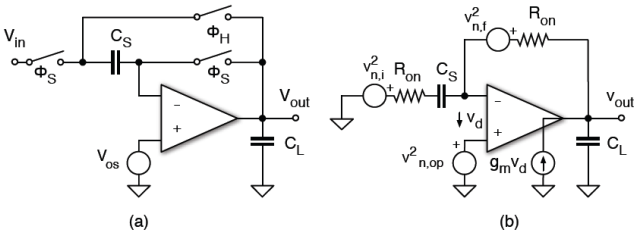


Example 5.3

Wrong picture in the book! The "reference" noise transfer function is that of the $R_{on}C_S$ low-pass filter



offset insensitive flip-around S&H



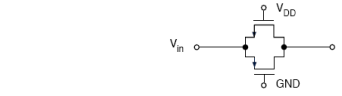
CMOS pass gate

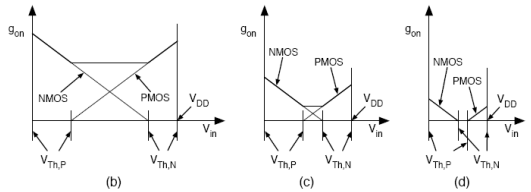
nMOS gate to V_{dd}, pMOS to GND → maximum conductance, given by

$$G_{on} = \beta_n V_{od,n} + \beta_p V_{od,p} \qquad V_{od,n} = V_{dd} - V_{in} - V_{th,n} \qquad V_{od,p} = V_{in} - |V_{th,p}|$$

If $V_{in} \le |V_{th,p}|$, the pMOS conductance goes to zero, as does that of the nMOS for $V_{in} \ge V_{dd} - V_{th,n}$. If $\beta_n = \beta_p$, the conductance when both MOS are on is independent of V_{in}, and equal to

$$G_{on} = \beta_n \left(V_{dd} - V_{th,n} - |V_{th,p}| \right)$$



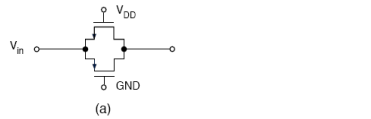


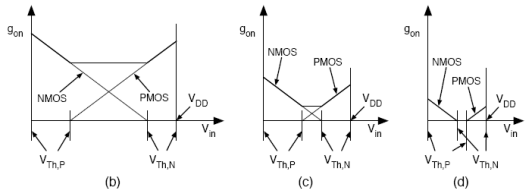
CMOS pass gate – II

This means that the conductance decreases with the supply voltage, and can become zero if

$$V_{dd} \le V_{th,n} + |V_{th,p}|$$

Usually, modern processes offer devices with low V_{th} – however, this increases the cost of the product because of added process steps; it is also possible to use thick-oxide MOS, which allows a (much) higher V_{dd} (double supply voltage required, extra process step)





Switched op-amp technique

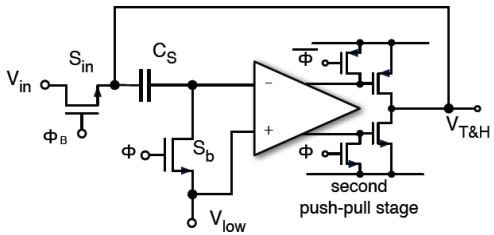
Flip-around S&H

V_{low} is low (close to ground) → no problem driving switch S_b

At the output → the whole output op-amp stage is switched off (i.e., the output impedance becomes very high) at nodes close to V_{dd} and ground → no problem

In this way, C_S can be connected to the input without having to disconnect the OTA with a switch

The only critical element is S_{in}, whose channel must allocate the whole signal range



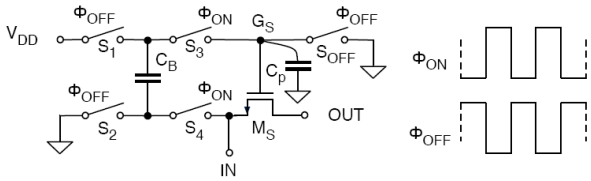
Bootstrapping

In principle, one could generate high gate voltages with a charge pump, but this is (probably) not possible because of strict maximum voltage limitations in today's CMOS processes

Bootstrapping ensure that the gate-to-source and gate-to-drain voltages are always below the allowed limits.

The basic approach is shown below → C_B (charged to V_{dd}) sustains the V_{GS} of the sampling switch M_S through switches S_3 and S_4 during *on*; during *off*, S_{OFF} grounds the gate of M_S, and S_1 and S_2 charge C_B to V_{dd}.
In reality, because of the par. cap. C_p, the voltage at the gate of M_S becomes

$$V_G = (V_{in} + V_{dd})\frac{C_B}{C_p + C_B}$$



Bootstrapping – II

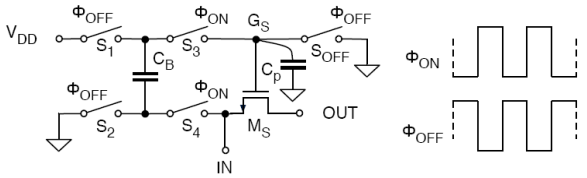
V_{GS} for M_S becomes

$$V_{GS} = V_{dd}\frac{C_B}{C_p + C_B} - V_{in}\frac{C_p}{C_p + C_B}$$

which is below V_{dd} and (almost) input independent – the on-conductance of M_S becomes

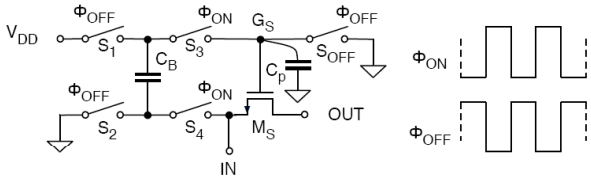
$$G_{on} = \beta\left(V_{dd}\frac{C_B}{C_p + C_B} - V_{in}\frac{C_p}{C_p + C_B} - V_{th}(V_{in})\right)$$

G_{on} is input-dependent mainly through the body effect → good for linearity
Direct-biasing of channel-substrate diodes should be avoided, and protection for drains undergoing large voltage wings should be provided

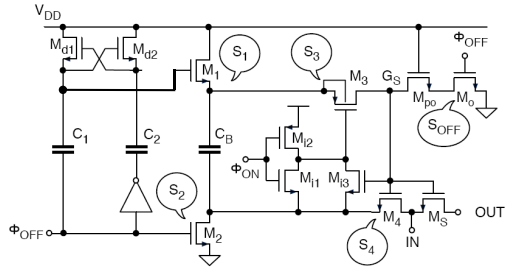


Bootstrapping – III

1) S_1 must be able to switch *on/off* V_{dd}; 2) S_3 must sustain the boosted voltage during *on*; 3) S_4 must operate under the same conditions as the main switch M_S; 4) S_{OFF} must be able to swing between the boosted voltage and zero

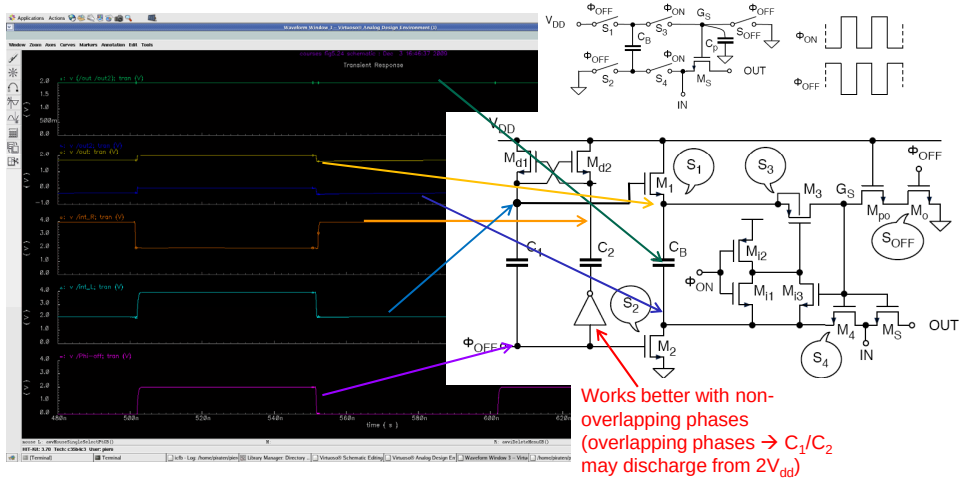


A possible circuital solution is shown below



Bootstrapping – 2×V_{dd} generation

S_1 is nMOS → control of its gate requires a voltage doubler → M_{d1}, M_{d2}, C_1, C_2, Inverter → the gate of M_1 is at $2V_{dd}$ during Φ_{off} and at V_{dd} during Φ_{on} → C_B charges to V_{dd} during Φ_{off} ; M_1 is off during Φ_{on}



Bootstrapping – more features

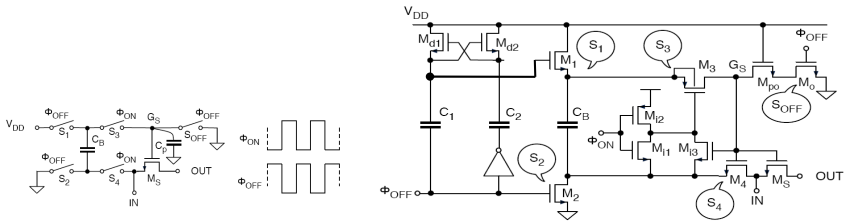
M_{po} reduces the V_{ds} and V_{gd} experienced by M_o during Φ_{off}

Body of M_3 connected to source → no latch-up hazard

M_{i3} ensures that V_{SG3} never exceeds V_{dd} (M_{i1} is cut off when the input voltage *IN* reaches a value for which $\Phi_{on} - IN < V_{th,n}$)

It is easier to implement M1 as an NMOS than as a PMOS, since a PMOS would start conducting during Φ_{on} as soon as $IN + V_{dd} - V_{g,M1}$ ($=V_{dd}$) > $|V_{th,p}|$

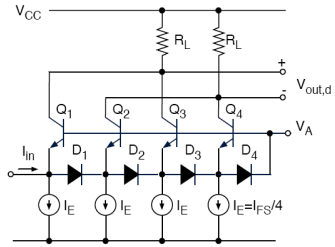
None of the terminal-to-terminal device voltages exceeds V_{dd} for any device



Current folding with BJTs

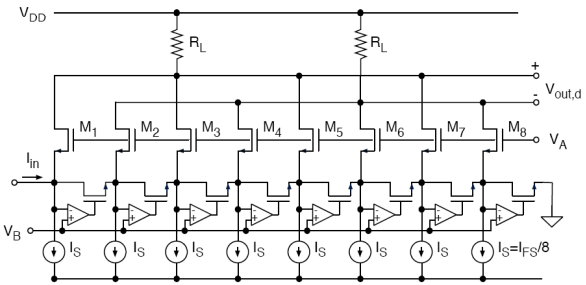
4-segment folding of input current → if I_{in} is zero, two bias currents I_E flow into one branch, two into the other → the diff. output voltage $V_{out,d}$ is zero
If now $0 < I_{in} < I_E$, the current through Q_1 is reduced, and we have $V_{out,d} = R_L I_{in}$
When I_{in} becomes higher than I_E, the current through Q_1 is zero and some current is taken from Q_2, obtaining $V_{out,d} = -R_L I_{in}$; when D_2 becomes active, the output voltage becomes positive again, to return to negative when D_3 is turned on

Notice that the input voltage must increase by one diode voltage for every active cell → dynamic range at input sets the limit to the number of cells



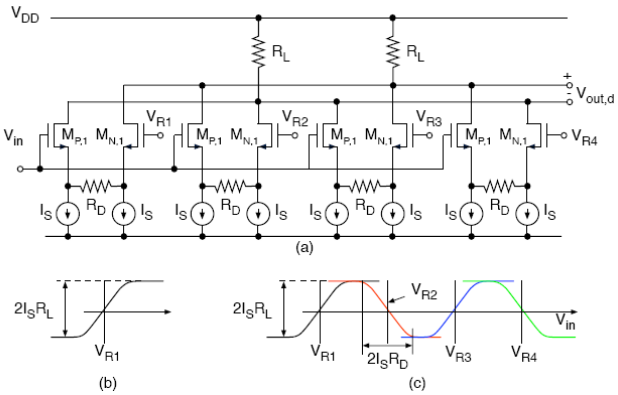
Current folding with MOS

8-segment folding of input current – the use of comparators in more efficient than a diode MOS; the comparator detects an increase of the respective MOS source voltage and turns on the switch – the threshold V_B should be slightly higher than V_A-$V_{tn,h}$ – comparators increase complexity and power consumption, but the voltage drop across the switches is small, and many cells can be cascaded



Voltage folding

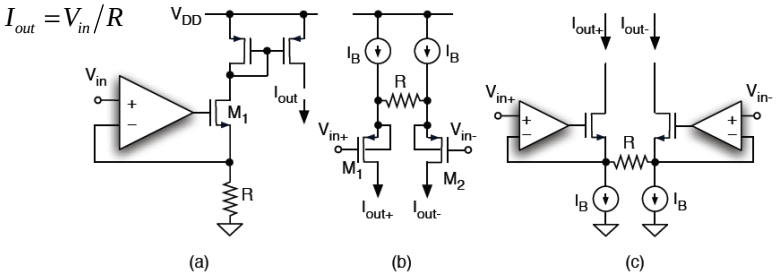
Segments (here: 4) generated by the linear region in the transfer function of a differential pair – $2V_T$ for BJT, $2V_{od}$ for MOS – too small → extended with degeneration resistors by as much as $2I_S R_D$, as the diff. pair becomes fully unbalanced for an input voltage of $\pm(I_S R_D + V_{od})$ → the differential output voltage changes by $\pm 2 I_S R_L$



Voltage-to-current conversion

(a): cascoding is often needed; can be simplified as in (b), where pMOS are used to avoid the body effect; however, the g_m of the transistors should be much higher than 1/R; further, it is less linear, although the differential circuits cancels some non-linearity. (c): g_m is amplified by the op-amp gain (body effect reduced by the same amount)

$$I_{out} = V_{in}/R \qquad I_{out,diff} = (V_{in+} - V_{in-})/R$$



Example 5.4

±0.5V input range, I_B=1mA, V_{od}=400mV → determine R for SFDR=85dB and SFDR=95dB

The large-signal resistance is $R_T = R + \frac{V_{od}}{2(I_B + I_{out})} + \frac{V_{od}}{2(I_B - I_{out})} = R + \frac{V_{od} I_B}{I_B^2 - I_{out}^2}$

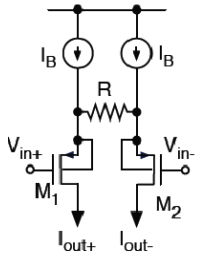
The differential input determines (implicitly) the output current as

$$\Delta V_{in} = R I_{out} + \frac{V_{od} I_B I_{out}}{I_B^2 - I_{out}^2}$$

from which we obtain $I_{out} \approx k_1 \Delta V_{in} + k_3 \Delta V_{in}^3 + k_5 \Delta V_{in}^5 + k_7 \Delta V_{in}^7 + \ldots$, and

$$SFDR \approx \frac{k_1 \Delta V_{in}}{\frac{1}{4} k_3 \Delta V_{in}^3} = \frac{4 k_1}{k_3 \Delta V_{in}^2}$$

For the above SFDR requirements, we need R=12.5kΩ and 18.5kΩ, respectively



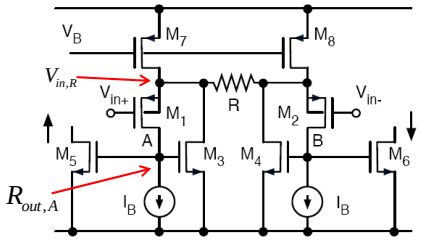
Improved V-I conversion

Current through M_1 (M_2) kept constant by feedback, together with avoidance of body effect → V_{in+} (V_{in-}) is copied at the source of M_1 (M_2) → the signal current flows into M_3 (M_4) , and copied to the output by M_5 (M_6)

More precisely: $V_{in,R} \approx V_{in+} \frac{-\beta A}{1-\beta A}$, where βA is the loop gain of the feedback:

$$\beta A \approx -g_{m3} \frac{g_{m1}}{g_{m1} + 2/R + g_{ds3} + g_{ds7}} R_{out,A} \approx -g_{m3} R_{out,A} \frac{g_{m1}}{g_{m1} + 2/R}$$

A loop gain of 30-40dB is possible → linearity improvement sufficient in many applications



Generation of clock phases

Usually, at least two non-overlapping (to avoid charge leakage) phases are needed (overlapping may be needed e.g. to keep feedback during phase transition)

NOR based → non-overlapping; NAND-based → overlapping, need one more inversion for non-overlapping

Non-overlap time → three inverter delays