Data Converters

Nyquist-rate D/A Converters

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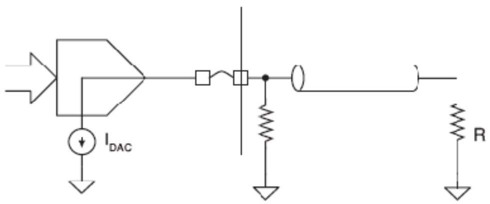
Overview

- Introduction
- Type of converters
- Architectures based on resistors
- Architectures based on capacitors
- Architectures based on current sources
- Other architectures

Introduction

The input of a DAC is a multi-bit digital signal, while the output is a voltage or a current capable of driving an external load



Often a current is used to drive an off-chip coaxial cable to yield a voltage across the terminations

Introduction (II)

- Many DACs use integrated resistance or capacitances to attenuate (or amplify) the reference
- A careful layout design (common-centroid, dummy components, temperature-insensitive, etc) leads to matching accuracies in the order of 0.02-0.1% → resolutions up to 60-70dB are possible without trimming of analog passive components, and without using digital correction or digital calibration
- Use of analog CMOS switches → low on-resistance, high speed of switching, minimum side effects
  - Natural in CMOS processes (MOS device is a better switch than transistor)
  - Complementary MOS or bootstrapped nMOS (gate voltage is a shifted-up replica of the signal to be switched)
  - Control of clock feedthrough (MOS channel charge flowing to D/S when the gate control goes off)

DAC applications

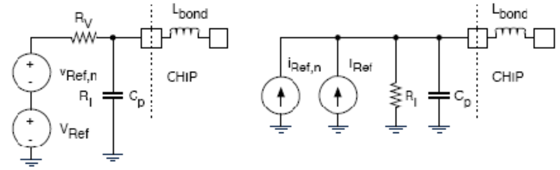
- Video: HDTV monitors display more than 1000 lines per frame, in addition to a higher contrast ratio and a more detailed color range
  - To maximize the viewing quality on a state-of-the-art display, a 12-bit 150 MSPS conversion rate are often necessary
- Wired: DACs for ADSL and ADSL2+ must handle signal bands of 1.1MHz or 2.2MHz with 12-bit resolution
- Wireless: UMTS, CDMA2000, GSM/EDGE require high conversion rates and high resolutions when multiple carriers are used
  - Conversion rates of 200-1000 MSPS and 12-16 bits of resolution may be necessary
- Audio: typically, 16 bits or more to headphones/speakers, with a conversion rate of 44 kSPS

Voltage and current references

Voltage and current references can be either generated inside the chip, or provided via an external pin

Any error affecting the references limits the overall system performance → should be constant independently of PVT variations, load, and time

Static errors are usually irrelevant; dynamic errors are much more important → speed and linearity are affected



The noise level must be well below the quantization floor:

$$v_{Ref,n}^2 << \frac{v_{FS}^2}{6 \cdot 2^N f_s} \quad \text{or} \quad i_{Ref,n}^2 << \frac{I_{FS}^2}{6 \cdot 2^N f_s}$$

Reference noise – an example

The request on the noise floor of the reference becomes very challenging for resolutions above 14 bits: if I_{FS}=20mA, the noise spectrum of the current reference must be below 0.79nA/sqrt(Hz), which, across 50Ω, results in a noise voltage density of 39.5nV/sqrt(Hz) (fairly low)

As a comparison, the spectral density of the input-referred noise of a MOS transistor is

$$v_n^2 / \Delta f = 4kT\gamma / g_m$$

and even a single transistor with $g_m = 0.2mA/V$ gives rise to a noise voltage density as large as

$$v_n = 7.4nV/\sqrt{Hz}$$

Types of converters

The basic components used in a DAC architecture normally classify the DAC. We distinguish between:

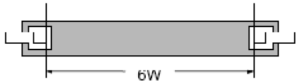
- Architectures based on resistors
- Architectures based on capacitors
- Architectures based on current sources

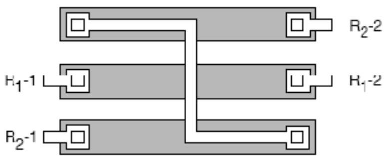
Resistor based

Strips of resistive layers with a given specific resistance, $\rho_{\square}$. The effective number of squares, $(L/W)_{eff}$, and the contact resistance R_{cont} give the total resistance value ($\rho_{\square}$ ranges from a few Ω/□ to kΩ/□)

$$R = \rho_{\square}\left(\frac{W}{L}\right)_{eff} + 2R_{cont}$$

2:1 matching (no dummies, metal-R neglected)

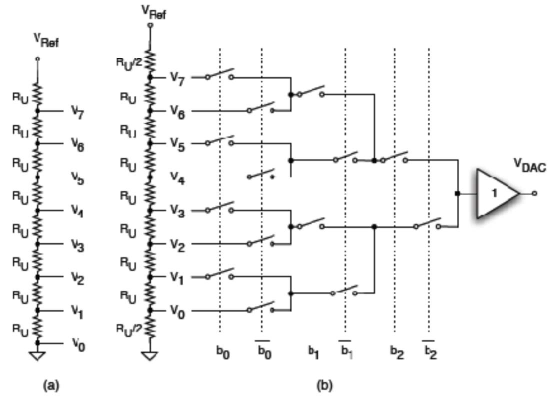




Absolute R-value only important for power and area consumption; relative value (matching) is what really counts

Resistive divider

Resistive (Kelvin) divider, invented by Lord Kelvin in the 18th century



Resistive divider (II)

2^3 equal resistor, R_U, generate 8 discrete analog voltages

$$V_i = V_{\mathrm{ref}}\,\frac{i}{8} \qquad i = 0 \ldots 7$$

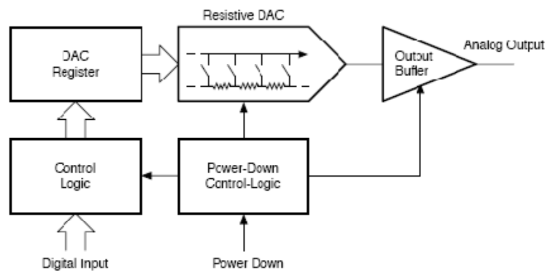
The resistive divider in (b) shifts the voltages by ½ LSB ($V_{ref}/2^{n+1}$) by moving ½ unit resistance from the top to the bottom of the divider.

The selection of a voltage is done by a tree of switches whose state is controlled by a digital input – however, there are *n* switches between ladder and buffer → RC delay

The buffer provides a very high input impedance, performing a voltage measurement, and a very low output impedance for adequate driving of the DAC load

Unary selection

Only one switch on the divider-to-buffer path, but many control lines

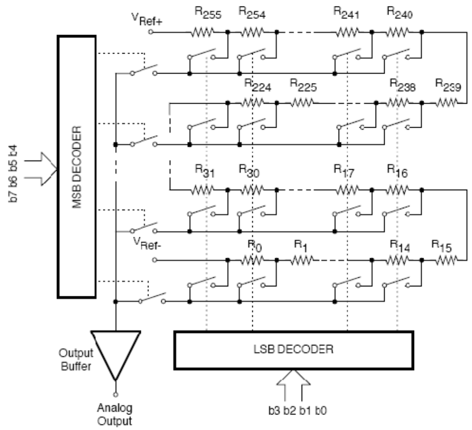


The decoding method used to select the divider voltage depends on a trade-off between speed, complexity, and power consumption

Matrix selection

A limit to the ladder DAC is set by the number of switches/control-lines (2^n) required. The matrix approach reduces the complexity to $2 \cdot 2^{n/2}$, however with two switches in series

In this example, n=8, the DAC is partitioned in 4 MSBs (rows) and 4 LSBs columns)



Settling of the output voltage

Assume the speed of the buffer very large → the voltage at the input and output of the buffer depends only on the divider, approximated by an RC time constant. If the output *k* is selected, then

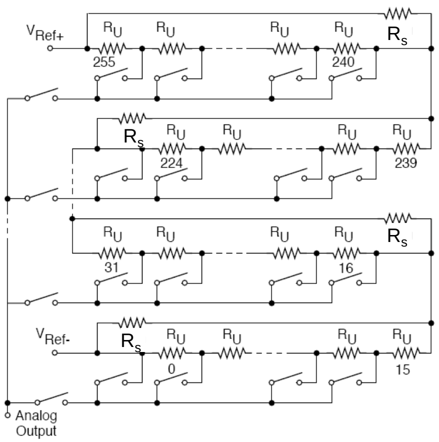
$$R_{eq} = \frac{(k-1)R_U \cdot (2^N - k + 1)R_U}{(k-1)R_U + (2^N - k + 1)R_U} + N_{on}R_{on} = \frac{(k-1)(2^N - k + 1)}{2^N} R_U + N_{on}R_{on}$$

$$C_{in} = C_{in,B} + N_{on}C_{p,on} + N_{off}C_{p,off}$$

$C_{in,B}$ is the input capacitance of the buffer; N_{on} and N_{off} are *on* and *off* switches connected to the buffer input (their number is constant); and $C_{p,on} \approx C_{p,off}$ are the associated parasitic capacitances

C_{in} is almost constant, R_{eq} depends on the selected tap (parabolic, maximum at mid-point) → signal-dependent time constant → distortion!! → unit resistor should be small enough

X-Y selection with shunt resistances

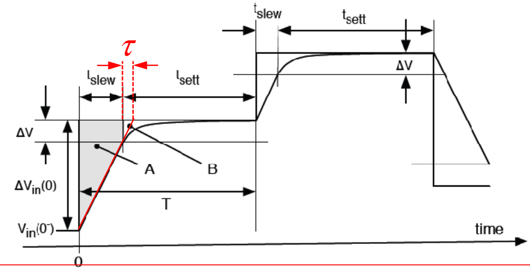


R_S in parallel to *k* R_U units: higher speed, but also higher power consumption; for each line, the equivalent resistance is

$$R_{eq}(t) = kR_U \parallel R_S = \frac{kR_U R_S}{kR_U + R_S}$$

Settling of the output voltage

If slew-rate and bandwidth of the buffer matter (disregarding RC from divider): assume input step $\Delta V_{in}(0)$:



From continuity of first derivative

$$V_{out}(t) = V_{in}(0^-) + SR \cdot t \qquad \text{for} \quad t < t_{slew}$$

$$V_{out}(t) = V_{in}(0^-) + \Delta V_{in}(0) - \Delta V \cdot e^{-(t - t_{slew})/\tau} \qquad \text{for} \quad t > t_{slew}$$

$$\Delta V / \tau = SR \qquad \tau = 1/2\pi\beta f_T \qquad t_{slew} = \frac{\Delta V_{in}(0)}{SR} - \tau$$

β = feedback factor; f_T = unit gain frequency of op-amp

Settling of the output voltage (II)

Non-linear combination of linear ramp and exponential ramp

Reconstruction filter yields the time average of the output waveform → average of non-linear error causes distortion

If the settling time is long enough, the integrated error during the slewing period (area A in figure) is

$$\frac{1}{2}\left(\frac{\Delta V_{in}}{SR} - \Delta V\right) t_{slew} + \Delta V \cdot t_{slew} = \frac{1}{2}\left(\frac{\Delta V_{in}^2}{SR} - SR \cdot \tau^2\right)$$

while during the settling period is

$$\Delta V_{in} \cdot \tau$$

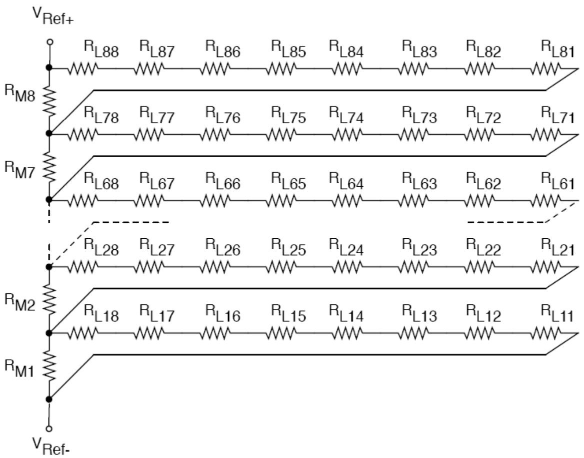
In both cases, it is signal dependent → distortion may be an issue
For a quantitative estimate of distortion, a transistor-level simulation is required

Remarks on linearity

- If linearity is an important issue, remember:
  - A code-dependent settling of the output causes distortion
  - A high SFDR requires a low resistance at every node → the variation of the settling time must be much smaller than the hold period

Segmented resistive DAC – principle

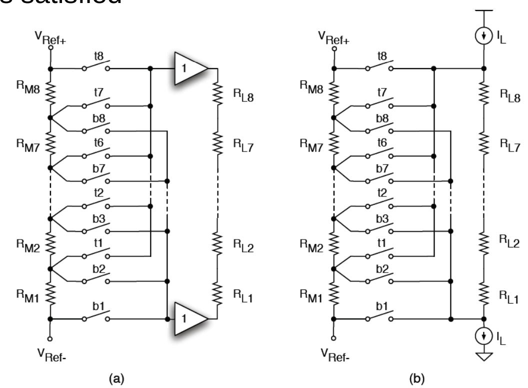
The use of shunting resistors has generated an auxiliary *n/2*-bit DAC → evolution: segmentation achieves a high-resolution DAC by combining the operation of two or more DACs (3+3 bits in DAC below: cascade of 3-bit MSB DAC + eight 3-bit LSB DACs)



Segmented DAC

Only one LSB DAC is in fact needed – buffers must have the same offsets, high input impedance and low output impedance, and an input common-mode range of V_{ref}

It is also possible to replace buffers with current sources: there is no current flowing from LSB DAC to MSB DAC if the equation on the right is satisfied



$$I_L = \frac{\Delta V_{LSB}}{2^{n_{LSB}} R_L} = \frac{V_{ref+} - V_{ref-}}{2^{n_{MSB}} 2^{n_{LSB}} R_L}$$

Effect of mismatch

The i^{th} resistance is

$$R_i = R_u(1+\varepsilon_a)(1+\varepsilon_{r,i})$$

where ε_a is the absolute error, and $\varepsilon_{r,i}$ is the relative mismatch. Voltage at tap *k* is

$$V_{out}(k) = V_{ref}\frac{\sum_0^k R_i}{\sum_0^{2^{n-1}} R_i} \qquad k = 0 \ldots 2^n - 1$$

and is of course independent of ε_a:

$$V_{out}(k) = V_{ref}\frac{k + \sum_0^k \varepsilon_{r,i}}{2^{n-1} + \sum_0^{2^{n-1}} \varepsilon_{r,i}} \qquad k = 0 \ldots 2^n - 1$$

The error depends on the accumulation of mismatches and is zero at the two endings of the string

Mismatch with linear gradient

A straight string with unity elements spaced by ΔX and gradient α in their relative values gives

$$R_k = R_0(1 + k\alpha\Delta X) \qquad k = 0 \ldots 2^n - 1$$

and the output at the tap *k* becomes

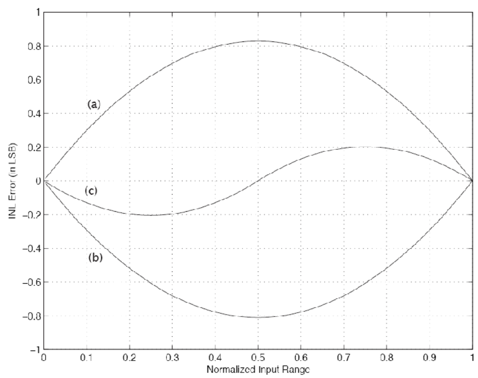
$$V_{out}(k) = V_{ref}\frac{k + \alpha\Delta X \cdot k(k+1)/2}{2^n - 1 + \alpha\Delta X \cdot (2^n - 1)2^n/2}$$

→ parabolic with initial value 0 and final value V_{ref}

INL with linear gradient: straight and folded line

Recall that $INL(k) = V_{out}(k) - \overline{V_{out}(k)}$. Curves (a) and (b) show the INL for $\alpha\Delta x = \pm 10^{-4}$, and result in a maximum INL of ±0.8LSB

If the divider layout is folded around the mid-point, then the mid-point voltage is correct; for the same value of the gradient, the maximum INL becomes ±0.2LSB, curve (c). Careful layouts are generally required



Example

Harmonic distortion caused by a linear gradient:

Consider a gradient $\alpha = 2.5 \cdot 10^{-5}/\mu$ in the resistivity of a straight string of resistors spaced by ΔX=4μ. The DAC is a resistive-string divider connected between 0V and 1V.

The FFT of an input sequence made of 2^{12} points gives a noise floor for an 8-bit DAC at

$$n_Q = -1.78 - 6.02 \cdot 8 - 10\log(2^{12}/2) = -83\text{dBc}$$

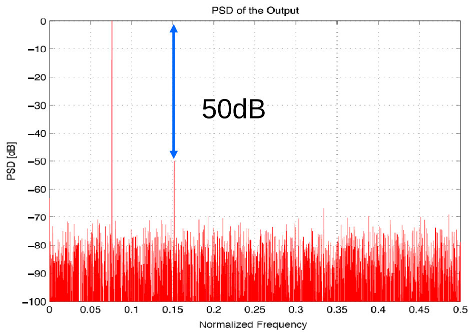
which is enough for detecting spurs higher than -65dBc (18dB above the noise floor)

Simulations/calculations

$$V_{in} \approx V_{ref}\frac{k}{2^n} \quad \text{and} \quad V_{out}(k) = V_{ref}\frac{k+\alpha\Delta X\cdot k(k+1)/2}{2^n-1+\alpha\Delta X\cdot(2^n-1)2^n/2} \rightarrow$$

$$V_{out}(k) \approx \frac{2^n\left[V_{in}(1+\alpha\Delta X/2)+V_{in}^2\cdot 2^n\alpha\Delta X/(2V_{ref})\right]}{2^n-1+\alpha\Delta X\cdot(2^n-1)2^n/2}$$

$$\approx V_{in}(1+\alpha\Delta X/2)+V_{in}^2\cdot 2^n\alpha\Delta X/(2V_{ref})$$



$$\left[\sin^2(\omega t) = \frac{1}{2}(1-\cos(2\omega t))\right]$$

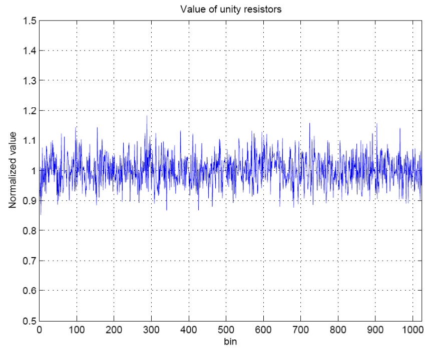
$$\frac{A_{2nd}}{A_{fund}} \approx \frac{V_{in}^2\cdot 2^n\alpha\Delta X/(4V_{ref})}{V_{in}}$$

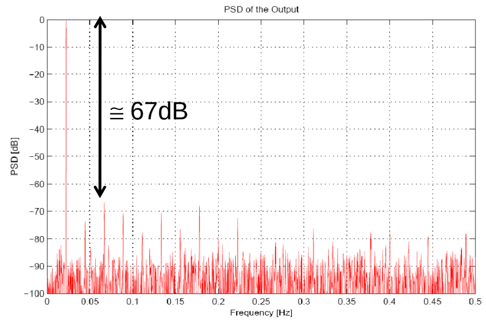
If $V_{in} = V_{in,\max} = V_{ref}/2$, then

$$\frac{A_{2nd}}{A_{fund}} = \frac{2.5\cdot 10^{-5}\cdot 4\cdot 2^8}{8} = 0.0032 = -49.9dB$$

Effect of random mismatch on resistors

Even if the resistor variations are as high as 10%, but they are not correlated → noise floor is increased, but very small distortion (DNL is high, but INL is very low)





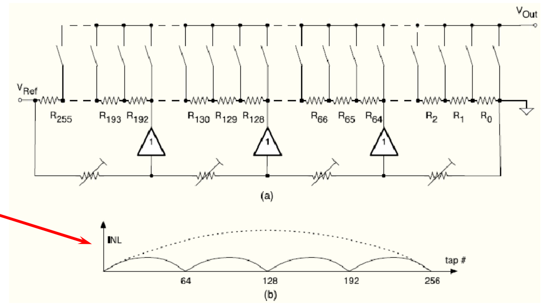
Trimming and calibration

- Mismatch effects are often investigated with Monte Carlo simulations
- Trimming corrects statically the mismatches caused by inaccuracies in the fabrication process
- Thin-film technologies that realize resistors on top of the passivation layer of the IC are particularly suitable; resistors are trimmed very accurately with a laser
- Use of fuses or anti-fuses for respectively opening or closing the interconnections of a network of resistive elements
  - Connection with fuses or anti-fuses is done during testing (either before or after packaging) and is permanent

Calibration

- Switches turned on or off at power-on (off-line calibration) or during the normal operation of the converter (without interfering, on-line calibration)
- Calibration is not permanent → can compensate for slow drift, like aging or (for on-line) temperature effects
- Correction at the group level instead than correcting all the elements

INL improvement with 3-point calibration of 8-bit DAC



Alternative approach: digital potentiometer

- Slight variation of the resistive ladder topology
- Same functionality as the conventional potentiometer, except that the wiper terminal is controlled by a digital signal, so only discrete steps are allowed
- Selection of the wiper position controlled via an *n*-bit register value
- Communication and control of the device can be supported by a parallel or serial interface
- Volatile or non-volatile logic to retain the wiper setting. For volatile logic, the wiper is normally set at mid-range at power-up

R-2R resistor ladder DAC

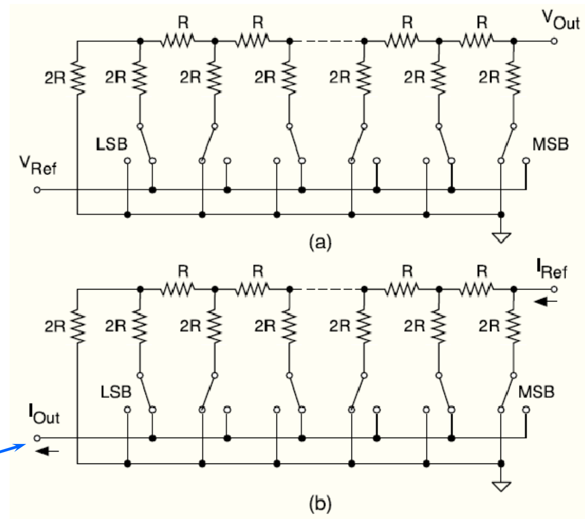
Reduces the total number of resistors from 2^n to (2+1)n = 3n

The resistance to the left of every node is 2R!

voltage mode

current mode

virtual ground



Voltage mode

It can be verified that connecting the k^{th} switch to V_{ref} leads to a contribution

$$V_{out} = V_{ref} / 2^k$$

The output of the R-2R ladder in the voltage mode is the superposition of terms that are the successive divisions of V_{ref} by 2

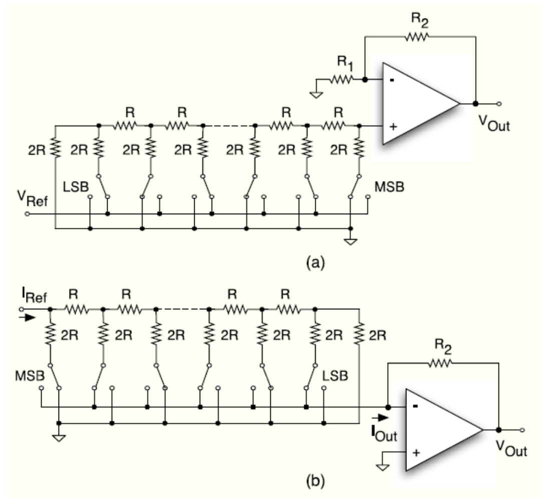
$$V_{out} = \frac{V_{ref}}{2} b_{n-1} + \frac{V_{ref}}{4} b_{n-2} + \ldots + \frac{V_{ref}}{2^{n-1}} b_1 + \frac{V_{ref}}{2^n} b_0$$

which is the DAC conversion of the digital input

R-2R resistor ladder with buffer

voltage mode

current mode



Limits of R-2R resistor ladder

- About the output resistance of the reference source: the load seen by the voltage ref. source is code-dependent → this may cause harmonic distortion → use reference generators whose output impedance is much lower than the load in any case
- About the R-2R algorithm: the input-output characteristics of the R-2R ladder (either voltage or current mode) is NOT intrinsically monotonic (as it was for the resistive ladder)
  - This is because in the R-2R ladder an increment by an LSB switches the connection in all those arms whose control bit changes → because of random mismatches, it may happend that an increase by 1 switches off a contribution whose value is higher than the amount that is switched on → worst case is at midpoint

Current mode

The current-mode circuit performs a successive division-by-2 of the reference current I_{ref}, provided that the voltage at the output node is (virtual) ground

The superposition of the currents selected by the switches yields the output current

$$I_{out} = \frac{I_{ref}}{2} b_{n-1} + \frac{I_{ref}}{4} b_{n-2} + \ldots + \frac{I_{ref}}{2^{n-1}} b_1 + \frac{I_{ref}}{2^n} b_0$$

- The parasitic capacitance of the switched node remains at the same voltage (analog ground or virtual ground) independently of the code (desirable: faster switching, linear)
- Glitches (because of large switched currents) may affect the dynamic response of the current-mode R-2R (undesirable, of course)

Current mismatches

Mismatch is problematic in the current-mode circuit as well, as an error in the binary division can cause non-monotonicity

Consider the switching at mid scale: $I_{ref}\left(1/2 - 1/2^n\right) \rightarrow I_{ref}/2$

If, because of mismatches, the MSB current is $I_{ref}(1-\varepsilon)/2$, the mid-scale transistion becomes

$$I_{ref}\left(1/2 - 1/2^n\right) \rightarrow I_{ref}(1-\varepsilon)/2$$

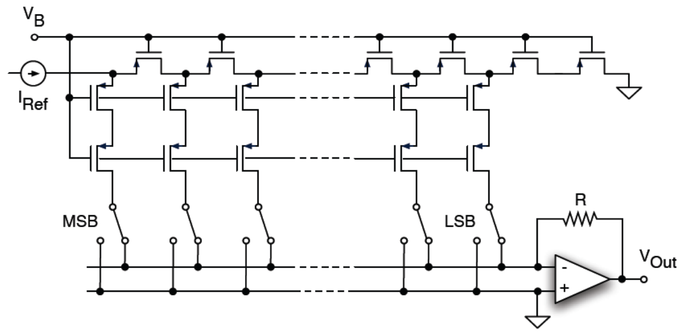
The step amplitude is $\Delta I \approx I_{ref}\left(-\varepsilon/2 + 1/2^n\right)$

If $\varepsilon > 1/2^{n-1}$ the step amplitude is negative, and the transfer function becomes non-monotonic

Replacing resistors with MOS

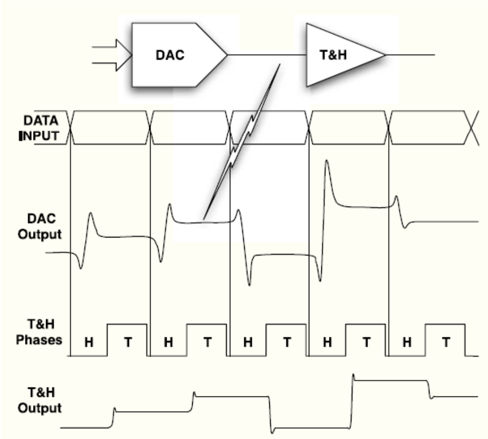
For medium accuracy, area can be saved by replacing passive resistors with MOS devices, as in the current-mode ladder below.

Observe that two equal parallel MOS networks divide the input current into two equal parts regardless of the non-linear response of the single element, as long as the two networks operate at the same (non-linear) point.

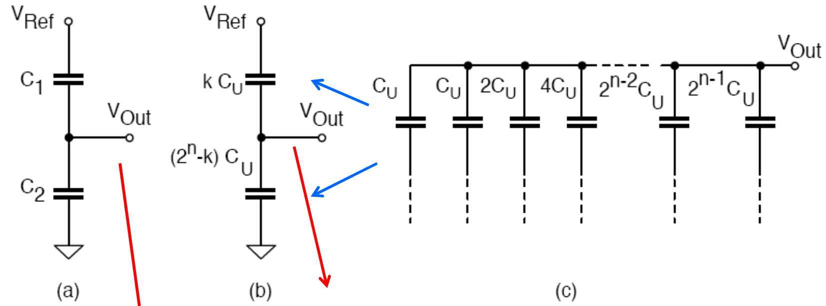


Deglitching

A track-and-hold (T&H) after the DAC can highly improve the performance removing the glitches. However, the linearity of the T&H must be at least 10dB higher than DAC, which may be difficult to obtain



Capacitive divider DAC

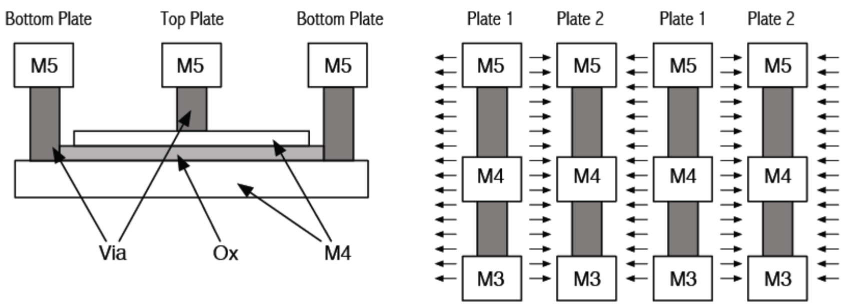


$$V_{out} = V_{ref} \frac{C_1}{C_1 + C_2}$$

$$V_{out} = V_{ref} \frac{k}{2^n}$$

Integrated capacitors

Capacitors may be implemented with parallel plates (poly-oxide-poly, metal-insulator-metal (MIM)), or with vertical plates (see right), which yields denser capacitors in modern fine-line processes with up to 10 different metal levels



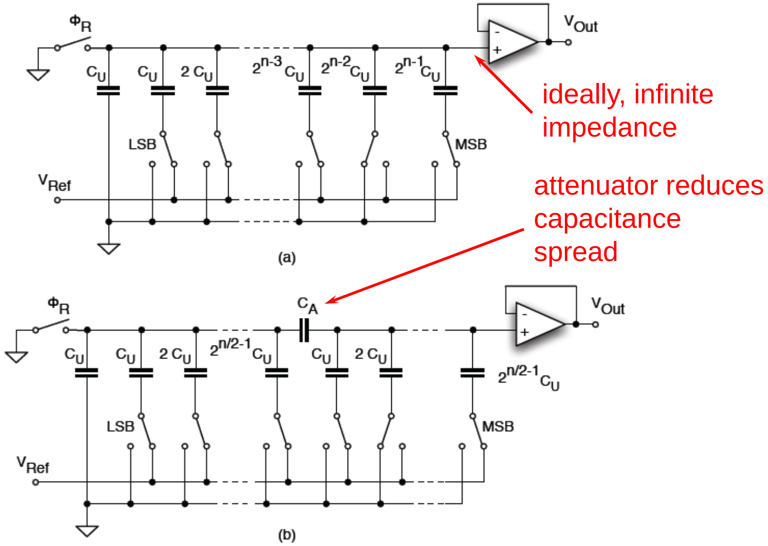
Parasitic limitations

- The parasitic capacitances connected to V_{ref} or ground receive the required charge by low-impedance nodes (good)
- The parasitic capacitances connected to the output node change the output voltage (bad)
- If the parasitic capacitances are independent of the output voltage, only a gain error is introduced (good)

$$V_{out} = V_{ref} \frac{\sum_1^n b_i C_i}{\sum_0^n C_i + \sum_0^n C_{p,i}}$$

- Non-linear parasitic capacitances that change with the output voltage cause harmonic distortion (bad)

N-bit capacitor-divider DAC



Attenuation capacitor

The attenuation capacitor C_A reduces the capacitor count

The largest element in the right array is $2^{\frac{n}{2}-1}C_U$ instead of $2^{n-1}C_U$

The total capacitance drops from $2^n C_U$ to $\left(2\cdot 2^{n/2}-1\right)C_U$

The value of C_A is found by considering that C_A in series with the left array must yield C_U:

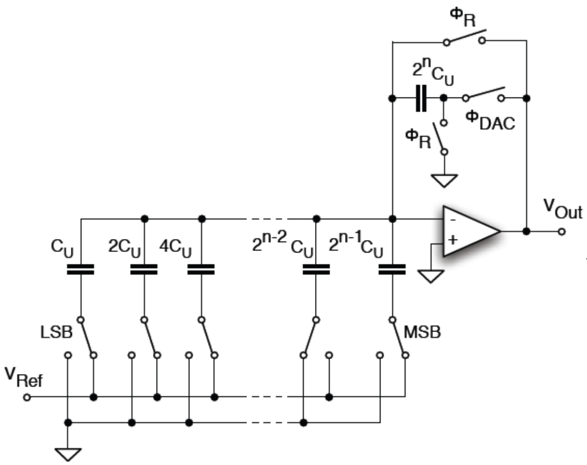
$$\frac{C_A\cdot 2^{\frac{n}{2}}C_U}{C_A+2^{\frac{n}{2}}C_U}=C_U$$

yielding $C_A=\dfrac{2^{\frac{n}{2}}}{2^{\frac{n}{2}}-1}C_U$

Unfortunately, the value of C_A is a fraction of C_U : obtaining the desired accuracy requires a great deal of care in the layout; furthermore, C_A is floating, and its bottom-plate capacitance is in parallel to the left array

Capacitive multiplying DAC (MDAC)

Avoids the demands on large input dynamic range for the op-amp (and performs offset cancellation as well)

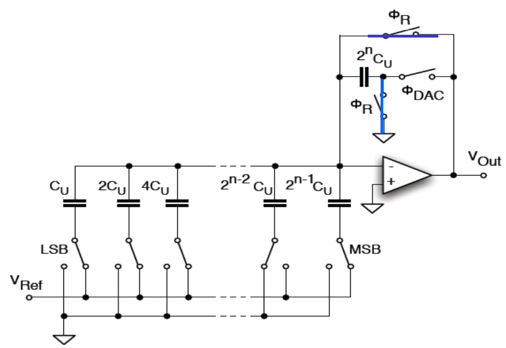


$$V_{out}=-\frac{\sum_0^{n-1}b_i2^iC_U}{2^nC_U}$$

Offset cancellation in MDAC

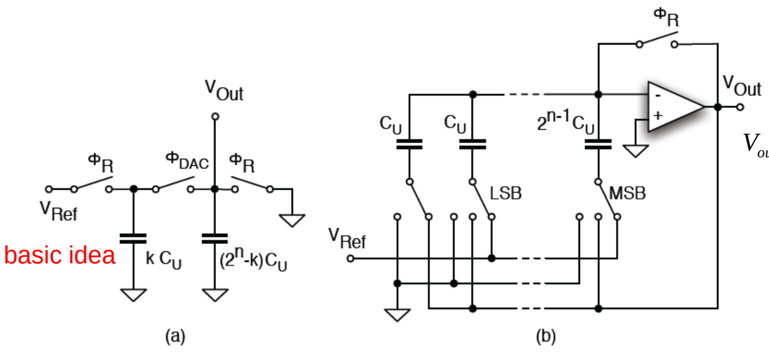
During the reset phase, the op-amp is connected as a feedack unity buffer, and the offset voltage is loaded onto the feedback capacitance and all other capacitances. During the active phase, the offset is effectively cancelled from the output.

However, the feedback factor is ½ during the active phase and 1 during reset, complicating the frequency compensation of the DAC.



Flip-around MDAC

The previous MDAC has as many as $2^{n+1}-1$ C$_U$. The "flip-around" MDAC has only half as many, by charging k capacitors to V$_{ref}$ -V$_{off}$ (all others to -V$_{off}$) during Φ_R and then connecting them in parallel to the other 2^n-k capacitors. During the active phase, all caps are tied together and connected to the output, performing charge sharing. Top-plate parasitics are discharged and then kept to virtual ground, while bottom-plate parasitic caps are driven by voltage sources.



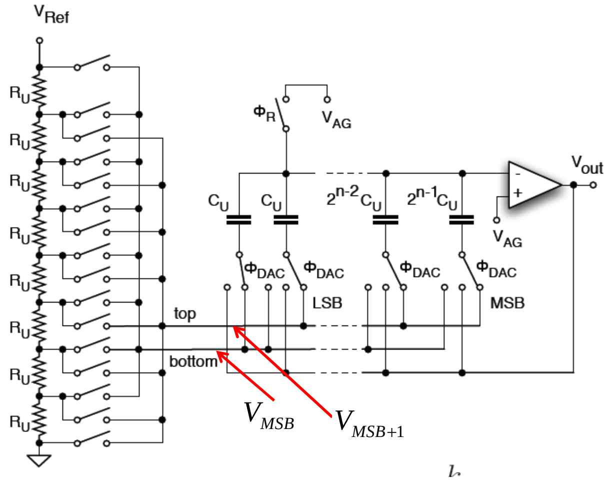
$$V_{out} = V_{ref}\frac{kC_U}{2^n C_U}$$

A reminder

- Any capacitor-based DAC architecture requires a reset phase to make sure that the capacitor array is initially discharged
- The output is not valid during reset → a track and hold is required to sustain the output during reset

Hybrid capacitive-resistive DAC

Resistance ladder implements the MSB conversion (3 bits here) while the capacitive flip-around DAC performs the LSB conversion (n bits)



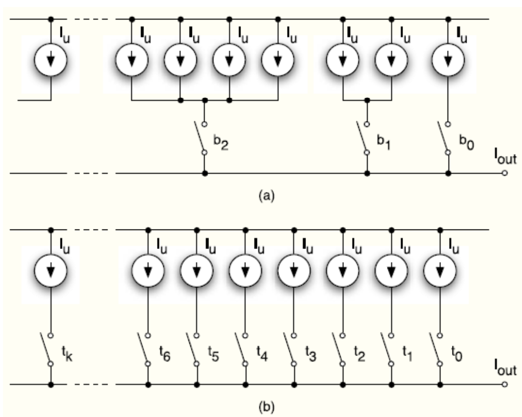
$$V_{out} = V_{MSB} + \Delta_{MSB}\frac{k}{2^n}$$

LSB

Current-based DAC

k currents out of 2^n-1 are steered toward the output node, obtaining, as usual

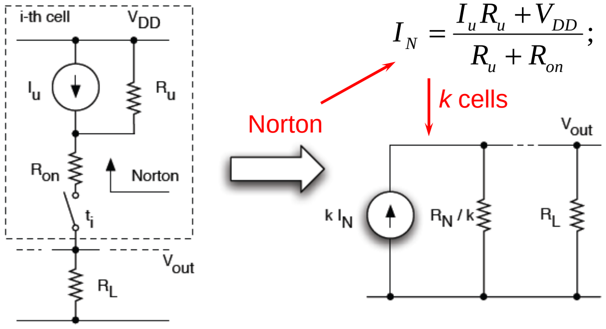
$$I_{out} = I_u\left(b_0 + 2b_1 + 2^2 b_2 + \ldots + 2^{n-1}b_{n-1}\right)$$



binary weighted

unary weighted

Simplified model of single current cell



$$I_N = \frac{I_u R_u + V_{DD}}{R_u + R_{on}}; \qquad R_N = R_u + R_{on}$$

$$V_{out} = kI_N \frac{R_L \cdot R_N/k}{R_L + R_N/k} = I_N R_L \frac{k}{1+\alpha k}; \qquad \alpha = \frac{R_L}{R_N}$$

V_{out} depends non-linearly on k, i.e. on the signal
→ distortion!

Distortion

$$V_{out,max} = I_N R_L \frac{2^n - 1}{1+\alpha\left(2^n-1\right)}; \qquad V_{out,max,nom} = I_N R_L \left(2^n - 1\right)$$

The endpoint-fit INL measured in LSBs is then

$$INL(k) = \frac{X'(k)\dfrac{V_{out,max,nom}}{V_{out,max}} - X(k)}{I_N R_L} = \frac{k\left(1+\alpha\left(2^n-1\right)\right)}{1+\alpha k} - k; \qquad k = 0 \ldots 2^n - 1$$

Its maximum is at mid-scale, and is approximately $INL_{max} = \alpha \cdot 2^{2n-2}$

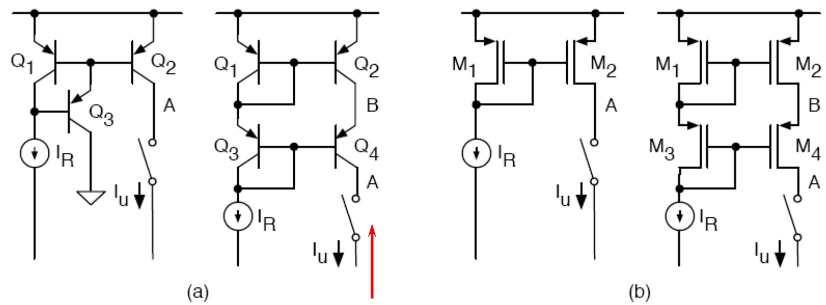
$$INL < 1LSB \;\rightarrow\; R_u > R_L \cdot 2^{2n-2};\;\; \text{if } R_L = 25\Omega,\;\; n = 12 \;\rightarrow\; R_u > 100M\Omega$$

If we have a full-scale sinusoidal input with amplitude $k_p = 2^{n-1}$, the fundamental output harmonic has amplitude $I_N R_L k_p$, while the 2nd harmonics has amplitude $I_N R_L \alpha k_p^2/4$, resulting in an SDR of $R_L/R_u \cdot 2^n/4$. With the above values, SDR=-72dB

To summarize

- The output resistance of the unity current source causes second-order harmonic distortion
- The use of differential architectures eliminates (ideally) all even-order distortion, relaxing the requirements on the unit current source
- A load resistance (coaxial cable) is only needed for very high speed applications; for lower speeds, op-amps can be used to present a virtual ground to the DAC, again much relaxing the requirements on the output impedance of the current sources

Unity current generator (BJT and MOS)



$$R_{out} = r_{ds2}\left(g_{m4} r_{ds4}\right)$$

- Using current sources with high output resistance secures linearity at low frequencies – at high frequencies, parasitic (non-linear) capacitances dominate
- In general, complex schemes reduce the speed of operation

Random mismatch in current mirrors

$$I_D = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2; \quad \beta = \mu C_{ox}\frac{W}{L}$$

Assume mismatches on β and V_{th}:

$$I_1 = \bar{I}\left(1 + \frac{\Delta\beta}{\beta} + \frac{2\Delta V_{th}}{V_{gs} - V_{th}}\right) \qquad I_2 = \bar{I}\left(1 - \frac{\Delta\beta}{\beta} - \frac{2\Delta V_{th}}{V_{gs} - V_{th}}\right)$$

Assume Δβ and ΔV_{th} are uncorrelated → the total error becomes

$$\frac{\Delta I^2}{I^2} = \frac{\Delta\beta^2}{\beta^2} + \frac{4\Delta V_{th}^2}{\left(V_{gs} - V_{th}\right)^2} \quad \text{with} \quad \frac{\Delta\beta^2}{\beta^2} = \frac{A_\beta^2}{WL}; \quad \Delta V_{th}^2 = \frac{A_{V_{th}}^2}{WL}$$

A_β and $A_{V_{th}}$ are process constants; to halve the error, the device area must increase 4 times

Example – scaling of transistor size

The required ΔI/I (for a given yield) for a 12-bit current-steering DAC is 0.3%; μC_{ox} is 39μA/V², the unit current I_U is 4.88μA; A_{Vth} is 2mV·μ and A_β is 0.3%·μ. Plot ΔI/I as a function of the MOS area. Estimate the MOS size for an a gate overdrive of 0.4V

$$(WL)_{\min} = \left(A_\beta^2 + \frac{4A_{V_{th}}^2}{\left(V_{gs} - V_{th}\right)^2}\right) \Bigg/ \frac{\Delta I^2}{I^2}$$

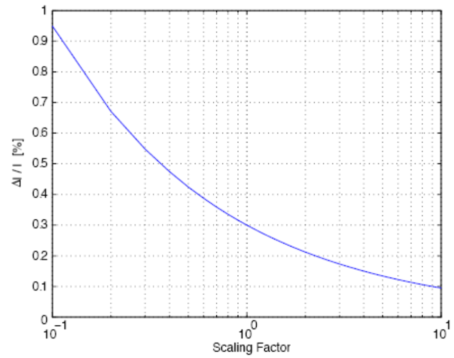
$WL = 12.11\mu^2$,

$\beta = 2I_U/V_{ov}^2 = 60.0\mu A/V^2$,

$W/L = 1.56$

$W = 4.35\mu m$

$L = 2.78\mu m$



Random mismatch with unary selection

The endpoint-fit error for *k* selected unit current sources is

$$\Delta I_{out}(k) = \sum_i^k \Delta I_{r,j} - k\overline{\Delta I_r} + \sum_i^k \Delta I_{s,j} - k\overline{\Delta I_s}$$

"random" "systematic"

where $\overline{\Delta I_r}$ and $\overline{\Delta I_s}$ are average errors cancelling the possible gain error

Explicitly, we have that the gain *g* at the endpoint is given, with I_u unary current, by (considering only random effects):

$$\sum_1^{2^n} \Delta I_{r,i} + 2^n I_u \equiv g \cdot 2^n I_u \quad \rightarrow \quad g = \frac{2^{-n}\sum_1^{2^n} \Delta I_{r,i} + I_u}{I_u}$$

The gain-normalized current error becomes:

$$\Delta I_{out,r}(k) = \frac{\sum_1^k \Delta I_{r,i} + kI_u}{g} - kI_u = \frac{\sum_1^k \Delta I_{r,i} - k2^{-n}\sum_1^{2^n} \Delta I_{r,i}}{1 + \frac{2^{-n}}{I_u}\sum_1^{2^n} \Delta I_{r,i}}$$

Random mismatch with unary selection – II

$$\Delta I_{out,r}(k) \approx \sum_1^k \Delta I_{r,i} - k2^{-n}\sum_1^{2^n} \Delta I_{r,i}$$

The variance is calculated as

$$\Delta I_{out,r}^2(k) = k\Delta I_r^2 + k^2 2^{-2n} \cdot 2^n \Delta I_r^2 - 2k2^{-n} \cdot k\Delta I_r^2 = \left(k - k^2 2^{-n}\right)\Delta I_r^2$$

Maximum at mid-range: $k_m = 2^{n-1} \quad \rightarrow \quad \Delta I_{out,r,\max}^2(k) \approx 2^{n-2}\Delta I_r^2$

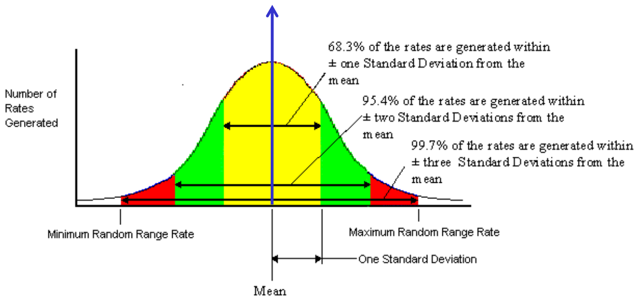
It is usually required that the maximum INL error must be lower than ½ LSB, which results in the following requirement on ΔI_r :

$$\sqrt{2^{n-2}\Delta I_r^2} = 2^{n/2-1}\Delta I_r < \frac{1}{2}I_u \quad \rightarrow \quad \frac{\Delta I_r}{I_u} < 2^{-n/2}$$

Random mismatch with unary selection – III

With a normal distribution of $x = \Delta I_r / I_u$, the probability of having an error equal to x is (with σ is the variance of x)

$$p(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{x^2}{2\sigma^2}}$$



Random mismatch with unary selection – IV

The normal distribution results in a yield of 0.99 at 2.57σ, and a yield of 0.999 at 3.3σ. In order to comply with these yields, we must then have:

$$2.57\sigma < 2^{-n/2} \quad \rightarrow \quad \sigma = \Delta I_r / I_u < 0.39 \cdot 2^{-n/2}$$

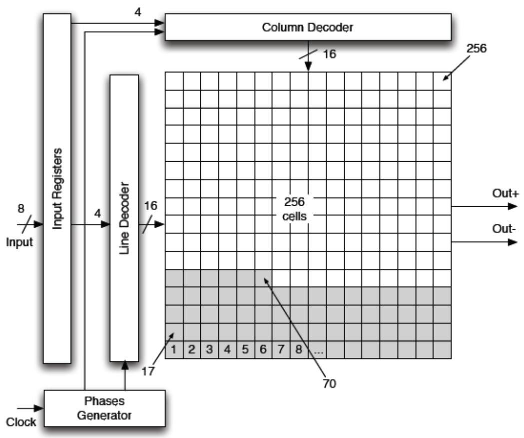
and

$$3.3\sigma < 2^{-n/2} \quad \rightarrow \quad \sigma = \Delta I_r / I_u < 0.30 \cdot 2^{-n/2}$$

However, it must be considered that this analysis does not account for the effect of systematic mismatch, which can be even worse than the random mismatch

Selection of current sources

Unit current sources are usually arranged in a two-dimensional array. The simplest selection mode is a sequential unary thermometric selection by lines and columns, starting in one corner of the array. Below we see an 8-bit DAC where 70 cells are selected (code 01000110)



Gradient error

Let us assume that the error is linearly dependent on the cell position:

$$I_u(i, j) = \overline{I_u}(1 + i\gamma_x\Delta_x)(1 + i\gamma_y\Delta_y)$$

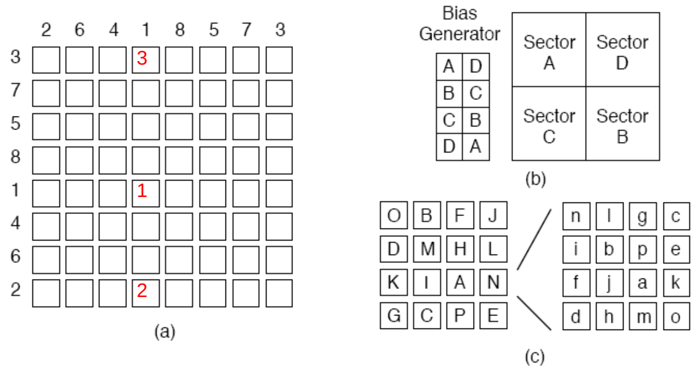
γ_x and γ_y being the gradients

Maximum error is approx. $n/2 \cdot \gamma_x\Delta_x$ and $m/2 \cdot \gamma_y\Delta_y$, and periodic

- The above error causes INL
- Moreover, it is worth pointing out that unary selection ensured monotonicity and enables flexibility, but requires one control signal for each element
- This makes the unary selection approach unpractical for 8-bit or more

Selection of current sources

The goal is to randomize the mismatches, keeping the accumulated error low



a) Line and column shuffling (in common-centroid fashion); b) Use of multiple local references, each close to the respective sector → lower threshold mismatch; c) multiple reference + random walk selection of sectors and unit cells → turns correlated error into pseudo-random noise

Current switching methods

- Binary-weighted DAC, combining 2^{k-1} unit current sources in parallel (with single control signal for entire parallel connection)
  - Virtually no decoding logic is required; however, possible non-monotonicity
  - With a random error, the maximum DNL (at mid-point) is

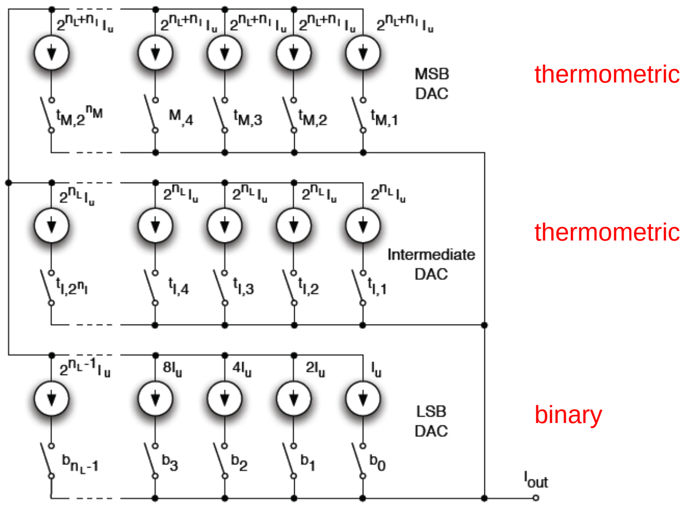
$$DNL_{\max} = \left(\left| \sqrt{2^{n-1}}\, \Delta I_r / \Delta I_u \right| + \left| \left(\sqrt{2^{n-1} - 1} \right) \Delta I_r / \Delta I_u \right| \right) \approx \pm 2\sqrt{2^{n-1}}\, \Delta I_r / \Delta I_u$$

- Unary-control DAC (thermometer, shuffled, random)
  - Intrinsic monotonicity, minimum glitch power, good DNL/INL; however, each current source needs an individual control signal;
  - The maximum DNL is, for any code transition

$$DNL_{\max} = 2\, \Delta I_r / \Delta I_u$$

Segmentation with current switching

Conceptual schematic of a 3-step segmented current-steering DAC



Area of segmented DAC

- The area of a segmented architecture depends on the area of the unit current sources and the area of the circuitry necessary to generate and distribute the control signals
- The maximum allowed DNL determines the value of the gate area WL of the MOS transistor used to generate I_U in the binary-weighted LSB DAC (see previous eq. on max. DNL in binary-coded DACs):

$$WL > 2^{n_L+1} \left(A_\beta^2 + \frac{4 A_{V_{th}}^2}{\left(V_{gs} - V_{th}\right)^2} \right) \bigg/ DNL_{\max}^2$$

Thus, the area of the single LSB cell is proportional to 2^{n_L} , and can be written as

$$A_U = A_u 2^{n_L}$$

Area of segmented DAC – II

- The area of the logic circuitry necessary to generate and distribute a single thermometric code increases (roughly) linearly with the number of MSB:

$$A_{U-MSB,extra} = A_d n_M$$

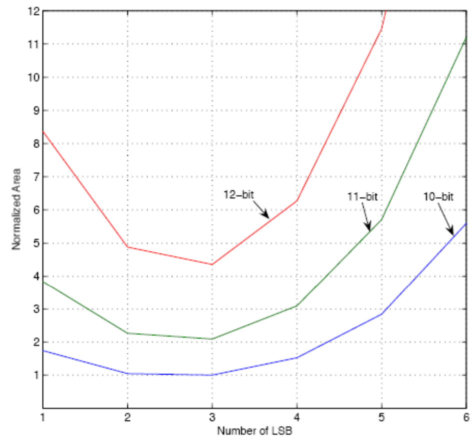
- For a segmentation $n = n_L + n_M$, we obtain in total

$$A_{DAC} = 2^n A_U + 2^{n_M} A_{U-MSB,extra} = 2^n A_u 2^{n_L} + 2^{n_M} A_d n_M$$

$$A_{DAC} = 2^n A_U \left(2^{n_L} + \frac{A_d}{A_u} \frac{n - n_L}{2^{n_L}} \right)$$

- If $A_d / A_u = 8$ and $n = 12$, the DAC area is minimum for $n_L = 3$

Area of segmented DAC – III



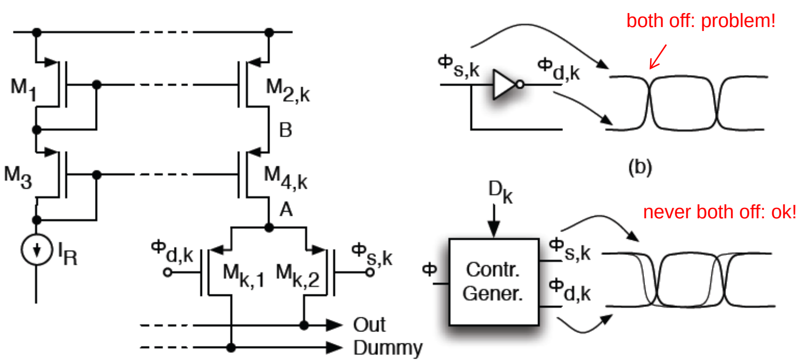
On the left, plots of normalized DAC area for 12-bit, 11-bit, and 10-bit segmented DACs, versus n_L

With a 3-step segmented current-steering DAC, the area becomes:

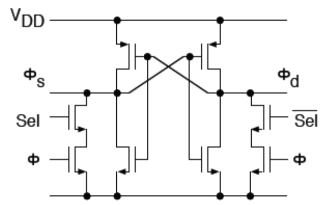
$$A_{DAC} = 2^n A_U \left(2^{n_L} + \frac{A_d}{2^n A_u} \left(n_I 2^{n_I} + n_M 2^{n_M} \right) \right)$$

Switching of current sources

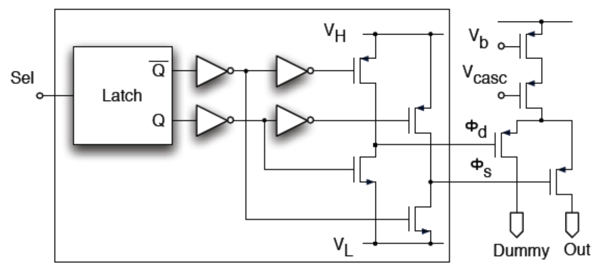
- Remember: when generating the control phases, never leave the connection of a unit current generator open, since the transistor would be pushed into the triode region, with a long recovering time



Switching phase generator



(a)



(b)