Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2011-03-12, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

Allowed equipment:

- Textbook: T. H. Lee, "The Design of CMOS RF Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

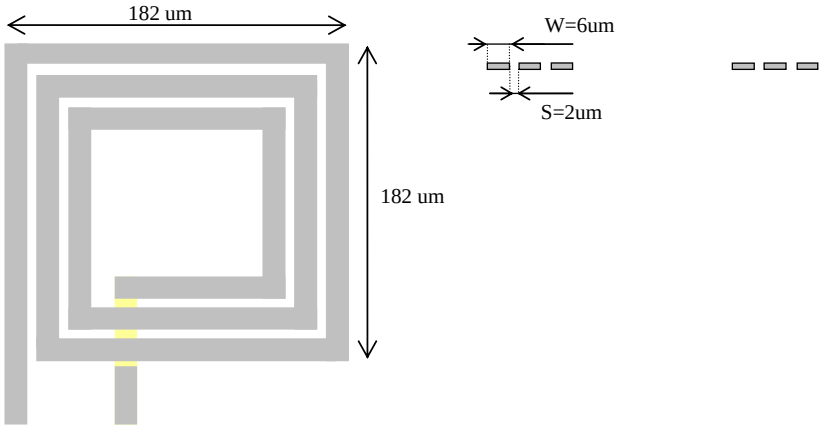
Good luck!

Problem 1.

Design an RC polyphase filter that generates a quadrature output signal from a differential input at 2.4GHz. Use a connection that gives zero quadrature phase error when the components are perfectly matched, although some amplitude error may still occur. To compensate for process variations, use a two stage design with the first stage tuned at 2.4GHz + 20% and the second stage tuned at 2.4GHz -20%. All resistors in the filter should be equal to 400Ω. Draw the schematic and indicate the value of the components. (6p)

Problem 2.

An inductor according to the figure below has been realized in the top Cu metal layer (metal 8) of the 130nm CMOS process with parameters in the data sheet. The thickness of the metal 8 layer is 0.6um. A metal 1 patterned ground shield is used beneath the spiral.



Neglect Eddy current losses in the substrate and proximity effects in the metal track. Further neglect capacitive fringing, so that the capacitance from the track to the ground shield can be calculated as a plate capacitor (with 0.007 fF/um^2 between metal 8 and metal 1). Also neglect the turn-to-turn capacitance and the capacitance of the underpass. The inductor is to be used in a 5GHz circuit.

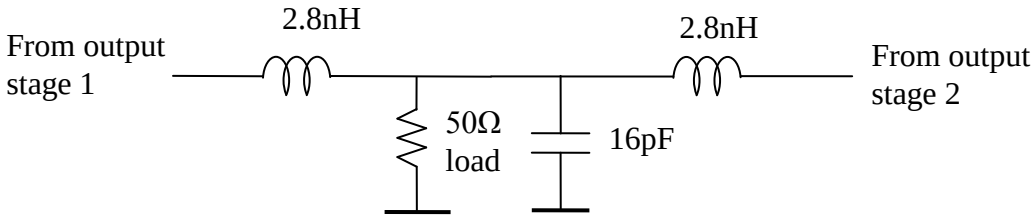
Calculate:

a. The inductance L and the quality factor Q at 5GHz. Also calculate the self resonance frequency, assuming one terminal to be grounded. (4p)
b. The capacitance required in parallel with the inductor to make the parallel resonance frequency equal to 5GHz. (Still one terminal is assumed grounded.) Also calculate the equivalent parallel resistance at resonance (5GHz) of this LC resonator. (2p)

(Useful constants can be found below problem 5)

Problem 3.

A power amplifier has two output stages. The output stages can operate either just one at a time, or both simultaneously, depending on how much output power is needed. By operating just one output stage when less output power is needed, power can be saved and the efficiency improved. The power amplifier is to operate at 1GHz, and the network below is used to combine the output power of the two stages. When an output stage is off its output will be short circuited to signal ground.



a. Calculate the load impedance at 1GHz of output stage 1 when output stage 2 is off. (1p)
b. Calculate the load impedance at 1GHz of output stage 1 when output stage 2 is on, producing an output voltage equal to that of stage 1. (1p)
c. Adjust the inductor value so that the impedance in b. becomes completely resistive at 1GHz. Both inductors should still be equal. (1p)
d. Recalculate a. for the new inductance. (1p)
e. Calculate the power in the load when the output stage 1 delivers $2V_{rms}$ at 1GHz and the output stage 2 is off. (1p)
f. Calculate the power in the load when both output stages deliver equal signals of $2V_{rms}$ at 1GHz. (1p)

Problem 4.

An LNA according to the schematic below has been designed in the 130nm CMOS process with process parameters according to the data sheet. The circuit parameters are:

Bias: Supply voltage=1.2 V, V_{G2} = 0.8 V, V_{IN}=0.5 V

Transistor dimensions: M1 and M2 equal size with W=100um, L=0.25um

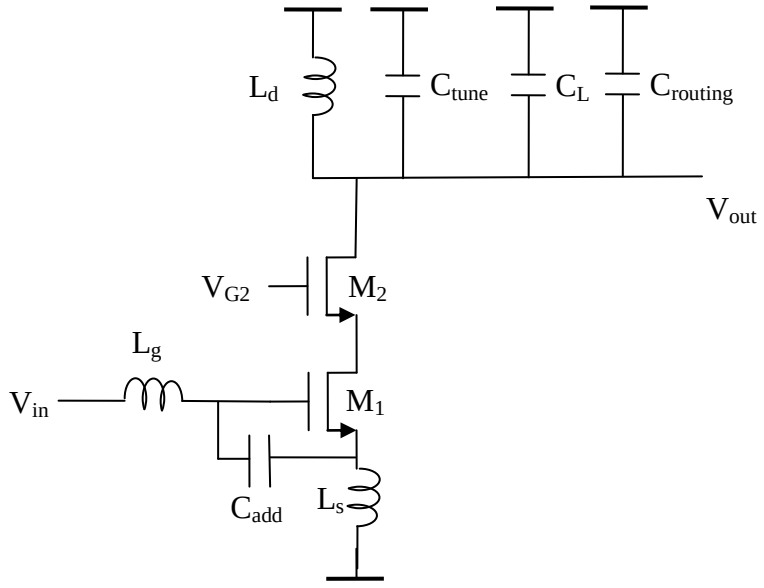
Transistor layout: Finger layout with 10 gate fingers per transistor, gate-gate distance (drain finger length)=0.4um

Source inductor: L_s=1nH, Q=∞, f_s=∞

Gate inductor: L_g=6nH, Q=∞, f_s=∞

Drain inductor: L_d= 8nH, Q=10, f_s=10GHz

Capacitances: C_{add}=380fF, C_L=100fF, $C_{routing}$=50fF



In the calculations you can assume long channel behavior of the transistors. Body effect and channel length modulation may be neglected. In calculation of drain-bulk capacitance side-wall capacitance can be neglected, and the capacitance can be calculated at 0V bias. The noise contribution of the cascode device M2 amounts to 20% of the thermal noise of M1.

Calculate:

a. The frequency f_o to which the input circuit is tuned (neglect C_{gd1}) (1p)
b. C_{tune} so that the output becomes tuned to the same frequency as the input (1p)
c. The input impedance at f_o. (1p)
d. The noise figure (with source matched to the input impedance) (1p)
e. The gain and bandwidth of the amplifier. (1p)
f. The input referred compression point. (May be limited by input or output) (1p)

Some useful equations, to be modified as necessary:

$$Q = \frac{1}{2\omega_0 R_S C_{gs}} \qquad R_{in} = R_S = \frac{g_m L_s}{C_{gs}} \qquad \omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}}$$

$$A_v = 2Qg_m R_L \qquad P = \frac{C_{gs}}{C_T} \qquad \delta = 2\gamma = 4 \qquad F = 1 + \frac{(\delta/5)(Q^2+1)P^2 + \gamma/4}{R_S Q^2 g_m}$$

Problem 5.

A local oscillator (LO) signal is to be generated for a direct conversion transceiver intended for both the DCS and the PCS systems. A quadrature LO signal is needed, and it is generated by a frequency divide by two circuit. The oscillator must therefore operate at two times the frequency of the final LO signal. A differential cross-coupled VCO is to be designed for this application in the 130nm CMOS process with parameters according to the data sheet.

The frequencies of DCS and PCS are given below:

DCS: uplink 1710.2-1784.8MHz, downlink: 1805.2-1879.8MHz

PCS: uplink 1850-1910MHz, downlink: 1930-1990MHz

To allow for process variations, make the tuning range so that in the nominal case the lowest frequency that can be generated is 4% below the minimum needed, and the highest is 4% higher than the maximum needed.

The phase noise requirements are -138dBc/Hz at 3MHz offset, and -162dBc/Hz at 20MHz offset, after the frequency divider. Frequency division by two improves the phase noise by 6dB.

Assume that differential inductors with Q equal to 12 at the frequency and inductance range of interest can be realized, and with a self resonance frequency of 12GHz. Minimum length varactors are to be used; assume these to have a capacitance tuning range Cmax/Cmin=2.5 and a Q equal to 20 for all different tuning voltage settings.

Use an oscillator including a tail current noise filter, and assume the resulting noise factor of the oscillator F to be equal to 2.

Draw the schematic of the oscillator and calculate values of all components. The supply voltage is 1.2V. How much current does your oscillator use? Try not to use more than necessary. (6p)

Useful constants:

$k = 1.38 \cdot 10^{-23}$ J/K
$\mu_0 = 4\pi \cdot 10^{-7}$ Vs/Am
$\varepsilon_0 = 8.85 \cdot 10^{-12}$ As/Vm
$\sigma_{Cu} = 59.6 \cdot 10^{6}$ S/m

in all problems the temperature T is equal to 300K