Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2010-03-10, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

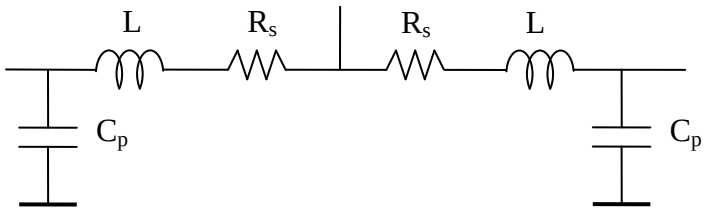
Allowed equipment:

- Textbook: T. H. Lee, "The Design of CMOS RF Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

You are about to design an oscillator at 5GHz. At your disposal you have a library consisting of 3 differential on-chip inductors. At 5GHz the inductors can be modeled according to the figure below.



Inductor	*L*	R_s	C_p
A	0.50 nH	1.5 Ω	200 fF
B	1.0 nH	2.5 Ω	140 fF
C	2.0 nH	7.0 Ω	100 fF

a. Calculate the quality factor (Q) of the 3 inductors (A,B & C) at 5GHz. (1p)
b. Calculate the self-resonance frequency for differential excitation (extrapolated from the 5GHz model above) for the 3 inductors. (1p)
c. Calculate the parallel resistance due to each inductor when used in the resonator of a 5GHz LC oscillator. (1p)
d. Which inductor is best suited for use in an oscillator where wide frequency tuning range is the main objective? Motivate! (1p)
e. Which inductor is best suited for use in an oscillator where low power is the main objective? Motivate! (1p)
f. Which inductor is best suited for use in an oscillator where low phase noise is most important, and the power consumption is not a problem? Motivate! (1p)

Problem 2.

An on-chip power amplifier has a differential output, where each side should be loaded by a 5Ω resistive impedance for best performance. This power amplifier should be connected to a 50Ω single-ended resistive load. For this reason a simple circuit is to be designed performing both the differential to single ended conversion (balun function) and the impedance transformation.

a. For a circuit consisting of one inductor between the positive amplifier output and the load, and one capacitor between the negative amplifier output and the load; choose the inductance L and the capacitance C so that the circuit delivers a voltage to the load that is proportional to the voltage difference between the amplifier outputs at 1GHz, and that the real part of the input admittance is 200mS at each input at 1GHz, when the load is 50Ω. (4p)
b. How large is the imaginary part of the admittance at the two outputs? Calculate values of shunt-capacitors or inductors connected from input to ground, that cancel the imaginary part, making the inputs completely resistive. (2p)

Problem 3.

An NMOS transistor has been realized in the 130-nm technology with parameters according to the data-sheet. Following is given:

W=100um, L=0.2um, layout with 20 gate fingers, 0.4um between two adjacent gates, V_G=0.5V, V_S=V_B=0V, V_D=0.6V, room-temperature

Use long-channel equations to find:

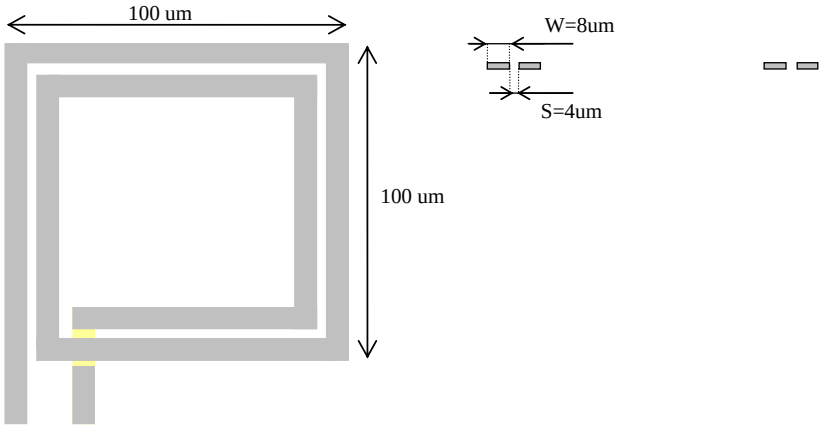
The small signal capacitances c_{gs}, c_{gd}, and c_{db}, the gate resistance r_g, the DC drain current I_D, the small signal transconductance g_m, the transition frequency f_t, the maximum oscillation frequency f_{max}, the drain-source small-signal conductance g_{ds}, the intrinsic voltage gain $A_{v,int}$, and the total drain current noise and gate current noise in a 1MHz band centered at 3GHz.

Assume the noise parameters γ=1.5 and δ=3

(Useful constants can be found below problem 5)

Problem 4.

An inductor has been realized according to the figure below. The spiral is realized in a 2um thick Cupper metal layer. The thickness of the oxide between the track and the substrate is 4um. However, a patterned ground shield is used, and the distance from the track to that is 3.5um. The relative permittivity of the dielectric isolation material is equal to 4.



Assue there are no Eddy current losses in the substrate, and no proximity effect in the metal track.

a. The inductor is to be used in a 10GHz X-band oscillator. Calculate the inductance L and the quality factor Q at 10GHz. Also calculate the self resonance frequency, assuming one terminal to be grounded. (3p)
b. Now the patterned ground shield is removed. Re-calculate the self resonance frequency. Also re-calculate the quality factor, assuming a substrate conductivity of 5Ωcm, and assuming that the effective (capacitively coupled) current path between the terminals through the substrate can be modeled as a box of length 100um, width 300um, and depth 100um, where the current flows in the length direction. Observe that this resistive current path is in series with the track-to-substrate capacitance. (3p)

(Useful constants can be found below problem 5)

Problem 5.

A fully integrated 5GHz low noise amplifier is to be designed in the 130-nm CMOS process. To achieve low noise an inductively source-degenerated topology is chosen. Cascode stages are used for stability reasons. They add 0.2dB to the noise figure. The amplifier is fully differential, and all inductors, including the gate inductors are to be realized on-chip. The quality factor of the on-chip inductors is equal to 14 at 5GHz, and values up to 5nH can be realized. Their self-resonance frequency is high enough to be neglected. The source impedance is 50Ω per side, to which the amplifier should be matched.

Requirements:

- F < 2.5dB
- A_v = 20dB
- ICP > -13dBm (total power at both inputs)
- I_{DC} < 10mA

a. Draw the schematic (1p)
b. Design the circuit, that is decide values of the inductors L_s, L_g, L_{Load}, of the parallel resistor R_{Load} at the output that may be necessary to reduce the gain, and of C_{Load} that may be needed to tune the output. Calculate transistor width W, gate bias voltages V_{Ginput}, $V_{Gcascode}$. Use long channel equations everywhere. When calculating $V_{Gcascode}$, 0.1V should be added to take body-effect into account. Also calculate the number of gate fingers needed to make the gate resistance below 0.4Ω. When calculating the noise contribution of the parasitic resistances at the input side, a term equal to the parasitic resistance divided by the source resistance can be added to the noise factor. Neglect noise due to the load. Also the supply voltage needed to avoid that the casode devices enter the triode region before the desired compression point should be calculated (thanks to the cascodes a supply slightly higher than 1.2V can be accepted). The distance between gate fingers in the transistor layout is equal to 0.4um. (5p)

Useful equations:

$$Q = \frac{1}{2\omega_0 R_S C_T} \qquad R_{in} = R_S = \frac{g_m L_s}{C_T} \qquad \omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_T}}$$

$$A_v = 2Qg_m R_L \qquad P = \frac{C_{gs}}{C_T} \qquad \delta = 2\gamma = 4 \qquad F = 1 + \frac{(\delta/5)(Q^2+1)P^2 + \gamma/4}{R_S Q^2 g_m}$$

Useful constants:

k = 1.38 · 10^{-23} J/K
$\mu_0 = 4\pi \cdot 10^{-7}$ Vs/Am
ε_0 = 8.85 · 10^{-12} As/Vm
σ_{Cu} = 59.6 · 10^6 S/m