Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2009-03-11, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

Allowed equipment:

- Textbook: T. H. Lee, "The Design of CMOS RF Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

a. Design an RC-CR filter that generates two signals in quadrature from a single input signal at 5GHz. The resistors should be set to 200 Ω. Calculate the capacitor values and draw the schematic. (2p)
b. Each capacitor has a parasitic series resistance of 10 Ω. Calculate the resulting amplitude error and phase error. (2p)
c. The signal generated by the RC-CR filter is used as LO signal in a quadrature mixer. The LO signal is large enough to saturate the mixer, and the amplitude error is thereby reduced 5 times. Calculate the resulting image rejection, assuming the mixer itself to have zero phase and amplitude errors, so that all errors are due to the LO signal. (2p)

Problem 2.

A GPS receiver at 1.575GHz is realized in the 0.35um CMOS process. The noise figure of the LNA must be below 2.5dB. In the simulations a noise figure of 2dB was achieved, but without taking transistor gate resistance or resistance of on-chip wires into account.

a. The input transistor is 100um wide, 0.4um long, and uses 8 gate fingers contacted on one side. Calculate the gate resistance. (2p)
b. The wire from the pad to the gate is in metal 4. Length=150um, width=10um. Calculate the resistance at 1.575GHz including skin effect. (2p)
c. Approximately what will the LNA noise figure be when simulated including the gate and wire resistance, does it still meet the specification? (2p)

Useful constants: $\mu_0=4\pi*10^{-7}$ As/Vm $\rho_{Al}=2.7*10^{-8}$ Ωm

Problem 3.

A differential NMOS only cross-coupled VCO is realized in the 0.35um CMOS process.

It consumes 2mA from a 2V supply. It uses a differential inductor with L=2*5nH, Q=10, and a self resonance frequency of 8GHz. An MOS varactor of 300um*0.5um is used at each side. The varactor has a Q of 30 at all control voltages, and a C_{max}/C_{min} ratio equal to 2.5. Each of the two switch transistors has 80um total with, is 0.4um long, has 8 gate fingers, and 1.2um wide drain fingers (gate-to-gate distance). Each oscillator output is loaded by 100fF in series with a 5Ω resistance.

a. Calculate the frequency tuning range, include effect of reverse bias dependent capacitances. (2p)
b. Calculate the total resonator Q at the edges of the tuning range, f_{min} and f_{max}. (3p)
c. Estimate the oscillation amplitude at f_{min} and f_{max}. (1p)

Problem 4.

Design a double balanced mixer for a WCDMA receiver using the 0.35um CMOS process. The RF input frequency is 2.14GHz, the IF bandwidth should be equal to 150MHz, the voltage conversion gain A_{cv} should be equal to 6dB, the input referred compression point should be at least 200mV per side, the supply is 2.5V, and the bias current should not exceed 5mA. The double sideband noise figure, comparing input voltage noise to that of a 50Ω resistor should not exceed 8 dB, with γ=1.5. Assume that the switch devices and load resistors together contribute with as much noise as the input devices. The LO amplitude is equal to 400mVpk per side. The switch devices should not conduct simultaneously for more than 25% of the time. No transistor is allowed to enter the triode region for input signals up to the compression amplitude of at least 200mV, this must be verified. Determine all component values and bias points, and draw the schematic. Long channel equations can be used, and body effect can be ignored. (6p)

Problem 5.

A power amplifier (PA) should drive a 50Ω antenna. The power amplifier should be used at frequencies ranging from 1.6GHz to 2.5GHz. The optimum load of the PA is 5Ω. An impedance matching network must thus be designed. It should transform 50Ω to 5Ω at an operating frequency of 2GHz.

a. Design a simple low-pass L-match network. Calculate the component values, and draw the schematic. Also design a matching network consisting of two cascaded L-match networks, with an intermediate resistance of 15Ω. Calculate the component values, and draw the schematic. (2p)

b. Calculate the impedance at the PA at 1.6GHz and at 2.5GHz for the two different matching networks. Which matching network is best at these frequencies? (2p)

c. The power amplifier can deliver a maximum of $2V_{rms}$ to the load, and a maximum current of $0.4A_{rms}$. Calculate the amount of power that can be delivered to the antenna at 1.6GHz and 2.5GHz using the two different matching networks. Which matching network is the best, and how large is the difference? (2p)