Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2008-03-14, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

Allowed equipment:

- Textbook: T. H. Lee, "The Design of CMOS RF Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

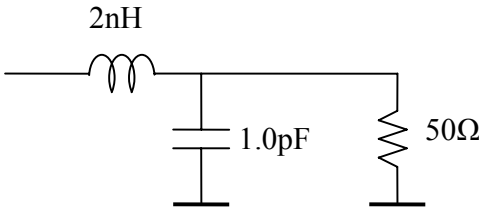
A power amplifier (PA) which should be loaded by 3Ω is to drive a 50Ω antenna. An impedance matching network must thus be designed. It should transform 50Ω to 3Ω at the operating frequency of 1GHz.

a. Design a simple low-pass L-match network. Calculate the component values, and draw the schematic. (2p)

b. Design the impedance transformation network as two cascaded low-pass L-match circuits. Transform the antenna impedance to an intermediate resistive impedance with the first L-match, and then from the intermediate impedance to 3Ω with the second L-match. Design the network so that both L-matches have equal Q-value. Calculate the component values, and draw the schematic. (4p)

Problem 2.

A low noise amplifier (LNA) has an input impedance equal to 50Ω on the chip. However, due to the capacitance of the input pad and the ESD-diodes, and the inductance of the bond-wire and package lead, the input impedance is not 50Ω at the PCB. This is illustrated below:



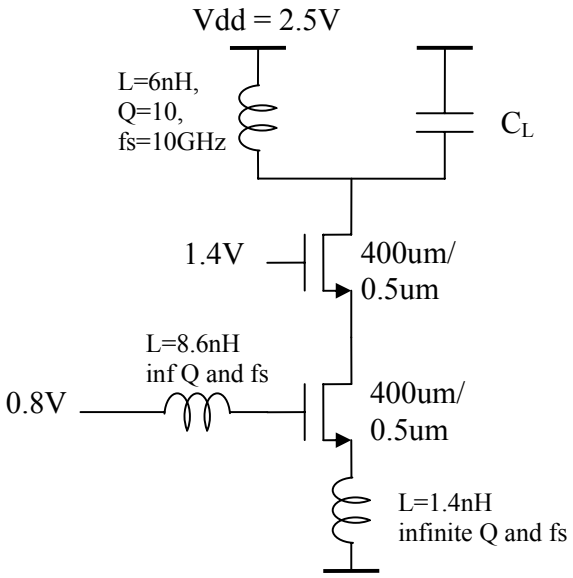
The operating frequency is 2.4GHz

a. Design an L-match which transforms the impedance to 50Ω. A low-pass network consisting of one inductor and one capacitor should be used. In this way an external bias voltage can pass through the network. (4p)

b. Design a high-pass network consisting of a series capacitor and a shunt inductor that transforms the impedance to 50Ω. (2p)

Problem 3.

A single-ended inductively source degenerated LNA has been designed in the 0.35um CMOS process, according to the schematic below:



Use long-channel equations.

Assume that the drain-bulk capacitance can be approximated by its zero reverse bias value. The drain fingers are 1.2um wide in the transistor layout.

The capacitance of the routing at the output plus the input capacitance of the next stage (the mixer) can be estimated to 400fF in total.

Assume that the cascode device increases the noise figure by 0.2dB, and that the noise due to the load can be ignored.

a. Calculate the bias current level. (1p)
b. Calculate the resonance frequency of the input circuit. Then calculate the value of C_L so that the output resonates at the same frequency. (2p)
c. Calculate the input impedance at the resonance frequency, the noise figure assuming the source to be matched to the input impedance, and the voltage gain under the same assumption. (3p)

The following equations can be used:

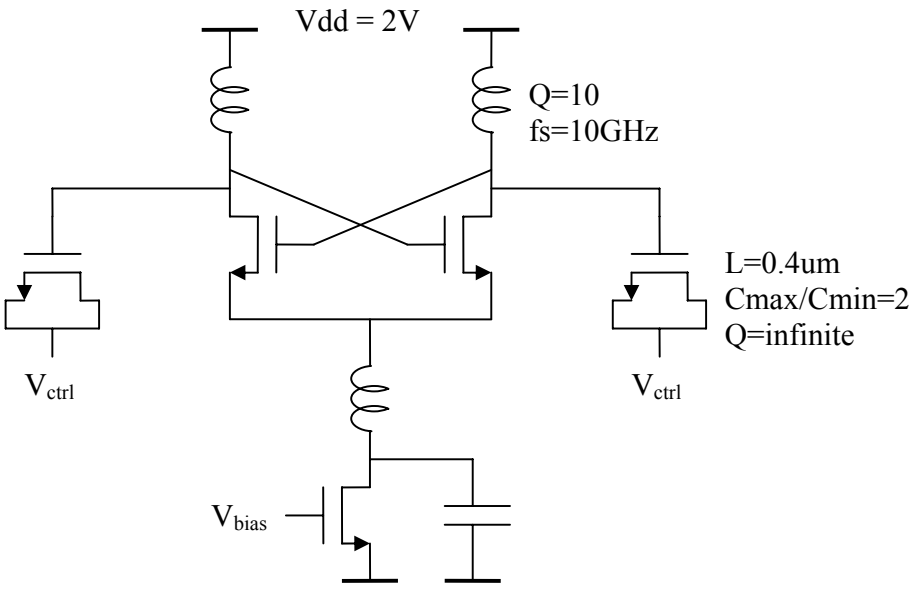
$$Q_{in} = \frac{1}{2\omega_0 R_S c_{gs}} \qquad R_{in} = R_S = \frac{g_m L_s}{c_{gs}} \qquad \omega_0 = \frac{1}{\sqrt{(L_s + L_g)\cdot c_{gs}}}$$

$$A_v = 2Q_{in} g_m R_L \qquad F = 1 + \frac{(\delta/5)\cdot(Q_{in}^2 + 1) + \gamma/4}{R_s Q_{in}^2 g_m} \qquad \delta = 2\gamma = 4$$

Problem 4.

A VCO is needed for a 1.8GHz mobile phone. Quadrature signals are needed, and a frequency divider is going to be used to generate these. The oscillator must therefore operate at twice the frequency. The desired tuning range is 3.45GHz to 3.75GHz. The phase noise must not exceed -136dBc/Hz at 3MHz offset. The power consumption must be as low as possible.

The schematic is shown below:



Assume that the bias current is switched to a perfect square-wave when calculating output oscillation amplitude. When you design the circuit, make the oscillation amplitude equal to 1.5V peak/per side.
Assume the noise factor F to be equal to 2.
The start-up loop-gain should be at least 5.
For drain-bulk capacitance, use the zero bias value divided by 2. Drain fingers are 1.2um wide.

Design the circuit, that is choose width and length of the switch transistors, width of varactors, and the inductance of the resonator. Calculate the bias current. How much capacitance is left for output routing and input capacitance of the frequency divider? A minimum of 100fF per side is required. Make sure that the requirements on phase noise, tuning range, and start-up loop gain are met. (6p)

You don't have to calculate the tail inductance in this problem!

Use long-channel equations.

Boltzmann's constant: $k = 1.38*10^{-23}$

Problem 5.

Now the tail inductance of the oscillator in the previous problem should be designed. You should design an on-chip spiral inductor that resonates with the source-bulk and gate-source capacitors of the transistors at twice the oscillation frequency.

Important: Don't forget to include the parasitic capacitance of the inductor itself in the calculations.

If you have not been able to solve the previous problem, you can assume each switch device to be 50um wide and 0.4um long. Observe that this is not the correct value of the previous problem, so if you have solved the previous problem with a different result there is no need to be worried.

In the parasitic capacitance calculation, use zero bias values for source-bulk capacitances.

The on-chip inductor should be designed using the data-sheet of the 0.35um process.

The only requirement is that the Q of the inductor should be equal to 5 or higher. The substrate losses can be neglected.

The parameters of interest are diameter, conductor width, number of turns, and spacing. You should also calculate the Q to verify that it is above 5. You must also show that the inductor resonates at twice the VCO frequency with its own capacitance plus the transistor parasitics of the common source node. (6p)

Useful constants: $\mu_0 = 4\pi \cdot 10^{-7}$ Vs/Am $\rho_{Al} = 2.7 \cdot 10^{-8}$ Ωm