Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2007-03-06, 14.00-19.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

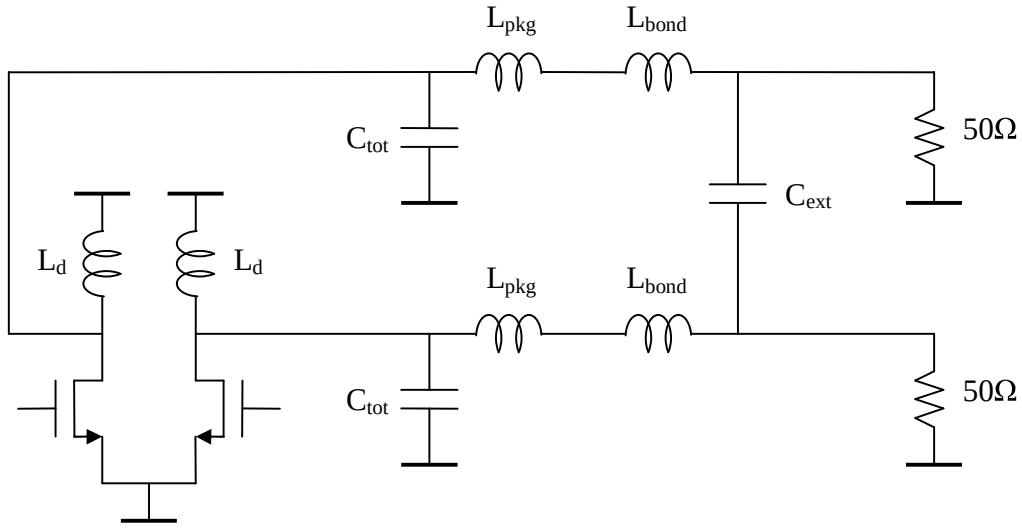
Allowed equipment:

- Textbook: T. H. Lee, “The Design of CMOS RF Integrated Circuits”
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

A differential 2.4GHz PA is designed to be loaded by 10Ω at the drain of each of the two output transistors. The load at the PCB, however is 50Ω per side (100Ω differentially). An impedance transformation is thus necessary. The schematic is shown below:



$C_{tot} = C_{drain}+C_{ESD}+C_{pad}$, $C_{ESD} = 0.2pF$, $C_{pad} = 0.1pF$, $C_{drain} = 0.7pF$

Calculate the inductance L_d to resonate with C_{tot} at 2.4GHz. Then calculate C_{ext} and $L=L_{pkg}+L_{bond}$ so that the desired 10Ω impedance is seen at each drain at 2.4GHz. (6p)

(The inductance L becomes quite low, requiring short bond wires and a good package)

Problem 2.

Three different inductors are designed in the 0.35um CMOS process. They are rectangular single-ended spirals in the top metal layer (metal 4). All inductors have the same outer diameter of 150µm, the same trace width of 8µm, and the same spacing of 2µm (spacing only relevant if more than one turn). The only difference between the inductors is the number of turns, which equals 1, 2, and 4, respectively.

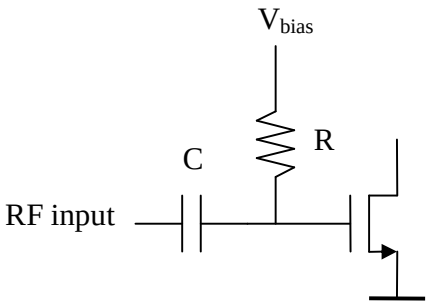
Neglecting substrate losses and fringing, calculate:

a. The inductance of all three inductors. (2p)
b. The self-resonance frequency of all three inductors. (2p)
c. The quality factor at 5GHz of all three inductors. (2p)

Useful constants: $\mu_0 = 4\pi\cdot10^{-7}$ Vs/Am $\rho_{Al} = 2.7\cdot10^{-8}$ Ωm

Problem 3.

The figure below illustrates the input of an AC-coupled amplifier, where a resistor is used to set the gate bias voltage. To avoid signal attenuation the impedance of the resistor should be as large as possible at the operating frequencies.



Unfortunately all resistors implemented on-chip are affected by significant parasitic capacitances to the substrate (ground), which limit the high frequency impedance.

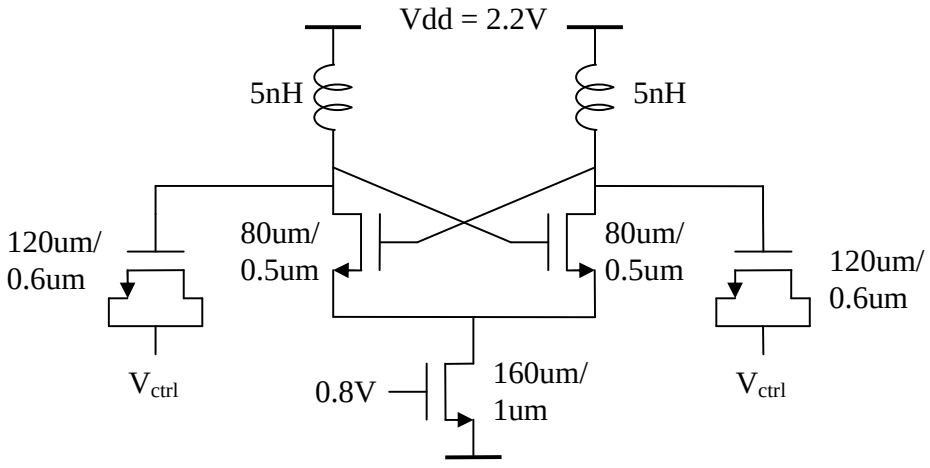
a. Calculate the impedance magnitude at 2GHz for two infinitely long resistors realized in poly1 in the 0.35um CMOS process. One resistor is 0.5um wide and the other is 2um wide. (4p)

   Hint: Use page 206 in textbook, figure 6.1, and $Z_{in} \approx \sqrt{Z/Y}$

b. Of course infinitely long resistors can't be realized, so instead we design them to have a DC resistance equal to 3 times the impedance magnitude calculated in a. Calculate the required length of the two different resistors. (2p)

Problem 4.

A VCO is designed in the 0.35um CMOS process according to the figure below:



The quality factor of the resonance tank is equal to 10 at the frequency of oscillation. The varactors have a ratio of maximum to minimum capacitance equal to 2. The parasitic capacitance due to the inductor and the routing is 100fF in each output node. The drain

capacitance at the same nodes can be approximated to half the zero bias voltage value counting the area and neglecting the perimeter. A finger layout is used with 1.2um between the gate fingers. The noise factor F is equal to 3. Use long channel equations to calculate:

a. The frequency of oscillation when the varactor is halfway between minimum and maximum capacitance. (Close to but not exactly the center frequency) (2p)
b. The output amplitude at the frequency in a. (2p)
c. The phase noise at 3MHz offset, for the oscillation frequency in a. (1/f noise will have no influence at this large offset frequency) (1p)
d. The tuning range, using the full capacitance range of the varactor (1p)

Boltzmann's constant: $k = 1.38*10^{-23}$

Problem 5.

Design a single ended inductively source degenerated LNA using the 0.35um CMOS process meeting the following requirements:

- Frequency of operation = 1.575GHz (GPS)
- NF < 2.5dB
- $Z_{in} = 50\Omega$
- Voltage gain > 30dB
- Supply voltage = 3V, Supply current < 5mA

The following assumptions and equations can be used:

- Long channel equations can be used
- Inductors at gate and source are not on-chip and losses are neglected
- Noise due to cascode increases noise figure by 0.2dB, noise due to load is ignored
- $C_{drain} = 0.6fF/um$, $C_{out,routing} = 50fF$
- On chip inductors up to 10nH can be used with

$$Q_L = \min(\sqrt{500\text{nH}/L},\ 20) \qquad f_s = \frac{30\text{GHz}\cdot\text{nH}}{L}$$

- $$Q_{in} = \frac{1}{2\omega_0 R_S c_{gs}} \qquad R_{in} = R_S = \frac{g_m L_s}{c_{gs}} \qquad \omega_0 = \frac{1}{\sqrt{(L_s + L_g)\cdot c_{gs}}}$$

$$A_v = 2Q_{in} g_m R_L \qquad F = 1 + \frac{(\delta/5)\cdot(Q_{in}^2+1) + \gamma/4}{R_s Q_{in}^2 g_m} \qquad \delta = 2\gamma = 4$$

Design the amplifier, that is draw the schematic and calculate all transistor sizes (cascode should have same size as main transistor), calculate all bias voltages, all inductor sizes, and if an additional capacitance is needed in the output resonance tank, calculate the size of that too. Check that all requirements are fulfilled (don't forget to add the noise due to the cascode). (6p)