Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2006-03-07, 14.00-19.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

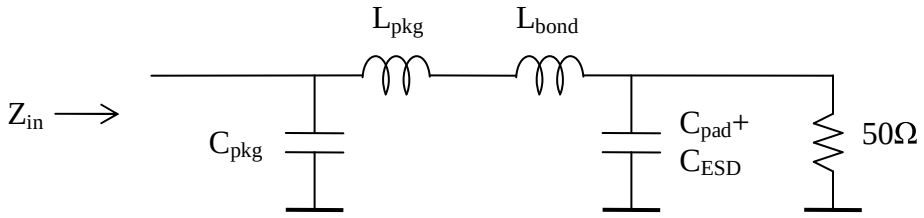
Allowed equipment:

- Textbook: T. H. Lee, “The Design of CMOS RF Integrated Circuits”
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

An LNA is designed to have 50Ω input impedance at 5GHz. This is successfully achieved on the chip. However, due to parasitics of the pad, ESD protection, bondwire, and package, the impedance seen from the PCB will be different. The circuit below can be used to model the effects:



C_{pad} = 0.1pF, C_{ESD} = 0.2pF, L_{bond} = 2nH, L_{pkg} = 1.5nH, C_{pkg} = 0.2pF

a. Calculate the impedance Z_{in}. (3p)
b. Design a network with capacitors and inductors which transforms Z_{in} to the desired impedance 50Ω on the PCB. (3p)

Problem 2.

A person with very limited experience in RF IC layout has made a transistor with just one finger. The transistor length is 0.4um and the width 100um. Use the datasheet of the 0.35um CMOS process to calculate:

a. The gate resistance r_g (1p)
b. The approximate frequency where the problems with signal delay and attenuation associated with the propagation in the gate becomes evident, $\omega = \frac{1}{r_g c_{gs}}$ (1p)
c. The number of fingers required for r_g to be between 1Ω and 2Ω (2p)
d. Is the finger length in c sufficiently short for 5GHz operation. Assume that we want a factor of 10 margin to the frequency where problems become evident. (2p)

Problem 3.

Design an on-chip inductor in the 0.35um process with the following requirements:

- Maximum area = 120um x 120um
- Inductance = 3nH ± 5%
- Quality factor > 8 at 5GHz
- Single-ended inductor (not differential)
- Self-resonance frequency > 14GHz with one terminal grounded

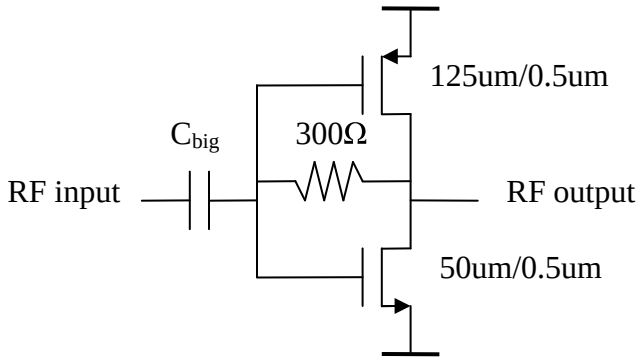
A poly-silicon shield is to be used below the inductor. Neglect resistive losses in the shield, substrate losses, and capacitive fringing. When connecting metal layers in parallel to increase the thickness, the via-layer(s) can be neglected, that is the total thickness is set to equal the sum of the thicknesses of the metal layers used.

Determine the inductor topology and geometrical parameters, and verify that the requirements are met. (6p)

Useful constants:
$\mu_0 = 4\pi \cdot 10^{-7}$ Vs/Am
$\rho_{Al} = 27 \cdot 10^{-9}$ Ωm
$\varepsilon_0 = 8.85 \cdot 10^{-12}$ As/Vm
$\varepsilon_r = 3.9$ for SiO_2

Problem 4.

A low noise amplifier (LNA) is designed in the 0.35um CMOS process according to the figure below:



Neglect all parasitic capacitances, use long-channel equations, assume C_{big} to be a short circuit at RF frequencies, and use a thermal noise coefficient γ=1.

a. Calculate the output DC voltage and the bias current of the circuit (1p)
b. Calculate the input resistance and the voltage gain (2p)
c. Calculate the noise figure (2p)
d. How can the poor noise figure be improved, motivate (1p)

Problem 5.

Design a differential CMOS VCO in the 0.35um process which can be used for the transmit as well as receive bands for both DCS and PCS (GSM 1800 and 1900). This means it must be able to generate frequencies from 1710MHz to 1990MHz. To achieve some margin for process variations the tuning range must be 1600MHz to 2100MHz.

The phase noise must be below -140dBc/Hz at 3MHz offset at 1990MHz.

A varactor is designed by someone else. This varactor can switch capacitors in and out of the resonator. The ratio of its maximum to minimum capacitance is 4. Its quality factor is so high that the varactor losses can be neglected. The varactor is a scalable design which can be adjusted to any capacitance value needed.

Four different differential inductors are also available:
Inductor 1: Q = 8 in band, L = 2 x 8nH (8nH per side), Self-resonance = 5GHz
Inductor 2: Q = 12, L = 2 x 4nH, Self-resonance = 6GHz
Inductor 3: Q = 12, L = 2 x 8nH, Self resonance = 3GHz
Inductor 4: Q = 14, L = 2 x 4nH, Self-resonance = 4GHz

The sum of parasitic metal routing capacitance and load capacitance is 150fF per side.

The noise factor of the oscillator can be assumed equal to 3.

The drain-bulk capacitance can be assumed equal to 0.5fF per um transistor width.

The supply voltage is 2V and the oscillation amplitude should be 1.5V per side at 1990MHz. (Perfect square-wave current can be assumed.)

The startup loop-gain should be at least 5.

Design a VCO that meets the requirements above using one of the inductors. The following needs to be specified: varactor capacitance range, which inductor is used, bias current, startup loop-gain, transistor dimensions, and gate bias voltage of tail transistor. It must be verified that all requirements are met. Use long channel equations. Also draw a schematic. (6p)

Boltzmann's constant: $k = 1.38*10^{-23}$