Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2005-03-08, 14.00-19.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

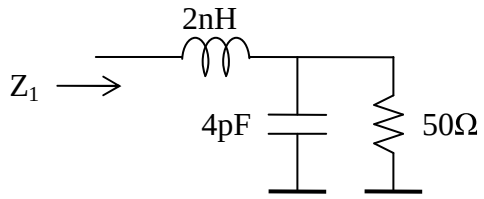
Allowed equipment:

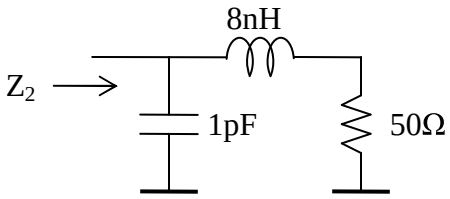
- Textbook: T. H. Lee, “The Design of CMOS RF Integrated Circuits”
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

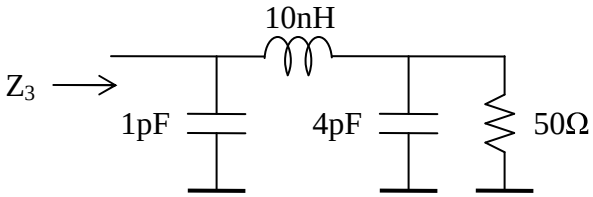
Good luck!

Problem 1.

Three RLC networks according to the figure below are to be investigated. Calculate the frequency where the impedances (Z_1, Z_2, and Z_3) are completely resistive. Also calculate the value of these resistive impedances.

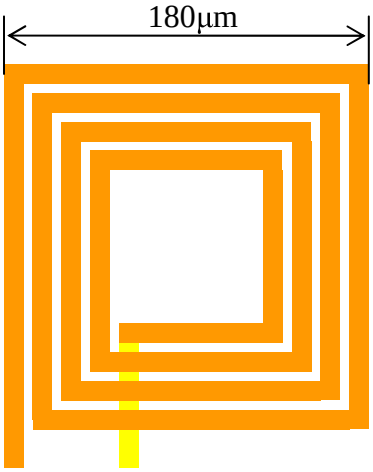




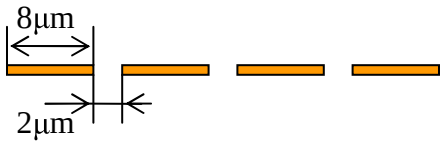


Problem 2.

An inductor is needed for an 1800MHz VCO for a GSM transceiver. The structure below meets the requirements. It is realized in the metal 4 layer of the 0.35um process. (metal 3 is used for the bridge to the center, but its effect can be neglected).



Top view



Side view (different scale)

To simplify the calculations assume the substrate to have infinite conductance. Also assume there are no Eddy currents in the substrate. (The two assumptions are of course not completely realistic.)

a. Calculate the inductance, the series resistance, the Q-factor, and the self-resonance frequency with one terminal grounded. (3p)

b. Calculate all the above for an inductor using both metal 3 and 4 in parallel. Apart from using two metal layers the dimensions of the spiral are the same. The thickness of the spiral can be approximated as the thickness of metal 3 plus the thickness of metal 4, neglecting the thickness of the via layer. (Metal 2 is used for the bridge to the center, but the effect of this can be neglected.) (2p)

c. Which inductor is best suited for an 1800MHz GSM VCO? Motivate! (1p)

Useful constants:
$\mu_0 = 4\pi \cdot 10^{-7}$ Vs/Am
$\rho_{Al} = 27 \cdot 10^{-9}$ Ωm

Problem 3.

Poly-phase filters are to be designed using resistors with an absolute accuracy of ±15% and capacitors of ±10%. Perfect relative accuracy (matching) can be assumed.

a. Design a single stage poly-phase filter which generates quadrature signals from a differential signal at 1GHz. All resistors are to be 500Ω. (1p)

b. Calculate the maximum quadrature error (phase error and amplitude error) at 1GHz due to the low absolute accuracy of R and C for the filter designed in a. (2p)

c. Design a two-stage poly-phase filter with the stages tuned to 800MHz and 1250MHz, respectively. Use a buffer between the stages to simplify the calculations in d. All resistors are still to be 500Ω. (1p)

d. Calculate the maximum quadrature error (phase error and amplitude error) at 1GHz due to the low absolute accuracy of R and C for the filter designed in c. (2p)

Problem 4.

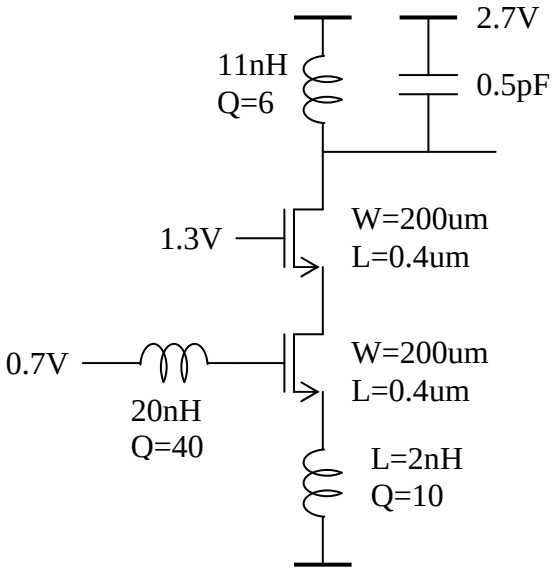
For the LNA below, calculate:

a. The bias point (DC current and voltages). (1p)

b. The resonance frequency at input and output. Neglect drain parasitic capacitances of the cascode transistor. (1p)

c. Input impedance at the input resonance frequency. (1p)

d. The noise figure. Assume the input to be matched and the cascode transistor to add 0.2dB to the noise figure, neglect noise from load. (3p)



Suitable formulas and parameters:

$$F = 1 + \frac{(\delta/5)\cdot(Q^2+1)+\gamma/4}{R_s Q^2 g_m}$$

$$Q = \frac{1}{2\omega_0 R_s c_{gs}},\ \gamma = 2,\ \delta = 4$$

Increase of F due to series resistance R_s in the input circuit:

$$F_{withRs} = F + \frac{R_s}{R_g}$$

Problem 5.

Design a double balanced mixer in the 0.35um process according to the specifications below:

- F_{DSB} < 8dB (relate input voltage noise to that of a 50Ω resistor). The switches and load can be assumed to add 2.0 dB to the noise figure. Neglect input capacitance, and use a γ equal to 1.5.
- Conversion gain (voltage) = 8 dB
- Input related compression point = 0dBm per RF input (related to 50Ω)
- Total bias current < 4mA
- Supply voltage = 3.5V
- Input frequency = 2.14GHz, (output frequency = 0, WCDMA direct conversion)
- Bandwidth at output = 10MHz
- Input capacitance < 0.2pF per RF input
- V_{od} = 0.2V for the switches in the balanced state
- LO amplitude = 400mV (peak) per side. (Total differential peak to peak = 1.6V)

The body effect can be neglected.

A full solution consists of a schematic and sizes for all included components. All required bias voltages must be specified. (6p)