Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2004-03-09, 14.00-19.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

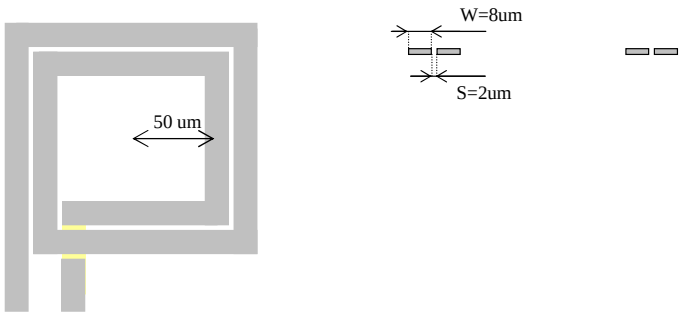
Allowed equipment:

- Textbook: T. H. Lee, “The Design of CMOS RF Integrated Circuits”
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

A set of inductors is fabricated in a 2um thick aluminum metal layer, with 5um thick SiO_2 isolation to the substrate. The inductors are square with a centre hole. For all the inductors the innermost turn has a radius of 50um, the conductor width is 8um, and the spacing is 2um. The set consists of inductors with different number of turns (n). There are four inductors with n=1,2,4,8, respectively. As an example the n=2 inductor is shown below.



For the four inductors (n=1,2,4,8) calculate:

a. The inductance. (2p)
b. The self-resonance frequency with one terminal grounded. The substrate is assumed to be a perfect conductor. Neglect turn-to-turn capacitances and fringing. (2p)
c. Q at 2 GHz. Neglect substrate losses. (2p)

Useful constants:
$\mu_0 = 4\pi \cdot 10^{-7}$ Vs/Am
$\rho_{Al} = 27 \cdot 10^{-9}$ Ωm
$\varepsilon_0 = 8.85 \cdot 10^{-12}$ As/Vm
$\varepsilon_{r,Si\text{-}oxide} = 3.9$

Problem 2.

a. Design a low-pass L-match to transform an antenna impedance of 50Ω to 5Ω for use with a power amplifier at 2GHz. Assume ideal components. (2p)
b. The antenna impedance can vary. For the L-match just designed, calculate the impedance seen by the power amplifier at 30Ω and at 100Ω antenna impedance. (2p)
c. If the power amplifier can deliver a maximum of 4Vpp output voltage and 800mApp output current, what is the maximum power that can be delivered to the antenna in the case of 30Ω, 50Ω, and 100Ω antenna impedance (using the L-match of a.)? (2p)

Problem 3.

You have a differential on-chip inductor with L=2*8nH, Q=12, and a self-resonance frequency of 4GHz. You also have a MOS varactor with minimum length (0.4um) with a C_{max}/C_{min} ratio equal to 2 in the 0.35um process.

Using this inductor and varactor a differential oscillator (see figure below) is to be designed in the 0.35um process of the data sheet. Requirements:

frequency range = 1.8GHz ± 7%

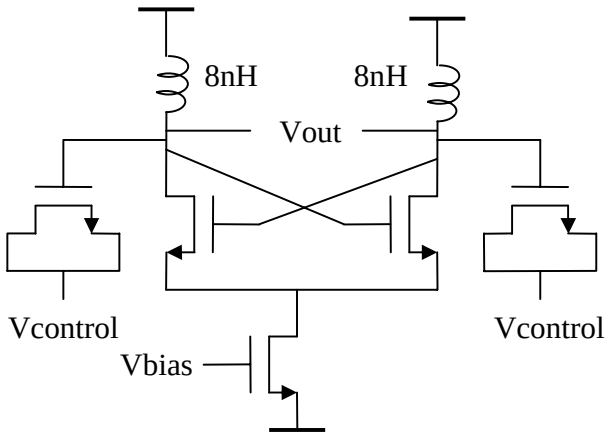
phase noise = -138dBc/Hz at 3MHz offset

startup loop-gain >3

Assume a noise factor F = 3

a. Calculate supply voltage and bias current. Leave 0.5V margin between the negative peaks of the signal and ground. (3p)
b. Calculate the dimensions of the varactor and the other transistors. Use an overdrive voltage equal to 0.2V for the tail current transistor. Calculate Vbias. When calculating the drain-to-bulk capacitances, assume 0V reverse bias (overestimation of cap.). Also assume a finger layout with 1.1um between gates. (2p)
c. Calculate the startup loop-gain for the circuit just designed. (1p)

Useful constant: $kT=4.2 \cdot 10^{-21}$ J



Problem 4.

A differential LNA with 50Ω input impedance per side for 1.575GHz signals (GPS) is to be designed in the 0.35um CMOS process. Low power has higher priority than high linearity. Low noise and high gain are very important. Because of these requirements the inductively source degenerated topology is chosen. The following is given:

Minimum length transistors (0.4um) are to be used

The overdrive voltage must be at least 100mV

Total bias current for the differential LNA is 3mA

Supply voltage = 2V

The noise of the cascode devices and the output load can be neglected, so use the following equations and parameters for noise:

$$F = 1 + \frac{(\delta/5)\cdot(Q^2+1)+\gamma/4}{R_s Q^2 g_m},\ A_v = 2Qg_m R_L,\ Q = \frac{1}{2\omega_0 R_s c_{gs}},\ \gamma = 1.4,\ \delta = 2.8$$

Q is chosen equal to 1.5 to achieve low noise.

Parameters for the inductors, use two of them in the load of the differential LNA:

$$Q_L = \frac{20}{\sqrt{L(\text{nH})}},\quad f_s = \frac{20\text{GHz}}{L(\text{nH})},\quad 1\text{nH} < L < 20\text{nH}$$

a. Draw the schematic. Calculate F, the width of the transistors (use same width for cascode and input device), and the gate bias voltages of the input and the cascode transistors. Also calculate Lg and Ls. (4p)

b. Find the value of the output load inductance giving maximum gain. Also calculate this gain. Assume the next block (mixers) to provide a purely capacitive load of 150fF per side of the differential output (including parasitics of the wires connecting the load to the LNA). A common finger layout of the transistors is assumed, with a gate-to-gate distance of 1.1um. (2p)

Problem 5.

In the GPS receiver two quadrature mixers are needed since we are going to use the low-IF architecture. To achieve low noise and some gain active mixers are chosen. We use double-balanced mixers with resistive loads. Requirements:

Vdd=2V, 0.35um process, Idc=1mA/mixer, Voltage conversion gain=5dB

LO amplitude = 1Vpp (single-ended)

The two transistors in a switch pair may not conduct simultaneously for more than 15% of the time.

An input signal of 0.2V (single-ended) must be handled without clipping. Assume the output to be a pure IF signal with high frequency components filtered off.

a. Draw the schematic. Calculate the width of the transistors (minimum length is assumed), the gate bias voltages of the input and the switch transistors, and the load resistances so the requirements are fulfilled. No transistors may turn off or enter the triode region at maximum input signal, either at the LO zero crossing or at the peak of the LO signal. (5p)

b. Calculate the capacitive load seen by the LNA in the previous problem due to the two mixers. Assume a 50fF routing capacitance per side.
Is the budget of 150fF per side kept? What is the resonance frequency of the LNA output circuit with this load if nothing is re-designed? (1p)