Lund University
Dept. of Electroscience

ETI170

Written Exam
Integrated Radio Electronics

2003-03-11, 14.00-19.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

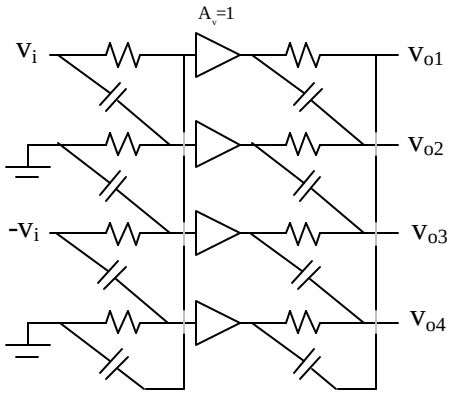
Allowed equipment:

- Textbook: T. H. Lee, "The Design of CMOS RF Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1.

A poly-phase filter according to the figure below is used to generate quadrature signals at 1GHz.



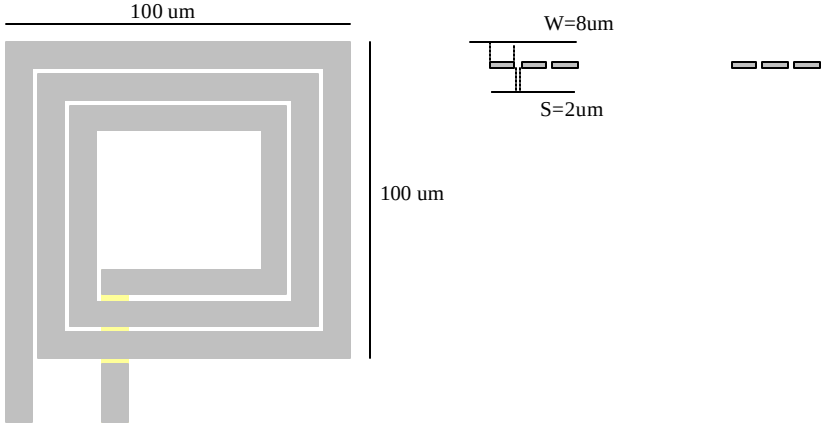
(The buffer amplifiers between the stages simplify the calculations)

Assume the matching to be perfect, but the RC-product to have an accuracy of ±30%. Therefore the frequency of the first link is to be chosen 20% above 1GHz, and of the second 20% below 1GHz. All resistors are to be 1kO.

a. Calculate the value of all resistors and capacitors. (2p)
b. Calculate the phase error at 1GHz if all R's and C's have nominal values. (2p)
c. Calculate the amplitude error at 1GHz under the same assumption as in b. (2p)

Problem 2.

An inductor is fabricated in metall3 in the 0.35um process according to the figure:



a. Calculate the inductance L. (2p)
b. Calculate the series-resistance in the metal including skin effect at 5GHz. What is the Q-value regarding just this metal-loss? (2p)
c. Calculate the capacitance to the substrate (which is assumed to be a perfect conductor). Neglect capacitances due to edges, and between turns. Calculate the self-resonance frequency when one terminal is grounded. (2p)

Problem 3.

A VCO must fulfill the following phase-noise specification:

? f	Phase Noise (dBc/Hz)
100 kHz	-100
1 MHz	-130
3 MHz	-140
10 MHz	-150

(The phase noise of the VCO must not exceed the specification at any point)

Assume the $1/f^3$ noise corner to be at 300kHz. Which point in the table is the most difficult to fulfill? (1p)

If the frequency of oscillation is 2GHz, F = 2, Q = 10, the efficiency converting battery to tank energy is 50%, and the phase noise requirements are to be fulfilled with 3dB margin, how much (battery) energy will the oscillator at least require? (2p)

If the supply voltage is 2V and a differential N-transistor only topology is chosen, how much inductance L per side should be used? (The total differential inductance of the resonance tank is 2L) (1p)

If the tuning-range is to be 1.85GHz to 2.2GHz, and the ratio between maximum and minimum capacitance of a 0.4um long MOS varactor is equal to two, how wide should the varactor be (the length is chosen to 0.4um for maximum Q)? Use the parameters of the 0.35um process. (2p)

Problem 4.

A very low noise LNA is needed to receive the weak 1.575GHz satellite signals in a GPS receiver. The inductively source degenerated topology is therefore chosen. To reduce the sensitivity to package and bondwire parasitics, a differential topology is chosen.

Given: R_s =50O/side, Vdd=2.7V, Idc=2mA (1mA/side), the load inductor has Q_L=5 and L=10nH (per side), parameters from the 0.35um process datasheet.

Use the following equations and parameters:

$$F = 1 + \frac{(d/5)\cdot(Q^2+1) + g/4}{R_s Q^2 g_m}\ ,\ A_v = 2Q g_m R_L\ ,\ Q = \frac{1}{2w_0 R_s c_{gs}}\ ,\ g = \frac{4}{3},\ d = \frac{8}{3}$$

Q is chosen equal to two to achieve low noise and at the same time a relatively high gain. The transistor length is chosen minimal to maximize the gain. Cascode devices are used to ensure stability.

Problem 4 continued:

a. Draw the schematic. Calculate transistor widths, inductance values (L_s and L_g), and transistor gate bias voltages. (2p)

b. Calculate the gain. (1p)

c. Calculate the noise factor F, regarding just the noise of the input transistors. (1p)

d. Calculate the noise factor F, regarding also the noise of the cascode devices. A common layout of the input- and cascode transistors is assumed, with a minimum gate-to-gate distance of 0.6um. (2p)

Problem 5.

A double balanced active mixer with resistive loads is to be used in a WCDMA direct conversion receiver with high requirements on linearity and LO to RF isolation.

Given: Vdd=2.7V, V_{LO}=1V_{pk} (single-ended), f_{RF}=f_{LO}=2.14GHz

Requirements:

- Conversion gain > 6dB
- No clipping for an input voltage amplitude that would give at total of 5dBm in two (imagined) input resistors of 50O per sida. (WCDMA => high linearity)
- F < 6dB (DSB), use a thermal noise coefficient $g = \frac{4}{3}$

  Just the input stage has to be regarded. The noise factor F is calculated by comparing the input noise voltage to the noise of a 50O resistor.
- The switching instants (all switches conducting simultaneously) will take place for 10% of the time.

a. Draw the schematic, and calculate component parameters and bias voltages. How much current is needed? (4p)

b. Assume a mismatch in the threshold voltages of the switch transistors, according to the equation:

$$s(\Delta V_t) = \frac{9}{\sqrt{W(\mu m) \cdot L(\mu m)}} \text{ mV}$$

Assume further that this causes a signal at the LO frequency with an amplitude equal to s in the source nodes of the switch-transistors. (The signal is assumed to be in opposite phase in the two nodes.) If the mixer is driven by an LNA with 500O resistive output impedance per side (the input impedance of the mixer is assumed to be resonated away) and a reverse voltage gain of -30dB, what is the LO leakage to the antenna after the differential signals have been combined in an ideal balun? Can the WCDMA specification allowing a maximum -60dBm leakage to the antenna be fulfilled? (2p)