

Examination
Integrated Radio Electronics

2001-03-06 14⁰⁰-19⁰⁰

The examination consists of 5 problems which each can give up to 6 points. The total maximum is thus 30 points. To pass the examination requires at least 15 points.

Important:

- Always start **a new problem on a new piece of paper**
- Write **name and page number on all papers**
- Sort the papers according to page number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points is not always proportional to difficulty

Allowed to bring:

- Textbook
- TEFYMA or similar mathematical and physical table of constants and formulas
- Datasheet for the CMOS process
- Pocket calculator

Good luck!

Problem 1.

- Design a phase-shifting network that from **one** input signal at 1GHz creates two output signals with equal amplitudes and 90 degrees phase difference. All resistors should be 500Ω . (2p)
- What is the input impedance when the outputs are unloaded (open)? (2p)
- Within which frequency range is the difference between the amplitudes of the output signals less than 5%? (2p)

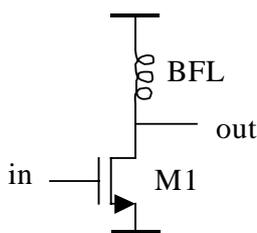
Problem 2.

- Derive the equation $IRR \approx \frac{4}{(\Delta\phi)^2 + \epsilon^2}$ (2p)
- Bluetooth is well suited for low-IF since about just 20 dB IRR is sufficient. How many degrees $\Delta\phi$ does this correspond to if $\epsilon = 0$, and how many percent amplitude error ϵ does it correspond to if $\Delta\phi = 0$? (1p)

In mobile phones you have near-far problems. Suppose you want to design the receiver of a mobile telephone using a low-IF architecture, and near-far problems make the required IRR equal to 80dB. How small must the amplitude and phase errors be to achieve this? (1p)

- In a GPS-receiver using low-IF architecture the image rejection is used to avoid receiving the thermal noise at the image frequency. In this way the noise of the LNA and mixer can be reduced by up to 3dB (compare SSB and DSB noise figure). How large must the IRR be to reduce the noise by 2.5dB? (2p)

Problem 3.



a. A (single-ended) power amplifier is built according to the figure and has a supply voltage of 3V. To maximize the efficiency, you want to use as high as possible output amplitude. Compromises leads to the choice of a $5V_{pp}$ output amplitude. Design LC-networks that transform the antenna impedance to an impedance suiting the amplifier for the two cases below.

- GSM: $R_L = 50\Omega$, $P_{out}=30\text{dBm}$, $f=900\text{MHz}$
- Bluetooth: $R_L = 50\Omega$, $P_{out} = 0\text{dBm}$, $f = 2.4\text{GHz}$

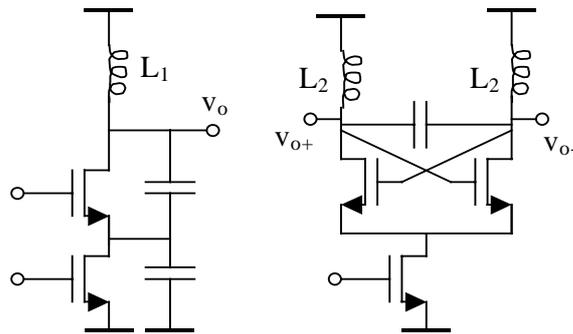
Assume ideal capacitors and inductors. You want the bandwidth of the LC-networks to be as large as possible to reduce the sensitivity to component variations. How large is the current in the inductors? How large is the bandwidth? (2p/case = 4p)

- How large bias current is required for class A operation in the two cases? If the transistor is minimum length and operates in class A, how wide must it be to avoid operating in the triode region at any time?

Observe: The transistor can be large in the GSM case.

(Use long channel equations and the datasheet of the CMOS process) (2p)

Problem 4.



- a. Assume that it is possible to design integrated inductors with a Q of 5 in our $0.35\mu\text{m}$ CMOS process regardless of the inductance value (actually not completely realistic). The capacitor losses are small enough to be neglected. You want to design oscillators for a supply voltage of 1.5V . The transistors are assumed to cause three times as much phase noise (power) as the losses of the inductors. Two oscillators are built according to the figure above. The maximum peak-to-peak output voltage is ideally equal to twice the supply voltage (per side in the differential design), which in this case is 3V . Compromises result in a choice of 2V_{pp} in this case. Determine the size of the inductors in the two oscillators, so that the phase noise requirement of GSM below is fulfilled.

GSM: $-140\text{dBc}/\text{Hz}$ vid 3MHz offset, $f = 900\text{MHz}$, ($T = 293\text{K} = 20$ Celsius)

At this offset (3MHz) the $1/f$ -noise can be neglected and a phase noise falling off with 20dB per decade can be assumed.

from TEFYMA: Boltzmann's constant $k = 1.3807 * 10^{-23} \text{ J/K}$ (2p)

- b. How large is the power consumption of the two oscillators if the efficiency is 50% ? (1p)

- c. Determine the physical dimensions of the different (integrated) inductors. Neglect substrate losses. When calculating the self resonance frequency, assume the substrate to be a perfect conductor. Design inductors with a Q -value of at least 5 and a self resonance frequency of at least twice the oscillation frequency. **If you have not succeeded in solving part a, you can use the inductance values 3nH and 11nH when solving this part (c).**

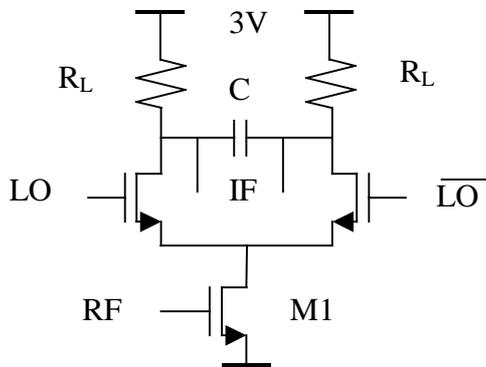
Connecting wires, vias and fringe capacitances may be neglected.

from TEFYMA: $\mu_0 = 4\pi * 10^{-7} \text{ Vs/Am}$

resistivity of Aluminum at 20 Celsius: $\rho = 2.7 * 10^{-2} \Omega\text{mm}^2/\text{m}$ (3p)

Problem 5.

A mixer for a Bluetooth low-IF receiver is to be designed according to the figure below:



$V_{dd} = 3V$
 $I_{dc} = 2mA$
 $f_{LO} = 2.4 GHz$
 $f_{IF} = 3MHz$
 $V_{LO} = 1V_{pp} / side$

Use the datasheet of the 0.35 μm CMOS-process

- a. Assume for a start that no parasitic capacitances exist and that the switches are ideal.

Determine the dimensions and select operating points for M1, R_L and C so that $G_c = 20dB$ voltage gain, the bandwidth at the output exceeds 8MHz, the LO leakage to the IF port is less than 10mVpp per side, and the output voltage can be up to 2Vpp per side. The switches are assumed to be ideal as long as the output nodes are at least 1V above ground, then they enter the triode region.

Which will have largest influence on the compression point in this case, the non-linearities of the output or the input? (3p)

- b. Calculate the dimensions of the switch-transistors so that $V_{od} = 0.2V$ in the switching instant ($V_{LO}=0$). If there is a 5% mismatch in c_{gs} between the switch transistors, how large will the LO to RF leakage be? The impedance at the RF port is 500 Ω . (C_{gs1} is assumed to be in resonance with an inductor and can therefore be neglected.) (Make necessary simplifying assumptions.) (3p)