Integrated Radio Electronics

Laboratory 1: Low Noise Amplifiers

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Introduction

In this laboratory you will verify your deign of the low noise amplifier in hand in exercise 1. You will also learn to simulate noise and linearity with GoldenGate.

It is very important that you have done hand in exercise 1 **before** attending the laboratory!

Getting started

```
mkdir rfic2010
cd rfic2010
inittde ana2009
icfb &
```

Create Library and Schematic

First a library and a schematic view must be created:

- Create a new Cadence library called 'RFIC_Labs'. Techfile = 'umc13mmrf'
- Create a schematic cellview in the new library, call it 'LNA'
- Draw the schematic according to the hand in assignment, and put in all component values you have calculated. Use transistor N_12_HSL130E from library umc130mmrf. Use ideal inductors 'ind' from analogLib. The Q value of the inductor can be set by putting a resistor in parallel (or in series) with the inductor.
- Put vdc sources to bias the inputs

Simulations

- Run a DC analysis and check if the bias points agree with your calculations. If the deviation is large, modify the schematic until you get the right bias currents and voltages.
  Hint 1: You can view the DC voltages and operating points using Results->Print or Results->Annotate, try both.
  Hint 2: Use options in the Choose analysis form, type DC in the Outfile prefix. This makes DC analysis results accessible to other analyses.
- Insert a psin source between the input terminals. Separate each bias voltage source from the input terminal with a 5k resistor. Make the impedance of the psin equal to 100 Ohms. Type = sine. DC voltage = 0. Number of frequencies = 1. Sinusoid Frequency 1 = fRF (a variable). Ampl1 = -40 dBm. AC magnitude = 1V. AC phase = 0. Insert a second psin source between the output terminals, with resistance = 50k.
  Save the changes using Design->Check and Save.
- Copy the variable from the schematic with Variables->Copy From Cellview
- Analysis -> Choose, the click on AC
  In the choosing analysis form:
  Simulation frequency = fRF
  Simulation variable = ticked
  Variable name = fRF
  From 100M to 10G, Log, 200 points per decade
  Define some performances:
  Xin=imag(PORT0.z())
  Rin=real(PORT0.z())
  VoltageGain_dB=20*log10(abs(PORT1.v())/abs(PORT0.v()))
- Run the simulation
- Investigate the performances (found under Golden Gate Results)
  A plot of VoltageGain_dB should be included in the lab report
- If necessary, tune the inductors until the circuit performs as expected.
- Set up an S parameter analysis (SP)
  Define a performance: S11=dB(s(1,1))
  The port number of the psin connected to the input should be set to 1 and the psin connected to the output should have port number equal to 2
  (Use the properties of the port to check this, and correct it if needed)
- Run the simulation and plot S11
  A plot of S11 should be included in the lab report
- In the AC analysis form, tick the Compute Noise button and the Compute NCT. This means noise will be simulated, and a Noise Contribution Table generated.
- Run the simulation
- Plot Noise Figure (NF) from Golden GateResults. Noise is found under AC.
- The noise figure will be extremely good! (Too good)

- Also print the NCT table to find the reason for the **unrealistic** noise figure.
- One noise source is missing in the NCT, the gate induced noise.
- Add the this noise source using a 570 Ohm resistor connected between the inputs of a vccs (voltage controlled current source) with the gain 1m Mhos (1mS). The outputs of the vccs should be connected to the gate and the source terminals of the input transistor. One of the input terminals of the vccs should also be connected to ground. Two of these circuits are needed, one for each input device. The values are calculated to correspond to a parameter δ equal to 3 and a frequency of 2.1GHz, at the gm and Cgs corresponding to the values found in the hand-in exercise.
- Design->Check and Save. Run the simulation.
- Plot the noise figure in the same plot as the last simulation (use append).
  This plot of NF with and without gate induced noise should be included in the lab report.
- Now the Carrier Analysis (CR) will be used to find the linearity of the LNA.
- In the psin at the input set the “Amplitude (dBm)” field to -40. The field just below, “Initial phase for Sinusoid”, is set to 0. The next field “Frequency” is set to fRF. Design->Check and Save
- In the Design variables set fRF equal to 2.1GHz. This can be done by double-clicking directly on fRF in the Analog Design Environment window.
- Select the CR analysis. Set fundamental frequency to fRF, and number of harmonics to 5.
- Run the analysis
- Under GoldenGate Results, check the results of the CR analysis. Look at the spectrum of the voltage of the output port.
- Define a performance in the choose analysis form for the CR analysis:
  VoltageGain_dB=dB(PORT1.v(1, 0, 0))-dB(PORT0.v(1, 0, 0))
- Run the simulation and check the voltage gain
- We will now run a sweep to find the 1dB compression point
- In the schematic, for the psin source at the input, change the properties:
  Amplitude (dBm) = pRF, that is a design variable is used for the amplitude. This allows the input power to be swept.
  Design->Check and save.
- In the analog design environment: Variables->Copy from Cellview, Then set pRF to -40.
- In the CR analysis, click the radio button next to “Specification Variable”. Variable name = pRF. Range, from -50 to -10 linear Step 2
- Simulate
- Plot the voltage gain from the CR analysis. Can you find the 1dB compression point?
  This plot should be included in the lab report
- If you have enough time you can try to Gain Compression analysis (GC), and compare the result to the 1dB compression point found by the CR analysis.
- We will now use the IP analysis to find the 3rd order intercept point (IP3)

- For the psin at the input set:
  Amplitude 2 (dBm) = pRF
  Initial phase for sinusoid 2 = 0
  Frequency 2 = fRF2
- Check and save
- Copy the design variables to the analog design environment, and set fRF2 = 2.11G
- Choose IP analysis with
  IP Rank = 3
  Input Sources: Choose the psin connected to the input, choose “Power (dBm)”
  Output probes: Choose the psin connected to the output, choose “Voltage (dBV)”
  Input Freq1 (Hz) = fRF
  Input Freq2 (Hz) = fRF2
- Run the simulation
- In GoldenGate Results for the IP analysis:
  Click the radio buttons “Power Sweep” and “Input IP3”, and click plot
- Is the IP3 as expected given the compression point simulated before?
- Create a new design variable called Vcm, and set the common mode DC voltage at the inputs to Vcm. Then use the Specification Variable in the IP analysis to sweep Vcm from 400m to 600m. Plot Input IP3 versus Vcm. **This plot should be included in the lab report.**

The lab report should contain all the plots indicated. It should also contain comments about the results and about what is seen in the plots.

Additional assignment:
The SpectreRF simulator is very well known and used by many companies. Repeat the simulations of bias (DC analysis), gain and input match (AC), and linearity (PSS). Instructions can be found in the lab manual from 2009, although for an older version of the simulator still valid in most parts.

Getting started with SpectreRF:
First save the state using Session->Save State
Then select Setup->Simulator/Directory/Host, and choose Spectre
Update the design variables and you can start simulating with SpectreRF
Note that there are now different analyses available that you can use.