Chapter 5
The CMOS Inverter

Goal With This Chapter
- Analyze Fundamental Parameters
  - A general understanding of the inverter behavior is useful to understand more complex functions
- Outline
  - Noise
  - Reliability
  - Performance
  - Power Consumption

Robustness
- Noise - “unwanted variations of voltages and currents in logical nodes”
- Classical noise such as thermal and flicker noise are not critical in digital design
- Noise sources in digital circuits are
  - Capacitive coupling
  - Inductive coupling
  - Power and ground noise
Capacitive and Inductive Coupling

A voltage or a current change may influence the signal on a parallel wire, especially when:
- Long wires
- Sub micron tech.
- Many metal layers

Power and Ground Noise

- A big problem on large synchronously clocked chips
- On chip decoupling capacitors helps (≈ 1/10 of the switched C)

Conclusion: The world is not digital. We need to know the limitations

Definitions

- DC Operation
- Noise Margins
- Fan OUT - Fan IN

DC Operation

- Voltage Transfer Characteristic (VTC)
- Switching Threshold $V_M$ when $V_{IN} = V_{OUT}$
  - Balanced if $V_M = V_{DD}/2$
- Logical “1” at $V_{OH}$
- Logical “0” at $V_{OL}$
Analog versus Digital Signals

\[ V_{OH}, V_{OL} = \text{nominal output voltage} \]

\[ V_{IH}, V_{IL} = \text{acceptable input voltage} \]

The noise margins are defined as the difference between \( V_{OH}/V_{OL} \) and \( V_{IH}/V_{IL} \)

\[ NM_H = V_{OH} - V_{IH} \]

\[ NM_L = V_{IL} - V_{OL} \]

Fan-In and Fan-Out

Fan-in = M

Fan-out = N

Fan-in = The number of inputs to the gate

Fan-out = The number of gates that loads the gate

The Ideal Gate

\[ R_{in} = \infty \]

\[ R_{out} = 0 \]

Noise Margin = \( V_{DD}/2 \)

Gain = \( \infty \)
A Real Gate

\[ N_{L} = V_{IL} - V_{OL} = 0.75 - 0.50 = 0.25V \]
\[ N_{H} = V_{OH} - V_{IH} = 3.50 - 2.25 = 1.25V \]
\[ V_{M} = 1.75V \]

Dynamic Definitions

- Propagation delay
- Rise and fall time
- Power consumption

Delay Definitions

\[ t_p = \frac{t_{pHL} + t_{pLH}}{2} \]

Ring Oscillator – minimum \( t_p \)

Odd # of inverters

“De-facto Standard” for performance

Fan-out = 1
Ring Oscillator

Do \( t_p = 100\text{ps} \) mean 10 GHz chip?
Good Custom Design \( \approx 1/10 \)
Synthesized design \( \approx 1/50 - 1/100 \)

Why?

- Low load
- Short Wires
- Fan-out = 1
- Low complexity

Power Dissipation

Two measures are important

- Peak power (Sets wire dimensions)
  \[ P_{\text{peak}} = V_{DD} \times i_{DD_{\max}} \]
- Average power (Battery and cooling)
  \[ P_{\text{av}} = \frac{V_{DD}}{T} \int_0^T i_{DD}(t) \, dt \]

Power-Delay Product

\[ PDP = t_p \times P_{\text{av}} \quad (J) \]

Energy per operation

Energy per switching event

Digital IC-Design

The CMOS Inverter
Inverters

- On-chip resistors are large
- Static power consumption
- $V_{OL} \neq 0$
- Large $t_{PLH}$

- Extra process step
- Static power consumption
- $V_{OL} \neq 0$
- Large $t_{PLH}$

The CMOS Inverter

- + Lower static power consumption
- + $V_{OH} = V_{DD}$; $V_{OL} = 0$
- + $t_{PLH} = t_{PHL}$ if properly designed
- + Low impedance connection to ground and $V_{DO}$
- - More fab. stages
- - Lower hole mobility

- Shared power and ground
- Cascaded abutted cells

Wider PMOS to compensate for lower mobility
CMOS Inverter - Model

- Complementary i.e. output have always a low impedance connection to GND or \( V_{DD} \)

\[
V_{OH} = V_{DD} \quad V_{OL} = 0
\]

\[
V_M = f(R_{eq-n}, R_{eq-p}) \quad V_M = V_{DD}/2 \text{ if } R_{eq-n} = R_{eq-p}
\]

CMOS Static Behavior

- Load characteristics
- VTC
- Switching threshold
- Noise margin

Load Lines

- N-channel
- P-channel

Inverter Load Characteristics

- The VTC can be determined graphically

\[
I_{Dn} = -I_{Dp} \quad V_{in} = V_{DD} - V_{GSp} \quad V_{out} = V_{DD} - V_{DSP}
\]
Inverter Load Characteristics

\( V_{in} = 5V \)
\( V_{in} = 0V \)
\( V_{in} = 1V \)
\( V_{in} = 2V \)
\( V_{in} = 3V \)
\( V_{in} = 4V \)

Region: Linear - Saturation

\( V_{out} = 2V \)
\( V_{out} = 3V \)
\( V_{out} = 4V \)
\( V_{out} = 5V \)

CMOS Inverter VTC

VTC graphically extracted from the load lines

High noise margin

\( N_{M} = V_{out} - V_{in} = 5 - 2.9 = 2.1V \)
\( N_{L} = V_{out} - V_{in} = 2.1 - 0 = 2.1V \)

Switching Threshold

Both transistors are saturated

\[ \frac{k_p}{2} (V_M - V_{th})^2 = \left(-\frac{k_p}{2} (V_M - V_{DD} - V_{tp})^2 \right) \Rightarrow \]
\[ V_M - V_{th} = \sqrt{-\frac{k_p}{k_n} \left(V_M + V_{DD} + V_{tp} \right)} \Rightarrow \]
\[ V_M + rV_M = V_{th} + r(V_{DD} + V_{tp}) \Rightarrow \]
\[ V_M = \frac{V_{th} + r(V_{DD} + V_{tp})}{1 + r} \text{ with } r = \sqrt{-\frac{k_p}{k_n}} \]
**Switching Threshold**

For Long Channel Transistors:

\[ V_M = \frac{r(V_{DD} + V_Tn) + V_Tn}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{-k_p}{k_n}} \]

\( V_{Tn} = V_{Tp} = 0.5 \, \text{V} \)

**Long Channel Transistors**

\[ V_M = \frac{r(V_{DD} + V_Tn) + V_Tn}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{-k_p}{k_n}} \]

**Moderate deviation from**

\( k_p/k_n = 1 \) **gives only small changes in** \( V_M \)

\( W_P = 2W_n \, \text{common to save area, since the change in} \, V_M \, \text{is small} \)

**Switching Threshold: Example**

Inverter with \( W/L = 0.6 \, \mu \text{m} / 0.35 \, \mu \text{m} \)

\( V_{Tn} = 0.50, \quad k_n = 300 \mu \text{m}, \quad V_{Tp} = -0.65, \quad k_p = -103 \mu \text{m} \)

\[ r = \sqrt{\frac{-k_p}{k_n}} = \sqrt{\frac{103 \mu}{300 \mu}} = 0.59 \]

\[ V_M = \frac{r(V_{DD} + V_Tp) + V_Tn}{1 + r} = \frac{0.59(3 - 0.65) + 0.5}{1 + 0.59} = 1.18 \, V \]

\[ V_{DD} = 3 \, \text{V} \]

**Simulated VTC: Short Channel**

Balanced 0.25\(\mu\text{m} \) inverter
Minimum sized 0.25\(\mu\)m transistors

PMOS

NMOS

Move the PMOS part to the first quadrant

The threshold \(V_M\) is when \(V_{IN}=V_{OUT}\)
Switching Threshold: Short Channel

Both NMOS and PMOS are velocity saturated

\[ k_s ((V_M - V_n) W_{DSATn} - \frac{V_{DSATn}^2}{2}) = k_p ((V_{DD} - V_M + V_p) W_{DSATp} + \frac{V_{DSATp}^2}{2}) \]

Solving \( V_M \) yields

\[ V_M = \frac{V_n + V_{DSATn} + r (V_{DD} + V_p + \frac{V_{DSATp}}{2})}{1 + r} \]

where \( r = \frac{k_p W_{DSATp}}{k_s W_{DSATn}} \)

Example 0.25 \( \mu \)m technology

Minimum transistor dimensions

\[ V_{DSAT} = 0.63; \quad V_{VTH} = -1; \quad V_n = 0.43; \quad V_p = -0.4; \]

\[ k_s = 0.375 \times 115 = 172.5; \quad k_p = 0.375 \times (-30) = -45 \]

\[ r = \frac{k_p V_{DSATp}}{k_s V_{DSATn}} = \frac{-45 	imes (-1)}{172.5 \times 0.63} = 0.41 \]

\[ V_M = \frac{V_n + V_{DSATn} + r (V_{DD} + V_p + \frac{V_{DSATp}}{2})}{1 + r} = \frac{0.43 + 0.63 + 0.41 \left(2.5 - 0.4 - \frac{1}{2}\right)}{1 + 0.41} = 1.0 \text{ V} \]

Example 0.25 \( \mu \)m technology

IF \( V_{DD} >> V_{DSAT} \) and \( V_T \)

\[ V_M = \frac{V_n + V_{DSATn}}{1 + r} \]

\[ V_M = \frac{0.41 \times 2.5}{1 + 0.41} = 0.73 \text{ V} \]

\( V_{DD} \) not high enough in this case

Balancing the inverter

It is desirable to have \( V_M \) around \( V_{DD}/2 \)

\[ k_s W_n ((V_M - V_n) W_{DSATn} - \frac{V_{DSATn}^2}{2}) = k_p W_p ((V_{DD} - V_M + V_p) W_{DSATp} + \frac{V_{DSATp}^2}{2}) \]

Assuming \( L_n = L_p \) yields

\[ \frac{W_n}{W_p} = \frac{k_s ((V_M - V_n) W_{DSATn} - \frac{V_{DSATn}^2}{2})}{k_p ((V_{DD} - V_M + V_p) W_{DSATp} + \frac{V_{DSATp}^2}{2})} \]
Balancing the inverter

Example using the same data

\[ W_p^{nM} = \frac{k_i(V_M - V_D) W_{25cm} - V_{25cm}^2}{2} = \frac{115 \times (1.25 - 0.43) \times 0.63 - (0.63^2)}{2} = 3.5 \]

To be balanced, the PMOS should be 3.5 times wider than the NMOS

For the minimal NMOS with \( W_n = 0.375 \mu m \), the corresponding PMOS has \( W_p = 1.3 \mu m \)

\[ V_M \] is rather insensitive to changes in the device ratio

A ratio decrease from 3.5 to 2 yields \( V_M = 1.13 \) V which is acceptable

Saves area

Determining \( V_{IH} \) and \( V_{IL} \)

\( V_{IH} \) and \( V_{IL} \) when the slope is -1

\[ \frac{\partial V_{OUT}}{\partial V_{in}} = -1 \]

A reasonable approximation is to use the gain (\( g \)) around \( V_M \)

\[ g = \frac{\Delta V_{OUT}}{\Delta V_{in}} \]
Determining $V_{IH}$ and $V_{IL}$

$$g = \frac{\Delta V_{OUT}}{\Delta V_{in}}$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$V_{IH} = V_M - \frac{V_{DD} - V_M}{g}$$

The Inverter Gain ($g$)

$g = -\frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \approx -\frac{1+r}{(V_M - V_t - \frac{V_{DSAT}^2}{2})(\lambda_n - \lambda_p)}$

Note that the gain is very sensitive to the channel-length modulation

Noise Margins

$V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$

$V_{IH} = V_M - \frac{V_{DD} - V_M}{g}$

$NM_H = V_{DD} - V_{IH}$; $NM_L = V_{IL}$

Example (Minimum sized transistors)

$$g = -\frac{1+r}{(V_M - V_t - \frac{V_{DSAT}^2}{2})(\lambda_n - \lambda_p)} = -\frac{1+0.41}{(1-0.43 - 0.63(0.06+0.1))} = -34.6$$
Example (Minimum size transistors)

\[ V_{IL} = V_D + \frac{V_{DD} - V_I}{g} = 1 + \frac{2.5 - 1}{-34.6} = 0.96 \text{ V} \]

\[ V_{IH} = V_D + \frac{V_{DD} - V_O}{g} = 1 - \frac{1}{-34.6} = 1.03 \text{ V} \]

\[ NM_{IH} = V_D + (V_{DD} - V_{IH}) = 2.5 - 0.96 = 1.54 \text{ V} \]

\[ NM_L = V_{IL} = 1.03 \text{ V} \]

Slightly to large values due to the approximation

CMOS Dynamic Behavior

\[ \sim \text{ Capacitors} \]

\[ \sim \text{ Propagation delay} \]

\[ \sim \text{ Power consumption} \]

Inverter Load

Capacitance model for propagation delay calculations

\[ V_{in} \quad V_{out} \quad C_L \]

\[ V_{in} \quad C_{gd1} \quad C_{ab1} \quad V_{out} \quad C_{gd2} \quad C_{ab2} \quad V_{out2} \]

\[ C_{gd1} = \text{Overlap Capacitance} \]

\[ C_{ab} = \text{Junction Capacitance} \]

\[ C_w = \text{Wire Capacitance} \]

\[ C_g = \text{Overlap & Gate Capacitance} \]
The Miller Effect

If \( C_{gd} \) is modeled from \( V_{out} \) to \( GND \), the value shall be doubled.

\[
C_{gd} = 2 \times C_{gd0} \times W
\]

\( C_{db} \) - Junction Capacitance

\[
C_{db} = K_{eq} \times C_{j0}
\]

- Depends on grading coefficient
- Diode area and perimeter

\( C_{w} \) - Wire Capacitance

- Neglected on short distances
- Increased importance in new technologies
Channel Capacitance

<table>
<thead>
<tr>
<th>Region</th>
<th>$C_g$</th>
<th>$C_{gs}$</th>
<th>$C_{gd}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cut off</td>
<td>$C_{ox}WL_{eff}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Linear</td>
<td>0</td>
<td>$(1/2)C_{ox}WL_{eff}$</td>
<td>$(1/2)C_{ox}WL_{eff}$</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>$(2/3)C_{ox}WL_{eff}$</td>
<td>0</td>
</tr>
</tbody>
</table>

Cut off: No channel $\Rightarrow C_g = C_{GB}$
Linear: Channel $\Rightarrow$ Divide channel in two parts
Saturation: $\approx 2/3$ Channel connected to source

Inverter Load Model

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd}$</td>
<td>$2C_{gd}W$</td>
</tr>
<tr>
<td>$C_{db}$</td>
<td>$K_{eq}(AC_j+PC_{jsw})$</td>
</tr>
<tr>
<td>$C_g$</td>
<td>$C_{gd}W+C_{ox}WL$</td>
</tr>
<tr>
<td>$C_w$</td>
<td>Area + Fringe Cap.</td>
</tr>
</tbody>
</table>

$\triangleright$ The values differ for $n$- and $p$-channel
$\sim$ The values differ for L to H / H to L
$\downarrow$ See table 5-2

$C_g$ - Gate Capacitance

$\triangleright$ Overlap – $C_{gs}$ (Not $C_{gd}$)
$\sim$ Channel – $WLC_{ox}$

Inverter - Transient Response

$$V_{out} = (1 - e^{\frac{t}{RC}})V_{DD}; \quad t_r = t_{90} - t_{10}$$
$$0.1V_{DD} = (1 - e^{\frac{t_{90}}{RC}})V_{DD} \iff 0.9 = e^{\frac{-t_{90}}{RC}} \iff$$
$$t_{90} = -RC \ln(0.9)$$
$$t_{10} = -RC \ln(0.1)$$
$$t_r = t_{90} - t_{10} = (-\ln(0.1) + \ln(0.9))RC = t_r = 2.2RC$$
$$t_{pH} = t_{90} = -\ln(0.5)RC = t_{pH} = 0.69RC$$
Chapter 5

The CMOS Inverter

Cont.

**Graphical Method**

\[ I_{D_{VDD/2}} = 145 \, \mu A; \quad I_{D_{VDD}} = 153 \, \mu A; \]

\[ \begin{align*}
R_{eq-n} &= \frac{1}{2} \left( \frac{V_{DS}}{I_{D} (V_{OUT}=V_{DD})} + \frac{V_{DS}}{I_{D} (V_{OUT}=V_{DD}/2)} \right) \\
&= \frac{2}{153 \times 10^{-6} + 145 \times 10^{-6}} = 10 \, k\Omega
\end{align*} \]
**$R_{eq}$ in Short Channel Transistors**

Model Based Method

\[
R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT} (1 + \lambda V_{DD})} + \frac{V_{DD}}{2} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right)
\]

with \( I_{DSAT} = k \left( V_{DD} - V_T \right) \left( \frac{V_{DD}^2}{2} \right) \) In Velocity Saturation

---

**$R_{eq}$ for Short Channel NMOS**

Find \( I_{DSAT} \)

\[
V_{DD} = 2 \text{ V}; \quad V_T = 0.43 \text{ V}; \quad V_{DSAT} = 0.63 \text{ V}; \quad k_n = 115 \text{ mA/V}^2
\]

\[
W = 0.375 \mu\text{m}; \quad = 0.25 \mu\text{m}
\]

\[
I_{DSAT} = k_n \frac{W}{L} \left( V_{DD} - V_T \right) \left( \frac{V_{DD}^2}{2} \right)
\]

\[
I_{DSAT} = 115 \frac{0.375}{0.25} \left( 2 - 0.43 \right) \left( 0.63 \right) = 136 \mu\text{A}
\]

$I_{DSAT} = I_D$ when $V_{DS} = 0$ (extrapolated)

---

**Inverter - Transient Response**

\[
C_L = 2 \text{ fF}; \quad R_{eq-n} = 10 \ k\Omega
\]

\[
t_r = 2.2RC = 2.2 \times 10^{-10} \times 2 \times 10^{-15} = 44 \text{ ps}
\]

\[
t_{pHL} = 0.69RC = 0.69 \times 10^{-10} \times 2 \times 10^{-15} = 14 \text{ ps}
\]
Inverter - Propagation Delay

Long Channel Transistors

\[ Q = C \times \Delta U = C_i \left( V_{OH} - V_{OL} \right)/2 = C_i V_{DD}/2 \]

\[ t_{pHL} = \frac{C_i V_{DD}}{k_i (V_{DD} - V_T)^2} \approx \frac{C_L}{k_i^{\prime} V_{DD}} \]

\[ t_p = \frac{C_i}{2V_{DD}} \left( \frac{1}{k_n} + \frac{1}{k_p} \right) \]

Ideal \( V_{in} \) (Step)

Propagation Delay (page 202)

Short Channel Transistors

\[ t_{pHL} = 0.69 \frac{3 C_i V_{DD}}{4 I_{DSAT}} = 0.52 \frac{C_i V_{DD}}{k_i^{\prime} V_{DSAT} \left( V_D - V_T - \frac{V_{DSAT}}{2} \right)} \]

Ideal \( V_{in} \) (Step)

Propagation Delay Simulation

Short Channel Transistors

Fan-Out = 1

\[ \beta = \frac{W_p}{W_n} \]

\[ \beta = 3.5 \text{ balance the inverter} \quad (V_M = V_{DD}/2) \]

\[ \beta = 2 \text{ (or 2.4) for equal delays} \quad (t_{pHL} = t_{PHL}) \]

\[ \text{However, } \beta = 2 \text{ might be acceptable} \quad (V_M \approx 0.45 \ V_{DD}) \]

What Ratio Should be Chosen?

Short-channel Transistors

Fan-Out = 1
Effect of Input Rise Time

\[ t_{pHL} \text{ [ns]} = \sqrt{t_{pHL\text{ [step]}}^2 + t_{\text{rise}}^2 / 4} \]

Note the gain

Digital IC-Design

Driving a Large Fan-out

Typical examples:
- Busses
- Clock network
- Control wires (e.g., set and reset signals)
- Memories (driving many storage cells)

Worst case:
- Off chip signals

Inverter Chain

\( \text{In} \rightarrow \text{Out} \)

If \( C_L \) is given:
- How many stages are needed to minimize the delay?
- How to size the inverters?
Inverter with Load (External only)

\[ t_p = 0.69 R_{eq} C_{ext} \]

Internal (intrinsic) load is neglected
Not the case in modern technologies

Inverter with Internal Load

\[ t_p = 0.69 R_{eq} (C_{int} + C_{ext}) \]

Self-loading if \( C_{int} \) dominate
Should be avoided

Device Sizing (W scaled with S)

Driving Large Capacitances

\[ C_{int} = \text{Intrinsic capacitance} \]
\[ C_{ext} = \text{Extrinsic capacitance} \]
\[ R_{eq} = \text{Resistance in channel} \]
\[ C_{ext} = C_w + C_g \]
\[ C_w = \text{Wire capacitance} \]
\[ C_g = \text{Gate C in next stage} \]
Scaling to Increase Driving Capability

Scaling $W$ with a factor $S$:

$$C_{int} = S \times C_{ref}$$

$$R_{eq} = \frac{R_{ref}}{S}$$

Scaling to increase driving capability

Delay RC-model

$$t_p = 0.69 R_{eq} (C_{int} + C_{ext}) = 0.69 R_{eq} C_{int} (1 + \frac{C_{ext}}{C_{int}})$$

Scaling with a factor $S$

$$t_p = 0.69 \frac{R_{eq}}{S} C_{ref} (1 + \frac{C_{ext}}{S C_{ref}}) = t_{p0} (1 + \frac{C_{ext}}{S C_{ref}})$$

$\checkmark$ $t_{p0}$ = intrinsic delay
$\checkmark$ Independent of $S$

Scaling Example (page 206)

$t_{p0} = 19.3 \, ps$; $C_{ext} = 3.15 \, fF$; $C_{ref} = 3.0 \, fF$

$$t_p = t_{p0} (1 + \frac{C_{ext}}{S C_{ref}}) = 19.3 (1 + \frac{1}{1.05 \times S}) \, ps$$

Scaling Example (page 206)

$$t_p = 19.3 \times (1 + \frac{1}{1.05 \times S}) \, ps$$

$S = 5$, Substantial improvement

$S > 10$, "No more gain"
Sizing a Chain of Inverters

$\gamma = \text{Capacitive proportionality factor for each inverter}$

- Technology Dependent
- Independent of the size ($W$)
- Close to 1 in Submicron

The in- and output capacitive ratio

$$C_{g,j+1} = \frac{C_{int,j}}{C_{g,j}}$$

$f = \text{The loading capacitive ratio in two following stages}$

Total Delay:

$$t_p = t_{p0} \sum_{j=1}^{N} \left( 1 + \frac{f_j}{\gamma} \right)$$

If each stage is scaled with the same factor $f$
Sizing a Chain of Inverters

\[ f = \frac{C_{g,1}}{C_{g,1}} \]
\[ f^2 = \frac{C_{g,1}}{C_{g,1}} \]
\[ f^3 = \frac{C_{g,1}}{C_{g,1}} = F \] (F = overall effective fan-out)

\[ f = \sqrt{N} \frac{C_f}{C_{g,1}} = \sqrt{F} \]

Known

Sizing a Chain of Inverters

\[ f = e^{(1+\frac{\gamma}{f})} \]

Has no closed form solution except for \( \gamma = 0 \)

\( \gamma = 0 \) when intrinsic capacitance is neglected

\[ f = e \]

Otherwise: \( f \) is solved numerically

Sizing a Chain of Inverters

\[ t_p = t_{p0} \sum_{j=1}^{N} \left(1 + \frac{f_j}{\gamma} \right) = N \times t_{p0} \left(1 + \frac{\sqrt{F}}{\gamma} \right) = \]

Optimum is found by setting the derivative to 0

\[ f = e \]

Sizing a Chain of Inverters

\[ f = \frac{C_{g,j,i+1}}{C_{g,j}} \]

Normalized delay \( \frac{t_j}{t_{p0}} \)

Too many stages

Common Practice
Around 4
Buffer Design

<table>
<thead>
<tr>
<th>N</th>
<th>f</th>
<th>t₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>64</td>
<td>65</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
<td>18</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>15</td>
</tr>
<tr>
<td>4</td>
<td>2.8</td>
<td>15.3</td>
</tr>
</tbody>
</table>

Inverter Chain

Common practice:
Optimum fan-out around \( f = 4 \)

Digital IC-Design

Power Consumption

Dynamic Power Consumption

Energy charged in a capacitor
\[ E_C = \frac{C V^2}{2} = \frac{C_L V_{DD}^2}{2} \]

Energy \( E_C \) is also discharged, i.e.
\[ E_{dis} = C_L V_{DD}^2 \]

Power consumption
\[ P = f C_L V_{DD}^2 \]
Dynamic Power Consumption

Note: The power is dissipated in the transistor resistance, $R_{eq}$

However: the power consumption is independent of the value of $R_{eq}$

$P = C_L V_{DD}^2 f$

Static Power Consumption

$I_{leakage}$ increases with decreasing $V_T$

$P_{stat} = I_{leakage} \times V_{DD}$

Current Spikes – Direct Path

Current peak when both N- and PMOS are open

$E_{dp} = V_{DD} \frac{I_{peak} \times t_d}{2} + V_{DD} \frac{I_{peak} \times t_f}{2} - \frac{t_f \times I_{peak}}{2} V_{DD} I_{peak}$

$P_{dp} = \frac{t_f \times I_{peak}}{2} V_{DD} I_{peak} f$

Dynamic vs. Static Power

The dynamic and static power is about equal in the 65 nm Technology

Source: ITRS
Power-Delay Product

- Helps to measure the quality of different circuit topologies
- Energy per switching event
- For static CMOS

\[ PDP = \frac{P \times t_p}{2} = \frac{C_L \times V_{dd}^2 \times f_{sw} \times t_p}{2} = \frac{C_L \times V_{dd}^2 \times \frac{t_p}{2}}{2} = \frac{C_L \times V_{dd}^2}{2} \quad (J) \]

- Independent of operating frequency

Some claims that EDP is a better measure since it includes the delay.

Some Examples - Cascaded Inverters

Minimal Design

Compensated to Decrease \( t_{PLH} \)

\( R_{\text{res}} = 10 \ \text{k}\Omega \); \( R_{\text{res}} = 30 \ \text{k}\Omega \);
\( C_{\text{良}} = 4 \ \text{fF} \)
\( R_{\text{res-comp}} = 10 \ \text{k}\Omega \); \( R_{\text{comp}} = 15 \ \text{k}\Omega \);
\( C_{\text{comp}} = 6 \ \text{fF} \)
Propagation Delay

- $R_{pp} = 10 \, k\Omega$; $R_{npp} = 30 \, k\Omega$; $R_{npp} = 15 \, k\Omega$;
- $C_{pp} = 4 \, fF$; $C_{npp} = 6 \, fF$; $V_{DD} = 2 \, V$
- $t_{p,pp} = 0.69 \times C_{pp} \times R_{pp} = 28 \, ps$
- $t_{p,npp} = 0.69 \times C_{npp} \times R_{npp} = 83 \, ps$
- $t_{p,comp} = 0.69 \times C_{comp} \times R_{pp} = 41 \, ps$
- $t_{p,ncomp} = 0.69 \times C_{comp} \times R_{npp} = 62 \, ps$
- Not much faster but more symmetric

Power Consumption at Max Speed

- $C_{min} = 4 \, fF$; $C_{comp} = 6 \, fF$; $V_{DD} = 2 \, V$
- $f_{min} = \frac{1}{2\,f_p} = 9.1 \, GHz$; $f_{comp} = \frac{1}{2\,f_p} = 9.7 \, GHz$
- $P_{min} = C_{min} \times V_{DD}^2 \times f_{min} = C_{min} \times \frac{V_{DD}^2}{2\,f_p} = 140 \, \mu W$
- $P_{comp} = C_{comp} \times V_{DD}^2 \times f_{comp} = C_{comp} \times \frac{V_{DD}^2}{2\,f_p} = 230 \, \mu W$

Power-Delay Product

- $PDP = P \times t_p = C_L \times V_{DD}^2 \times f_{p,peak} \times t_p = \frac{C_L \times V_{DD}^2}{2\,f_p}$ (J)
- $PDP_{min} = \frac{C_{min} \times V_{DD}^2}{2} = 8 \, fJ$
- $PDP_{comp} = \frac{C_{comp} \times V_{DD}^2}{2} = 12 \, fJ$

Compensating gives higher energy per switching event

Total Power Consumption and PDP

- $P_{tot} = P_{dyn} + P_{dp} + P_{stat}$
- $= C_L \times V_{DD}^2 \times f + \frac{t_r + t_f}{2} \times V_{DD} \times I_{peak} \times f + I_{leakage} \times V_{DD}$
- $PDP = P \times t_p = \frac{C_L \times V_{DD}^2}{2}$ (J)