Chapter 3
The Devices

This chapter will
- Present intuitive understanding of the device operation
- Introduce basic device equations
- Introduce models for manual analysis
- Show secondary and deep-sub-micron effects
- Show future trends

The Diode

Diode - The simplest IC-device

One-dimensional

IC-structure

pn-junctions

Thin transition = abrupt junction

p+

n+

SiO₂

Metal

Semi-conductor
The Diode in an IC-device

- Diodes appear reverse biased in all MOS-transistors
- They have parasitics that affects the performance (speed, power)
- Protects input devices against static charges

The Diode – Static Models

Exponential First Order

\[ I_D = I_s \times \left( \frac{V_D}{V_{Don}} \right) - 1 \]

The Diode – a One Way Conductor

The diode current \( I_D \) has an exponential behavior regarding the voltage \( V_D \)

\[ I_D = I_s \times \left( e^{\frac{V_D}{V_{Don}}} - 1 \right) \]

Forward biased

Backward biased

Forward “not allowed”

The Diode – Dynamic Behavior

- Affects the maximum speed (how fast the charges can be removed)
- Affects the dynamic power consumption
- The diode can be seen as a capacitor
- Charges are built up around the \( pn \)-junction
Junction Capacitance (abrupt junction)

Strongly non-linear capacitance

\[ C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\Phi_0})^{1/2}} \text{ F/m}^2 \] (derived at page 82)

- \( C_{j0} \) is the zero-bias capacitance in \( \text{F/m}^2 \) (when \( V_D = 0 \))
- \( \Phi_0 \) is the built-in potential

\( C_{j0} \) and \( \Phi_0 \) are physical device parameters

Junction capacitance – Example 3.3

Determine the junction capacitance for

- Junction area \( A_j = 0.5 \mu\text{m}^2 \)
- \( C_{j0} = 2 \times 10^{-3} \text{ F/m}^2 \)
- \( \Phi_0 = 0.64 \text{ V} \)
- \( V_D = 2.5 \text{ V} \)

\[ C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\Phi_0})^{1/2}} = \frac{2 \times 10^{-3}}{(1 - \frac{2.5}{0.64})^{1/2}} = 0.9 \times 10^{-3} \text{ F/m}^2 \]

Example 3.3 - Continued

Determine the junction capacitance for

- \( C_{j0} = 2 \times 10^{-3} \text{ F/m}^2 \)
- \( \Phi_0 = 0.64 \text{ V} \)
- \( V_D = -2.5 \text{ V} \)

\[ C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\Phi_0})^{1/2}} = \frac{2 \times 10^{-3}}{(1 - \frac{2.5}{0.64})^{1/2}} = 0.9 \times 10^{-3} \text{ F/m}^2 \]

Small but billions of them give a high total capacitance

\[ C_{\text{total}} = A_j \times C_j = 0.50 \times 10^{-12} \times 0.9 \times 10^{-3} = 0.45 \times 10^{-15} = 0.45 \text{ fF} \]
Junction capacitance

- Abrupt and graded junctions

![Graph showing abrupt and graded junctions with capacitance C(fF) and voltage V_D(V) plotting.]

\[ A_0 = 0.5 \ \mu m^2 \]
\[ C_{j0} = 2 \times 10^{-3} \ \frac{F}{m^2} \]
\[ \Phi_0 = 0.64 \ \text{V} \]
\[ V_D = -2.5 \ \text{V} \]

Strongly voltage dependent capacitance

- However, digital circuits tend to move fast between high and low voltages
- An equivalent (average) capacitance \( C_{eq} \) can be used
- The same amount of charges is moved as by the non-linear model

\[ C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = K_{eq} \times C_{j0} \quad \text{(derived at page 83)} \]
- \( K_{eq} \) is dependent on the grading coefficient \( m \)

Conclusion Diode

- Diodes appear in the drain and source areas (affect power and speed)
- Diodes should always be backward biased
- For digital design: the dynamic behavior is important
- A simple model for hand calculations can be used in digital design:

\[ C_{eq} = K_{eq} \times C_{j0} \]

Digital IC-Design

The MOS Transistor
The MOS-transistor: An Old Invention

- In 1925, Julius Edgar Lilienfeld described the first MOSFET structure
  - U.S. Patent in 1930
- In early 30's, a similar structure was shown by Oskar Heil
  - British Patent in 1935
- None of them built a working component
- The first working MOS-transistor was shown in early 60's

What is a MOS-transistor?

MOS = “Metal Oxide Semiconductor”

The MOS Transistor (or MOSFET)

- Most important device in digital design
- Very good as a switch
- Relatively few parasitics
- Rather low power consumption
- High integration density
- Simple manufacturing
- Economical for large complex circuits

Simple Large Signal Model

\[ I_D = \frac{k_n}{2} (V_{GS} - V_T)^2 \]

- \( I_D \) = Drain current
- \( V_{GS} \) = Gate-Source voltage
- \( V_{DS} \) = Drain-Source voltage
- \( V_T \) = Threshold voltage
- \( k_n \) = Gain factor (n-channel)
How does it Work?

A simple model:

\[ I_D = \frac{k}{2} (V_{GS} - V_T)^2 \]

Opens a channel

\( V_{GS} \) must be larger than a threshold \( V_T \)

\( V_{DS} \) drives a current \( I_D \)

What is a MOS Transistor?

ASwitch

\[
\begin{align*}
V_{GS} & \quad \text{G} \\
R_{eq} & \quad \text{D} \\
S & \quad \text{G} \\
D & \quad \text{D}
\end{align*}
\]

\( V_{GS} \) - infinite resistance when \( V_{GS} < V_T \)

\( R_{eq} \) when \( V_{GS} \geq V_T \)

\( V_T \) = Threshold voltage

MOS – a Four Terminal Device

- Gate voltage determines the current from drain to source
- Source connected to lower potential for n-channel devices (often to GND)
- Source connected to higher potential for p-channel devices (often to VDD)
- Bulk keeps the substrate at a stable potential. If not shown – it is assumed to be connected to the supply/GND.

Important Dimensions

Technology development:

1993: 0.6 um
2003: 65 nm
2013: 18 nm?

The technology is named after the gate length \( L \)

“Diode area”
MOS Circuit Symbols

N-MOS
- Enhancement
- With Bulk
- Depletion

P-MOS
- Enhancement
- With Bulk

Simple Large Signal Model
\[ I_D = \frac{k}{2} (V_{GS} - V_T)^2 \]

Two Devices are Available - CMOS
- CMOS = Complementary MOS
- Static CMOS means complementary NMOS/PMOS pairs
- Their gates are always connected pair wise

The Threshold Voltage \( V_T \)
- The substrate is slightly doped (p for NMOS)
- There are always free electrons in the substrate
- To form a channel, we need to attract these negative charges
- The threshold is when the number of negative and positive charges are equal
- The value of \( V_T \) is thus set by the p-doping concentration

\[ V_{GS} > V_T \]

n-channel

Depletion Region
The Bulk (Body) Potential

- The bulk is most often connected to GND ($V_{ss}$ for PMOS)
- Negative $V_{ss}$ opens the diode; Not Allowed
- Positive $V_{ss}$ makes it harder to attract negative charges to the channel
- That is, the threshold voltage will increase

![Diagram showing the Bulk Potential](image)

The Threshold Voltage $V_T$

$$V_T = V_{T0} + \gamma (\sqrt{-2\phi_F} + V_{SB}) - \sqrt{-2\phi_F}$$

- $\phi_F$ = Fermi potential
- $\gamma$ increases with the acceptor concentration
- Low threshold $\Rightarrow$ Low voltage transistors but they are leaky
- Two threshold voltage technologies can be used for low power

Threshold Voltage: Example 3.5

- Determine the threshold voltage for a PMOS transistor with the following data:
  - $V_{T0} = -0.4 \, V$
  - $\gamma = -0.4 \, V$
  - $V_{SB} = -2.5 \, V$
  - $\phi_F = 0.3 \, V$

  Twice the threshold voltage!

$$V_T = V_{T0} + \gamma (\sqrt{-2\phi_F} + V_{SB}) - \sqrt{-2\phi_F}$$

$$V_T = -0.4 - 0.4 (\sqrt{-0.6 - 2.5} - \sqrt{-0.6}) = -0.79 \, V$$

Threshold Voltage: Plot NMOS

- Twice the threshold for NMOS as well
How does the MOS Work? (Cont.)

- When $V_{GS}$ is slightly increased
- Negative charges are attracted
- A Depletion region is formed

$V_{GS} > 0$

When $V_{GS}$ is increased above $V_T$

- More negative than positive charges are attracted close to the gate (turns into $n$-type material)
- A channel is formed (Strong inversion)

How does it Work?

Linear Region (Resistive Operation)

- $V_{DS}$ is increased slightly
- Horizontal E-field from drain to source
- A current $I_D$ is established

$V_{GS} > V_T$

$V_{GS} < V_{GS}-V_T$

$V_{DS} < V_{GS}-V_T$

Linear Region (Resistive Operation)

- $I_D(V_{DS})$ has a resistive behavior
- $I_D$ has a linear relation to $V_{GS}$

$V_{GS} > V_T$

$V_{DS} < V_{GS}-V_T$

$I_D$
Linear Region (Resistive Operation)

- $I_D$ is proportional to the vertical E-field
  - i.e. to the # of charges attracted by the gate voltage $V_{GS}$

- $I_D$ is proportional to the horizontal E-field
  - i.e. to the charge velocity caused by the drain voltage $V_{DS}$

- $V_{GS}$ forms a vertical E-field
- $V_{DS}$ establish a horizontal E-field

Saturation Region

- $V_{DS} = V_{GS} - V_T$
- Strong inversion reached precisely (i.e. $V_{GD} = V_T$)
- No channel close to the drain

- $V_{GS} > V_T$
- $V_{DS} = V_{GS} - V_T$

- $I_D = \mu_e Q \xi W$
  - $\mu_e$ = Electron mobility
  - $\xi$ = E-field over the channel

- $Q \sim V_{GS} - V_T$
  - # of charges attracted by the gate
- $Q \sim V_{DS}$
  - Less charges close to the drain

- $\xi = \frac{V_{GS}}{L}$

- $I_D = k_n \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}$
  - $(k'_n = \mu_e C_m)$

- From charge conc.
- From Horizontal E-Field

Saturation Region

Insert $V_{DS} = V_{GS} - V_T$ in the linear equation

- $I_D = k'_n \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}$
- $I_D = k'_n \frac{W}{L} (V_{GS} - V_T - \frac{V_{GS} - V_T}{2})(V_{GS} - V_T)$
- $I_D = \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2$
The gain factor \( k_n \)

\[ I_D = \frac{k_n}{2} W \left( V_{GS} - V_T \right)^2 \]

The gain factor is

\[ k_n = k_n' \frac{W}{L} \]

Where the process transconductance parameter is

\[ k_n' = \mu_n \times C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]

Where

\( \varepsilon_m = \text{SiO}_2 \)

Permittivity

Note that the gain is dependent on the oxide thickness i.e. the oxide capacitance

**Channel Length Modulation**

\( V_{DS} \gg V_{GS} - V_T \) \( \Rightarrow \) Pinch off

The effective channel length is modulated by \( V_{DS} \)

Electrons are injected through the depletion region

\[ V_{GS} > V_T \]

\[ V_{DS} > V_{GS} - V_T \]

Saturation Region

\( \bullet \) \( I_D \) have a quadratic relation to \( V_{GS} \)

\( \sim \) \( I_D \) have a small dependence to \( V_{DS} \)

**Channel Length Modulation**

\( V_{DS} > V_{GS} - V_T \)

\[ I_D \approx \frac{W}{L - L'}; \quad \{ L' = \lambda V_{DS} L \} \]

\[ I_D \approx \frac{W}{L(1 - \lambda V_{DS})} \approx \frac{W}{L} (1 + \lambda V_{DS}); \quad \lambda V_{DS} \ll 1 \]

\[ I_D = k_n' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\( \lambda = \text{Empirical constant} \)
MOS Model for Long Channels

Widely used model for manual calculations

\[ V_{DS} \geq V_{GS} - V_T; \quad I_D = \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2 \left( 1 + \lambda V_{DS} \right) \]

\[ V_{DS} < V_{GS} - V_T; \quad I_D = \frac{k'_n}{L} (V_{GS} - V_T)^2 \left( \frac{V_{GS}^2}{2} \right) \left( 1 + \lambda V_{DS} \right) \]

\[ k'_n = \mu C \]

\[ V_T = V_{T0} + \gamma (\sqrt{2\Phi_F + V_m} - \sqrt{2\Phi_F}) \]

Often added to avoid discontinuity

\[ \lambda = 0.1 \]

MOS-Model

Discontinuity (no channel length modulation in linear region)

With channel length modulation

Without channel length modulation

\[ \lambda = 0.1 \]
Conclusions - Static Behavior

**Long channel device**

**Linear Region**

\[ I_D = k'_n \frac{W}{L} ((V_{GS} - V_T) - \frac{V_{DS}^2}{2}) \]  

\[ V_{DS} < V_{GS} - V_T \]

**Saturated Region**

\[ I_D = \frac{k'_n W}{2} \left( V_{GS} - V_T \right)^2 (1 + \lambda V_{DS}) \]  

\[ V_{DS} > V_{GS} - V_T \]

**Threshold Voltage**

\[ V_T = V_{T0} + \gamma (\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \]

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**Velocity & Mobility**

- The electron (hole) velocity is related to the mobility \( \mu \).
- The velocity is also dependent on the E-field \( \xi \).

\[ \nu_n = \mu_n \xi \frac{m}{s} \]

\[ \nu_p = \mu_p \xi \frac{m}{s} \]

**Typical values**

- \( \mu_n = 0.038 \frac{m^2}{Vs} \) = Electron mobility
- \( \mu_p = 0.013 \frac{m^2}{Vs} \) = Hole mobility

- The mobility is dependent on doping concentration ...
- Often determined empirically
- Note that the electron mobility is about 3 times higher

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**Velocity Saturation (\( \nu_{sat} \))**

- \( V_{DS} \) forms a horizontal E-field \( \xi \).
- An increased E-field leads to higher electron velocity.
- However at a critical E-field \( \xi \), the velocity saturates due to collisions with other atoms.

\[ \nu_{sat} \approx 10^5 \frac{m}{s} \] for both electrons and holes

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**Velocity & Mobility**

**Threshold Voltage**
Velocity Saturation \( (\nu_{\text{sat}}) \)

- Electrons typically saturates around 1-5 V/\( \mu \)m
- Example, Determine the maximum non-saturated \( V_{DS} \) for a 0.25 \( \mu \)m technology if:

\[
\xi_c = 2.5 \times 10^6 \frac{V}{m} \\
\xi_c = \frac{V_{DSAT}}{L} \\
V_{DSAT} = L \times \xi_c = 0.25 \times 10^{-6} \times 2.5 \times 10^6 = 0.63 \ V
\]

Velocity Saturation \( (\nu_{\text{sat}}) \)

The velocity is

\[
\nu = \mu_n \xi
\]

For saturated devices we modify the expression

\[
\nu = \frac{\mu_n \xi}{1 + \frac{\xi}{\xi_c}} \text{ for } \xi \leq \xi_c \\
\nu = \nu_{\text{sat}} \text{ for } \xi \geq \xi_c
\]

Velocity Saturation \( (\nu_{\text{sat}}) \)

\[
V_n = \mu_n \xi_{DS}
\]

Resistive Operation

We know the gain factor as

\[
k_a = \mu_n \times C_{ox} \times \frac{W}{L}
\]

A factor \( K \) must be added

\[
\kappa = \frac{1}{1 + \frac{\xi}{\xi_c}} = \frac{1}{1 + \frac{V_{DS}}{L \times \xi_c}}
\]

The E-field \( \xi = \frac{V_{DS}}{L} \)
Resistive Operation

The equation for the linear region is modified to

\[ I_D = \frac{\mu_C}{1 + \frac{V_{DS}}{L \times \xi_c}} \cdot W \cdot \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

Small \( V_{DS} \) and Large \( L \) give \( \kappa \approx 1 \)

A function of \( V_{DS} \)

\[ I_D = k_a \times ((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}) \times \kappa(V_{DS}) \]

\( V_{DS SAT} = 0.63 \text{ V} \)

\( \text{Velocity saturation neglected} \)

\( \text{Short-channel device} \)
The Short channel Model

The equation is complex

\[ I_D = \frac{\mu_n \times C_{ox} \times W}{1 + \frac{V_{DS}}{L \times \xi}} \times (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \]

A model for first order manual analysis is needed

Model for Manual Analysis

A first order model of the velocity is

\[
\begin{align*}
\nu &= \mu_n \xi & \text{for } \xi < \xi_c \\
\nu &= \nu_{sat} = \mu_n \xi_c & \text{for } \xi \geq \xi_c
\end{align*}
\]

Compare to previous model

Model for Manual Analysis

A first order model for the velocity saturated region:

\[ I_{DSAT} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \]

\[ V_{DS} = \xi \times L \]
A Unified Model for Manual Analysis

\[ I_D = k_n \frac{W}{L} \left( (V_{GS} - V_T) V_{\min} - \frac{V_{\min}^2}{2} \right) (1 + \lambda V_{DS}) \]

\[ V_{\min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT}) \]

Alternative Velocity Saturation

\[ k_n = \mu_n \times C_{ox}; \quad \mu_n = \frac{V_{SAT}}{\xi}; \quad \xi = \frac{V_{DSAT}}{L} \]

\[ I_D = k_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) (1 + \lambda V_{DS}) \]

\[ I_D = \mu_n \times C_{ox} \times \frac{W}{L} \left( (V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) (1 + \lambda V_{DS}) \]

\[ I_D = \frac{V_{SAT}}{V_{DSAT}} \times C_{ox} \times \frac{W}{L} \left( (V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) (1 + \lambda V_{DS}) \]

\[ I_D = \nu_{sat} \times C_{ox} \times W \left( (V_{GS} - V_T) - \frac{V_{DSAT}^2}{2} \right) (1 + \lambda V_{DS}) \]

Example – Unified Model

\[ V_T = 0.43 V; \quad V_{GS} = 1.5 V; \quad V_{DS} = 1.5 V; \quad V_{DSAT} = 0.63 V; \]

\[ \lambda = 0.06 \times \frac{W}{L_{min}} = 115 \times 10^{-9} \times \frac{0.375}{0.25} = 172.5 \mu A / V^2 \]

Find \( V_{\min} \)

\[ V_{\min} = \min \left( V_{GS} - V_T, V_{DS}, V_{DSAT} \right) \]

\[ V_{\min} = \min(1.5 - 0.43, 1.5, 0.63) \]

\[ I_D = k_n \frac{W}{L} \left( (V_{GS} - V_T) V_{\min} - \frac{V_{\min}^2}{2} \right) (1 + \lambda V_{DS}) \]

\[ I_D = 172.5 \times 10^{-6} \left( 1.5 - 0.43 \right) - \frac{0.63^2}{2} \left( 1 + 0.06 \times 1.5 \right) = 89.4 \mu A \]
Simple Model

Model for manual calculations

Simulated

Three Regions

$V_{DSAT}$

$0.63 \text{ V}$

$V_{GS} = 2 \text{ V}$

$V_{GS} = 1.5 \text{ V}$

$1.06 \text{ V}$

$V_{GS} = 1 \text{ V}$

$L_{1}$ (mA)

Velocity saturated

Saturated

$V_{DS} (\text{V})$

Transistor Model for Manual Analysis

Table on Back Cover

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

<table>
<thead>
<tr>
<th></th>
<th>$V_{TH} (\text{V})$</th>
<th>$\gamma (\text{V}^{-1})$</th>
<th>$V_{MIN} (\text{V})$</th>
<th>$\kappa (\text{A/V}^2)$</th>
<th>$\lambda (\text{V}^{-1})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-50 \times 10^{-5}$</td>
<td>-0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-50 \times 10^{-5}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

$W_{min} = 0.375 \text{ μm}$

$L_{min} = 0.25 \text{ μm}$

A PMOS Transistor

Velocity saturation is less pronounced for PMOS due to lower mobility

Assume all variables negative!

Transistor Model for Manual Analysis

Table on Back Cover
The Transistor as a Switch

\[ R_{eq} = \frac{1}{2} \left( \frac{V_{DS}}{I_{DSsat}} + \frac{V_{DS}/2}{I_{DSsat} + \frac{1}{2} \lambda V_{DS}} \right) = \frac{3 V_{DD}^2}{4 I_{DSsat}} \left( 1 - \frac{5}{6} \lambda V_{DS} \right) \]

NMOS (kΩ)

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

$R_{eq}$ resistance for a square transistor ($W/L = 1$) in 0.25 um

(Table on Back Cover)
Second Order Effects

Sub-Threshold Region

The sub threshold drain current have an exponential relation to the gate voltage (compare to bipolar).

The Trend is to reduce $V_T$

Exponential increase of the static power!

$I_{off} = I_0 \times e^{\frac{V_{GS} - V_T}{m \times V_T}}$

The Drain/Source Depletion "helps the channel" to strong inversion.

The threshold voltage tends to be lower.
The depletion region increases around the drain when the \( V_{DS} \) increases. The effect cannot be neglected in a short channel device; \( V_T \) tends to be lower.

Long devices have lower leakage.

Latch Up avoided by Substrate and Well Contacts. Today’s Technologies are better protected against latch up.
MOS Dynamic Behavior

Two Types of Capacitance

- Junction Capacitance
  - Diode areas
  - Divided in two parts - area and side wall

- Gate Capacitance
  - Gate to Bulk
  - Gate to Source/Drain

MOS Capacitances

Junction Capacitance

Drain/Source Diffusion

\[ C_{\text{Diff}} = C_{\text{Bot}} + C_{\text{SW}} \]

- \( C_{\text{Bot}} = C_j \times \text{Area} \)
  - \( C_j \) in \( \text{F/\mu m}^2 \)
- \( C_{\text{SW}} = C_{\text{jsw}} \times \text{Perimeter} \)
  - \( C_{\text{jsw}} \) in \( \text{F/\mu m} \)

Don’t count the wall towards the channel into the perimeter
Junction Capacitance

\[ C_{\text{bottom}} = C_j \times \text{Area} = \frac{1}{(1 - \frac{V_{\text{BD}}/V_{\text{BS}}}{\phi_0})^2} C_{j0} \times \text{Area} \]

\[ C_{\text{sw}} = C_{\text{jsw}} \times \text{Perimeter} = \frac{1}{(1 - \frac{V_{\text{BD}}/V_{\text{BS}}}{\phi_0})^3} C_{\text{jsw0}} \times \text{Perimeter} \]

\[ \forall \quad C_j/C_{\text{jsw}} \text{ is dependent on the bulk voltage} \]

\[ \forall \quad C_{j0} \text{ and } \phi_0 \text{ are process parameters} \]

Gate Capacitance

\[ C_G = C_{\text{ox}} \times W \times L_{\text{eff}} \]

\[ C_G \text{ depends on the region} \]

\[ C_{\text{ox}} \text{ in F/\mu m}^2 \]
Channel Capacitance

<table>
<thead>
<tr>
<th>Table 3-4</th>
<th>To Bulk</th>
<th>To Source</th>
<th>To Drain</th>
<th>Total Gate Cap.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$C_{GCB}$</td>
<td>$C_{GCS}$</td>
<td>$C_{GCD}$</td>
<td>$C_G$</td>
</tr>
<tr>
<td>Cutoff</td>
<td>$C_{ox}WL$</td>
<td>0</td>
<td>0</td>
<td>$C_{ox}WL + 2C_{ox}W$</td>
</tr>
<tr>
<td>Resistive</td>
<td>0</td>
<td>$(1/2)C_{ox}WL$</td>
<td>$(1/2)C_{ox}WL$</td>
<td>$C_{ox}WL + 2C_{ox}W$</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>$(2/3)C_{ox}WL$</td>
<td>0</td>
<td>$(2/3)C_{ox}WL + 2C_{ox}W$</td>
</tr>
</tbody>
</table>

Cut off: No channel ⇒ $C_{GC} = C_{GCB}$

Resistive: Channel ⇒ Divide $C_{GC}$ in two parts

Saturation: $\approx \frac{2}{3}$ of Channel to Source

Overlapp Capacitance

$C_{GD} = C_{ox} \times W \times X_d$

$C_{GS} = C_{ox} \times W \times X_d$

$C_{ox}$ in F/μm²

Or

$C_{GD} = C_{o} \times W$

$C_{GS} = C_{o} \times W$

$C_{o}$ in F/μm

$C_{o}$ or $X_d$ are overlap process parameters

MOS Capacitance Example

Gate Capacitance - 0.35 micron process

$C_{ox} = 4.6$ fF/μm²

$W = 0.6$ μm; $L_{eff} = 0.3$ μm;

$C_G = C_{ox}WL_{eff} = 4.6 \times 0.6 \times 0.3 \times 10^{-12} =

C_G = 0.83$ fF

Junction Capacitance

$C_j = \frac{C_{ox}}{(1-V_D/\Phi_0)^m}$

$m = \frac{1}{2}$ for abrupt and $m = \frac{1}{3}$ for graded junction
Linearized Junction Capacitance

Replace non-linear capacitance by a large-signal equivalent linear capacitance which distribute equal charge over the voltage swing of interest

\[
C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}
\]

\[
K_{eq} = \frac{-\phi_0^m [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]}{(V_{high} - V_{low})(1-m)}
\]

See page 83

MOS Capacitance Example (0.35)

Drain (Junction) capacitance

\[
C_{j0} = 0.93 \text{ fF/ \mu m}^2; C_{jsw0} = 0.28 \text{ fF/\mu m};
\]

Drain area = \( W \times L_s = 0.6 \times 0.7 \text{ fF/\mu m}^2; \ K_{eq} = 1\)

\[
C_{bottom} = 0.7 \times 0.6 \times 0.93 = 0.39 \text{ fF}
\]

\[
C_{sw} = (2 \times 0.7 + 0.6) \times 0.28 = 0.56 \text{ fF}
\]

\[
C_{diffusion} = 0.39 + 0.56 = 0.95 \text{ fF}
\]

MOS Capacitance Example

\[
C_G = 0.83 \text{ fF}
\]

\[
C_{bottom} = 0.39 \text{ fF}
\]

\[
C_{sw} = 0.56 \text{ fF}
\]

\[
C_{diffusion} = 0.39 + 0.56 = 0.95 \text{ fF}
\]

Compare!

The drain capacitance is comparable to the gate capacitance in sub micron

MOS Decoupling Capacitor

\[ V_{DD} \]
**Filer Cells in a Typical 0.13 um Tech.**

- Leaf Cell
- Decoupling C capacitance when there is space left

**Parasitic Resistances**

- Resistance in diffusion and contact

**MOS Models**

- **SPICE Level 1 (Shichman-Hodges)**
  - Long channels and manual calculations

- **SPICE Level 2**
  - Physical model. Not accurate for sub micron tech.

- **SPICE Level 3**
  - "Empirical" model based on "curve matching"

- **BSIM (Berkeley Short-channel IGFET Model)**
  - Accurate for short channel devices

**Typical Values (0.35μm)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Discrete (BF 170)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k'$</td>
<td>175 uA/V$^2$</td>
<td>-60 uA/V$^2$</td>
<td>50 mA/V$^2$</td>
</tr>
<tr>
<td>$V_T$</td>
<td>0.50 V</td>
<td>-0.60 V</td>
<td>2 V</td>
</tr>
<tr>
<td>$L_{eff}$</td>
<td>0.30 um</td>
<td>0.38 um</td>
<td></td>
</tr>
<tr>
<td>$W_{eff}$</td>
<td>0.55 um</td>
<td>0.55 um</td>
<td></td>
</tr>
<tr>
<td>$y$</td>
<td>0.58 V/√2</td>
<td>-0.45 V/√2</td>
<td></td>
</tr>
<tr>
<td>$\lambda$</td>
<td>0.05</td>
<td>-0.15</td>
<td></td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>7.5 nm</td>
<td>7.5 nm</td>
<td></td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>4.6 fF/um$^2$</td>
<td>4.6 fF/um$^2$</td>
<td></td>
</tr>
<tr>
<td>$C_{j0}$</td>
<td>0.93 fF/um$^2$</td>
<td>1.42 fF/um$^2$</td>
<td></td>
</tr>
<tr>
<td>$C_{jsw0}$</td>
<td>0.28 fF/um</td>
<td>0.38 fF/um</td>
<td></td>
</tr>
</tbody>
</table>
Conclusions - Static Behavior

\[ I_D = \frac{k_n}{L} W (V_{GS} - V_T) V_{DS}^2 \left( 1 + \lambda V_{DS} \right) \] Resistive

\[ I_D = \frac{k_n}{2} W \left( V_{GS} - V_T \right)^2 (1 + \lambda V_{DS}) \] Saturated

\[ I_D = \frac{k_n}{L} W (V_{GS} - V_T) V_{DSAT}^2 \left( 1 + \lambda V_{DS} \right) \] Velocity saturated

\[ V_T = V_{T0} + \gamma \left( \sqrt{2\phi_F} + V_{SB} \right) - \sqrt{2\phi_F} \] Threshold Voltage

Conclusions - Dynamic Behavior

\[ C_G = C_{ox} \times W \times L_{eff} \] Gate Capacitance

\[ C_{GD} = C_{GS} = W \times C_{ox} \times X_d \] Gate to Drain Capacitance

\[ C_{diff} = C_{bottom} + C_{SW} \] Junction Capacitance

\[ C_{bottom} = C_j \times Area \] Junction Capacitance

\[ C_{SW} = C_{jSW} \times Perimeter \] Junction Capacitance

A Unified Model for Manual Analysis

\[ I_D = \frac{k_n}{L} W \left( V_{GS} - V_T \right) V_{min} - \frac{V_{min}^2}{2} \left( 1 + \lambda V_{DS} \right) \]

\[ V_{min} = \min(V_{GS} - V_T, \ V_{DS}, \ V_{DSAT}) \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{2\phi_F} + V_{SB} \right) - \sqrt{2\phi_F} \]

Digital IC Design

Small Signal Model
(Extra)
**Small Signal Model**

\[ g_m V_{gs} - g_o V_{ds} \]

- Linear Region
- Saturation Region

**Small Signal Model (Linear)**

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} = k' \frac{W}{L} \frac{(V_{GS} - V_T - V_{DS})^2}{2} \]

**Small Signal Model (Saturation)**

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{k' W}{L} (V_{GS} - V_T) \]

\[ g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{k' W}{L} (V_{GS} - V_T)^2 \]

\[ V_{gs} \quad g_m V_{gs} \quad g_o \quad V_{ds} \]