Electrical Parameters

Transistor					
	N-type		P-type		Unit
Gain factor (datasheet)	KP_n	175	KP_p	58	μA/V^2
Gain factor (simulated)	KP_n	115	KP_p	40	μA/V^2
Threshold voltage (W/L=10/10)	V_{tn0}	0.46	V_{tp0}	-0.60	V
Threshold voltage (W/L=10/0.35)	V_{tn0}	0.48	V_{tp0}	-0.60	V
Effective channel length (0.35 μm)	$L_{eff,0.35,n}$	0.40	$L_{eff,0.35,p}$	0.53	μm
Effective channel width (0.6 μm)	$W_{eff,0.6,n}$	0.50	$W_{eff,0.6,p}$	0.50	μm
Body effect factor (W/L=10/10)	γ_n	0.58	γ_p	-0.45	$\sqrt{V}$
Bulk potential (2·ϕ_f)	ϕ_{bn}	0.79	ϕ_{bp}	-0.77	V
Resistance, active region (sim.)	r_{ds_n}	55	r_{ds_p}	55	ΩA/μm
Saturation current (0.35 μm)	I_{sat_n}	540	I_{sat_p}	-240	μA/μm
D-S breakdown volt. (0.35 μm)	V_{brn}	> 8	V_{brp}	> -8	V

Capacitances (layer to substrate)				
	Area fF/μm^2		Perimeter fF/μm	
gate capacitance	C_{ox}	4.60		
gate-diff overlap			C_{gd0}	0.21
gate-bulk overlap			C_{gb0}	0.11
n$^+$ diffusion (0 V)	C_{jn}	0.93	C_{jnp}	0.28
p$^+$ diffusion (0 V)	C_{jp}	1.42	C_{jpp}	0.38
$N_{well} - bulk(0V)$	C_{jw}	0.11	C_{jwp}	0.53
poly1	C_{p1}	0.119	C_{pp}	0.052
metal1	C_{m1}	0.032	C_{m1p}	0.046
metal2	C_{m2}	0.012	C_{m2p}	0.036
metal3	C_{m3}	0.008	C_{m3p}	0.037
metal4	C_{m4}	0.006	C_{m4p}	0.033
poly1-poly2	C_{poly_s}	0.86	C_{poly_p}	0.082

Sheet resistance		
Layer		$\Omega/\square$
metal4	R_{sm4}	0.05
metal3	R_{sm3}	0.05
metal2	R_{sm2}	0.08
metal1	R_{sm1}	0.08
poly1	R_{sp}	6
poly2	R_{sp2}	50
n^+ diff.	R_{sdn}	80
p^+ diff.	R_{sdp}	150
n-well	R_{nw}	1000

Max. current density		
Layer	mA/μm	
metal4	J_{m4}	1.6
metal3	J_{m3}	1.0
metal2	J_{m2}	1.0
metal1	J_{m1}	1.0
poly1	J_p	0.5
poly2	J_{p2}	0.3

Max. contact current		
0.4 μm×0.4 μm contact		
0.5 μm×0.5 μm via, via2, via3		
Layer-layer		mA
metal4-metal3	I_{via3}	0.96
metal3-metal2	I_{via2}	0.60
metal2-metal1	I_{via}	0.60
metal1-poly1/diff	I_{cp}	0.94

Contact resistance		
Layer-layer	Ω/cnt	
metal4-metal3	R_{via3}	3
metal3-metal2	R_{via2}	1.5
metal2-metal1	R_{via}	1.5
metal1-poly1	R_{cp}	5
metal1-n$^+$ diff.	R_{cdn}	40
metal1-p$^+$ diff.	R_{cdp}	90

Diode data		N	P
Area junc. pot.	V_j	0.69 V	1.02 V
Sidewall junc. pot.	V_{sw}	0.69 V	1.02 V
Area grading coeff.	m_j	0.31	0.55
Sidewall grading coeff.	m_{sw}	0.19	0.39

Structural and geometrical parameters		
Gate oxide thickness	t_{ox}	7.5 nm
Poly1-poly2 oxide thickness	t_{pox}	41 nm
Field oxide thickness	t_{fox}	290 nm
Poly1-metal1 oxide thickness	t_{pox}	645 nm
Metal1-metal2 oxide thickness	t_{mox}	1.00 μm
Metal2-metal3 oxide thickness	t_{mox2}	1.00 μm
Metal3-metal4 oxide thickness	t_{mox3}	1.00 μm
Passivation thickness	t_{prot}	900 nm
Poly1 thickness	t_p	282 nm
Metal1 thickness	t_{m1}	665 nm
Metal2 thickness	t_{m2}	640 nm
Metal3 thickness	t_{m3}	925 nm
Metal4 thickness	t_{m4}	925 nm
n$^+$ and p$^+$ junction depth	x_j	200 nm
n-well junction depth	x_w	2.0 μm

Latch-up prevention

1. All wells must have at least one contact connected to V_{dd}.
2. Place well and substrate contacts wherever possible.
3. Max. spacing between well/substrate contacts: 50 μm.

Note: The design rules and electrical parameters presented in this document are representative for a 0.35 μm CMOS process, and they are intended for teaching purpose only.
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