Lund University
Dept. of Electroscience

ETI063

Exam
Analog IC-design

2007-10-20, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

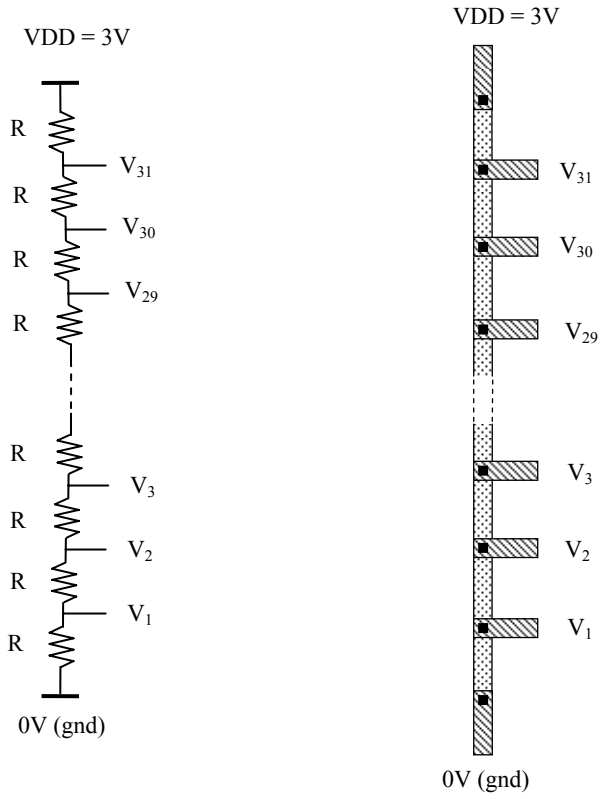
Allowed during exam:

- Textbook: Gray, Hurst, Lewis, Meyer,
  "Analysis and Design of Analog Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1

A resistor ladder is to be designed in the 0.35um CMOS process (use the parameters in the data-sheet). The purpose of the resistive ladder is to generate 31 different reference voltages to be used in an analog to digital converter. The schematic and a sketch of the layout of the ladder are shown in the figure below:



a. Calculate the total length of the resistor ladder required in the layout not to exceed the maximum current density of the resistor material. Perform the calculation for two different alternatives: resistors made in poly1 and in poly2. (3p)

b. If the resistors are 1um wide, and the length calculated in a. is used, what is the DC current consumption of the ladder? Perform the calculation for both the poly1 and the poly2 alternative. (2p)

c. Which resistor layer is best to use in this case, poly1 or poly2? Motivate! (1p)

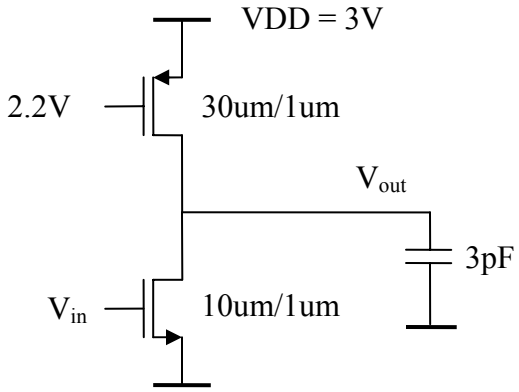
Problem 2

An amplifier according to the figure below is realized in the 0.35um process. In the calculations, use long channel equations and neglect all capacitances except the load.

a. Find the input bias voltage at which the both the transistors are in the active region. (hint: set the drain currents equal) (1p)

b. Draw a small signal schematic of the amplifier. (2p)

c. Calculate the DC voltage gain, the -3dB bandwidth (location of the pole), and the unity voltage gain frequency. (3p)



Problem 3

To increase the voltage gain of the amplifier in problem 2, cascodes are introduced. In the calculations, use long channel equations and neglect the Body effect.

a. Draw the schematic. Choose appropriate gate bias voltages of the cascode devices. The cascode devices should have the same size as the main devices of the same type. The gate bias voltages and sizes of the main devices are kept the same as in problem 2. (3p)

b. Calculate the DC voltage gain (2p)

c. Calculate the output voltage range when all devices remain in saturation (1p)

Problem 4

A transistor with W=10um and L=1um has been realized in the 0.35um process. For the three different bias points indicated below, find the small signal transconductance, gm, and the small signal drain source conductance, gds. Use long channel equations and take the Body effect into account where it has effect.

Bias points:

a. V_G=1V, V_S=0V, V_D=2V, V_B=0V (2p)

b. V_G=2V, V_S=1V, V_D=3V, V_B=0V (2p)

c. V_G=2V, V_S=0V, V_D=0V, V_B=0V (2p)

Problem 5

A two stage operational amplifier is designed in the 0.35um process, according to figure 9.28a in the textbook. All transistors are 1um long. The following parameters are given:

VDD = 3V

M1, M2: W=20um

M3, M4: W=10um

M5: W=40um, V_{G5}=2.2V

M6: W=50um

M7: W=200um, V_{G7}=2.2V

M8: this transistor is omitted

C=1pF, R_Z=2kΩ

C_L=2pF

Assume that all capacitances except C_L can be ignored. Use long channel equations to calculate

a. The DC bias current, the unity voltage gain frequency, the DC voltage gain, and the slew-rate. (3p)
b. The phase margin with C_L=2pF, and how much can the load capacitance can be increased before the phase margin drops to 60 degrees? (3p)