Lund University
Dept. of Electroscience

ETI063

Exam
Analog IC-design

2006-10-21, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

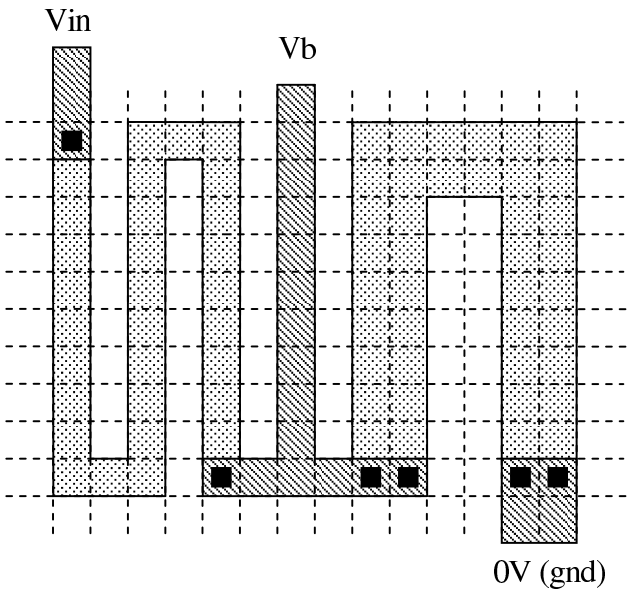
Allowed during exam:

- Textbook: Gray, Hurst, Lewis, Meyer,
  "Analysis and Design of Analog Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1

The layout below is drawn in the 0.35um CMOS process. The grid line spacing is 1um. Two poly1 resistors are realized.



The terminal Vb is unloaded, that is no current flows in or out of the Vb terminal.

a. Calculate the voltage division from Vin to Vb. Include contact resistances. Corners correspond to 0.55 squares. (4p)

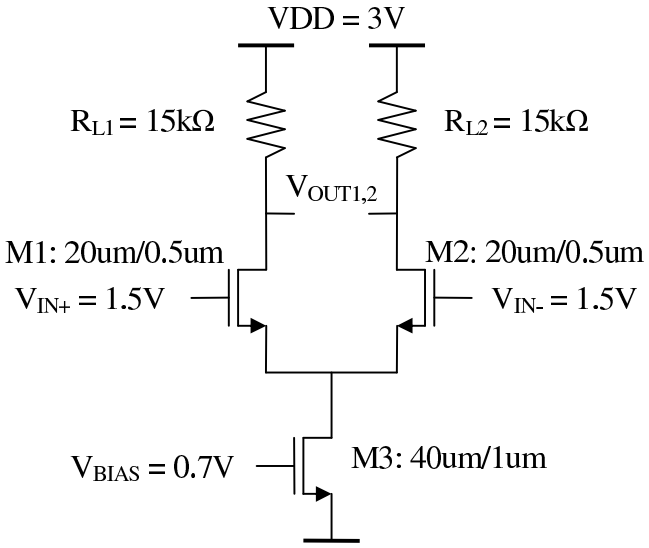
b. Calculate the maximum voltage Vin not to exceed the maximum current density or the maximum contact current anywhere (neglect current crowding in corners). (2p)

Problem 2

A differential amplifier according to the figure below is realized in the 0.35um process. Neglect body-effect and use long channel equations to:

a. Calculate the bias currents and output voltages, and verify that all transistors operate in strong inversion and saturation. (3p)

b. For low frequencies (DC), calculate the differential-mode voltage gain, common-mode voltage gain, and the common-mode rejection ratio. (3p)



Problem 3

An NMOS transistor is realized in the 0.35um process. The length is 0.6um and its total width is 20um. It is realized using a finger layout with two gate fingers. The drain is located between the two gate fingers, which have a separation of 1.2um. The source regions have a diffusion length of 1.0um from the gate fingers.

The transistor is biased at V_S=1V, V_G=2V, and V_D=3V (and V_B=0V). For this bias-point, take body-effect into account and use long-channel equations to calculate:

a. The drain current (1p)

b. g_m, g_{mb}, and g_{ds} (1p)

c. Cgs, Cgd, Cdb, and Csb (3p)

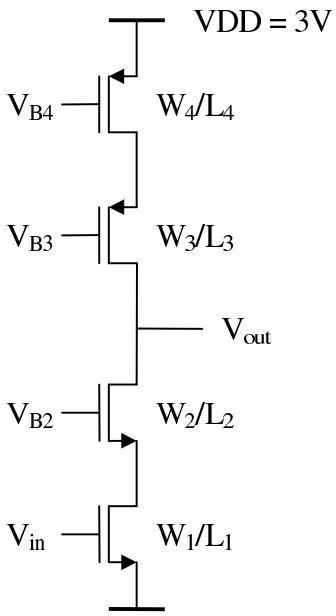
d. f_T (1p)

Problem 4

An amplifier according to the figure below is to be designed in the 0.35um process. Choose V_{IN} (the input bias voltage), V_{B2}, V_{B3}, V_{B4} & W_1, W_2, W_3, W_4 & L_1, L_2, L_3, L_4 so that the following specification is fulfilled with a capacitive load of 1pF:

- $I_{DC} < 10uA$
- Unity voltage gain frequency = 10MHz (assuming single pole response)
- DC voltage gain > 100 000 when $1V < V_{out} < 2V$
- Second pole > 400MHz

Use long-channel equations. The second pole is due to the capacitance at the drain of M1/source of M2. Shared junction is recommended, but not necessary.



Problem 5

An input stage for a two stage amplifier has been designed in the 0.35um process. The input stage consists of M1 to M5 in figure 6.16 in the textbook.

The transistor dimensions and bias voltages:

- L = 1um for all transistors
- W1,2 = 40um
- W3,4 = 5um
- W5 = 40um
- VDD = 3V
- VG5 = 2.1 V

Calculate using long-channel equations neglecting body-effect:

- CM input voltage range (1p)
- SR limitation of input stage if Cc of output stage is 4pF (1p)
- Input referred thermal noise, total rms noise voltage in band 1MHz to 2MHz (2p)
- Offset voltage standard deviation (2p)

For the offset voltage calculation:

- $\sigma(V_{tn,p}) = \frac{10\text{mV}}{\sqrt{WL}}$, W & L in um
- $\sigma\left(\frac{W}{L}\right) = \frac{2\%}{\sqrt{WL}}$, W & L in um

Boltzmann's constant (needed in noise calculation):

$k = 1.38 \cdot 10^{-23}$ J / K