Lund University
Dept. of Electroscience

ETI063

Exam
Analog IC-design

2006-01-09, 08.00-13.00

The exam consists of 5 problems which can give a maximum of 6 points each. The total maximum is thus 30 points, and to pass the exam at least 15 points is needed. To pass the course the laboratory part must also be completed.

Remember:

- Always start a **new problem on a new page**
- Write **name and page number on each page**
- Sort the pages according to number before you hand them in
- All assumptions must be motivated
- Finish your solution with an answer if possible
- The problems are not sorted according to difficulty
- The number of points of a problem does not always reflect its difficulty

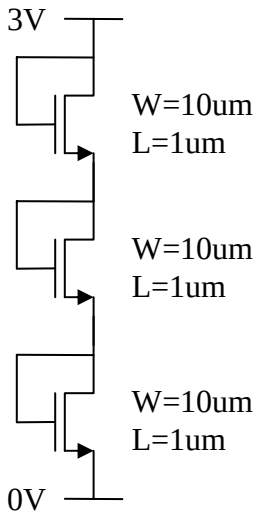
Allowed during exam:

- Textbook: Gray, Hurst, Lewis, Meyer,
  "Analysis and Design of Analog Integrated Circuits"
- Table of basic physical constants and equations (TEFYMA equivalent)
- Data sheet of process
- Pocket calculator

Good luck!

Problem 1

The circuit below is realized in the 0.35um CMOS process.



a. Calculate the DC current and voltages in the circuit. Use long channel equations and neglect the body effect. (4p)

b. If the body effect is taken into account, would the DC current increase or decrease. What about the DC voltages? (2p)

Problem 2

A two-stage amplifier according to figure 9.28a in the textbook is realized in the 0.35um CMOS process. The supply voltage is 3V. All transistors have the length 1um. M1, M2, M5, M6, and M8 have a width of 40um. M3 and M4 are 8um wide, and M7 is 100um. C is 2pF, and R_z is 900Ω. I_{BIAS} is 50uA, and the input DC voltages both are 1.5V.

Use long channel equations and neglect the body effect.

a. Calculate all bias currents and voltages. The output is assumed to be at 1.5V. (3p)

b. Calculate the unity gain bandwidth. (1p)

c. Calculate the phase margin with a 5pF load. Assume a total parasitic capacitance of 0.2pF at the output node, and 0.4pF at the input node of the second stage. (2p)

Problem 3

The 2pF capacitor of the previous problem should be realized in the 0.35um process.

a. Calculate the dimensions of a poly1-poly2 capacitor. Also calculate the bottom plate parasitic capacitance and the ratio of undesired to desired capacitance. Include fringing. (2p)

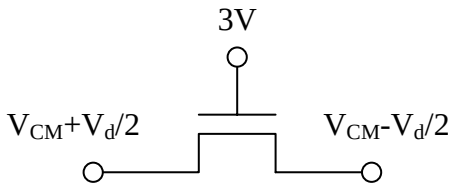
b. If poly2 is not available, a stack of metal2-metal3-metal4 can be used to form a plate capacitor structure. Calculate the dimensions. Also calculate the parasitic capacitance and the ratio of parasitic to desired capacitance. Include fringing of the bottom plate capacitance only. Hint: Use the thickness data to calculate layer to layer capacitances. (2p)

c. Repeat b. but with a stack consisting of poly1-metal1-metal2-metal3-metal4. (1p)

d. Conclusions. (1p)

Problem 4

To save chip area a transistor operating in the triode region is used to realize a 1MΩ resistance in the 0.35um process, see figure below.



Use long channel equations and neglect the body effect, and assume the common mode voltage (V_{CM}) to be equal to 1V.

a. Calculate suitable dimensions so that the resistance equals 1MΩ when the common mode voltage is 1V. To get the best matching accuracy the dimensions should be as large as possible. At the same time, however, the gate-channel capacitance must be less than 2pF. (2p)

b. Show that the resistance is independent of V_d (linear resistor) when the transistor operates in the triode region. (2p)

c. Neglecting process variations, and considering variations in the common mode voltage only, how much variation in that voltage is allowed if the resistance may change by no more than ±20% ? (2p)

Problem 5

Design a current mirror in the 0.35um CMOS process using any topology of your choice that meets the following requirements:

- $V_{out,min}$ = 200mV
- I_{out} = 100uA
- I_{in} = 100uA
- r_{out} > 1MΩ
- c_{out} < 0.1pF
- The total (from all transistors) output noise current integrated from 10kHz to 100kHz must be less than 2nA (rms). The noise spectral density can be assumed flat in this range (no 1/f noise, and no influence of high frequency poles)

Verify that all requirements are met using long channel equations.

Useful data:

- The distance between two gates in a transistor with finger layout is 1.2um.
- Boltzmann's constant: $k=1.38*10^{-23}$ J/K