Technology parameters

Note: The design rules and electrical parameters presented in this document are representative for a 130nm CMOS process, and are intended for teaching purpose only.

	—Transistor—				
	N -type		P -type		Unit
Gain factor	k'_n	400	k'_p	100	μA/V^2
Threshold volt. (W/L=10/0.5)	V_{t0n}	0.3	V_{t0p}	-0.3	V
Side diffusion S/D (0.13 μm)	$L_{d,n}$	0.005	$L_{d,p}$	0.005	μm
Depletion layer width, active region (0.13 μm)	$X_{d,n}$	0.005	$X_{d,p}$	0.005	μm
Body effect factor (W/L=10/1)	γ_n	0.58	γ_p	-0.45	$\sqrt{V}$
Surface potential ($\phi_0 \approx 2 \cdot \phi_f$)	$2\phi_{fn}$	0.7	$2\phi_{fp}$	-0.7	V
Channel length modulation	$\lvert\frac{dX_{d,n}}{dV_{DS}}\rvert$	0.08	$\lvert\frac{dX_{d,p}}{dV_{DS}}\rvert$	0.04	μm/V
D-S breakdown volt. (0.13 μm)	V_{BVn}	> 3	V_{BVp}	< -3	V

—Capacitances (layer to substrate)—

	Area fF/μm^2		Perimeter fF/μm	
gate oxide capacitance	C_{ox}	14		
gate-diff (S/D) overlap			C_{ol}/W	0.07
gate-bulk cap.			C_{gb0}	0.11
n$^+$ diffusion (0 V)	C_{j0n}	1.0	C_{jswn}	0.05
p$^+$ diffusion (0 V)	C_{j0p}	1.1	C_{jswp}	0.06
N$_{well}$-bulk (0 V)	C_{jw}	0.11	C_{jwp}	0.53
poly	C_p	0.105		
metal1	C_{m1}	0.043		
metal2	C_{m2}	0.025		
metal3	C_{m3}	0.017		
metal4	C_{m4}	0.012		
metal5	C_{m5}	0.010		
metal6	C_{m6}	0.008		
metal7	C_{m7}	0.007		
metal8	C_{m8}	0.006		

—Sheet resistance—

Layer	$\Omega/\Box$	
poly	R_{sp}	7.5
metal1-6	R_{sm1-6}	0.065
metal7	R_{sm7}	0.03
metal8	R_{sm8}	0.03
n$^+$ diff.	R_{sdn}	8
p$^+$ diff.	R_{sdp}	8
n-well	R_{snw}	400

—Max. current density—

Layer	mA/μm	
poly1	J_p	0.5
metal1-6	J_{m1-6}	2.4
metal7	J_{m7}	7.2
metal8	J_{m8}	7.2

—Contact resistance—

Layer-layer	Ω/cnt	
metal1-n$^+$ diff.	R_{cdn}	12
metal1-p$^+$ diff.	R_{cdp}	12
metal1-poly	R_{cp}	8
metal2-metal1, via1	R_{via1}	1.2
metal3-metal2, via2	R_{via2}	1.2
metal4-metal3, via3	R_{via3}	1.2
metal5-metal4, via4	R_{via4}	1.2
metal6-metal5, via5	R_{via5}	1.2
metal7-metal6, via6	R_{via6}	0.7
metal8-metal7, via7	R_{via7}	0.7

—Max. contact current—

0.16$\mu m \times$ 0.16μm metal1-poly/diff
0.2$\mu m \times$ 0.2μm via1-5,
0.4$\mu m \times$ 0.4μm via6,7

Layer-layer	mA/via	
metal1-poly/diff	I_{cp}	0.94
via 1-5	I_{via1-5}	0.7
via 6,7	$I_{via6,7}$	1.8

Layer	mA/μ m	
metal 1-6	I_{m1-6}	2.5
metal 7,8	$I_{m7,m8}$	7.5

Latch-up prevention

1. All wells must have at least one contact connected to V$_{DD}$.
2. Place well and substrate contacts wherever possible.
3. Max. spacing between transistor and well/substrate contacts: 50 μm.