

Exercises:

2002-10-26 kl. 8-13

Problem 1

An NMOS-transistor is made in the 0.35 μm CMOS process with the parameters according to the data sheet:

Given:

$W=100\mu\text{m}$, $L=1\mu\text{m}$

$V_{GS}=V_{DS}=1\text{V}$, $V_{SB}=0\text{V}$

The transistor is made using a simple straight layout (one finger)

The source and drain regions extend 1.2 μm from the gate

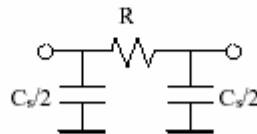
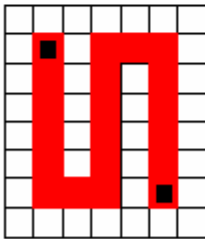
Long channel equations can be used.

Calculate:

C_{gs} , C_{gd} , C_{sb} , C_{db} , g_m and g_{ds} (6p)

Problem 2

A resistor in poly1 is made according to the layout below:



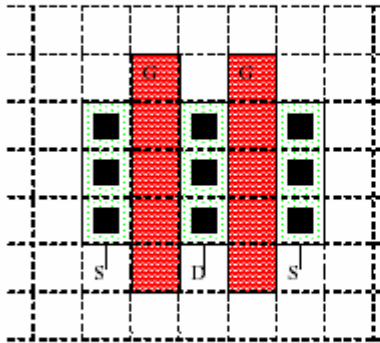
Each square is 4 μm x 4 μm . The contacts are drawn simplified. Use a contact resistance of 1 Ω , and a resistance of half a square for a poly square with contact.

Use the data sheet of the 0.35 μm process to calculate the resistance R and the total parasitic capacitance to the substrate C_s in the model to the right. (6p)

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Problem 2

A transistor has a layout according to the picture below. The distance between the dotted grid lines is $1\mu\text{m}$. (Some layout rules might be broken, but we neglect this to make the figure simpler). The transistor is biased with $V_S = V_B = 0\text{V}$, $V_G = 1\text{V}$, and $V_D = 2\text{V}$.



Use the data-sheet of the $0.35\mu\text{m}$ process and long channel equations to find:

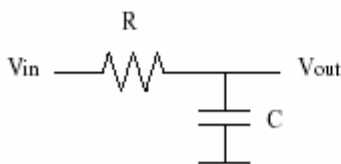
- W & L of the device (1p)
- C_{gs} , C_{gd} , g_m and f (2p)
- C_{sb} and C_{db} (3p)

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Problem 2.

A low-pass filter consisting of an RC-link is to be designed, see figure below. The transition frequency (-3dB) shall be 10MHz, and R is to be $1\text{k}\Omega$.

- Calculate the value of the required capacitance C. (1p)
- If C is realized using a quadratic shaped poly1-poly2 capacitance, calculate the side-length of the square. (3p)
- If R is realized using a $2\mu\text{m}$ wide poly1 resistor, calculate the length (disregard corners and contacts). (2p)



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Problem 1

A $30\text{k}\Omega$ resistor is to be implemented using N-well with $2\mu\text{m}$ width in the $0.35\mu\text{m}$ CMOS process. Draw a layout of the resistor with the physical dimensions indicated. The contacts should be included in the drawing, but they can be neglected in the calculations. (2p)

Calculate the total parasitic capacitance to the substrate when the voltage between the resistor and the substrate is 0V . (2p)

If half the parasitic capacitance is located at each end of the resistor, calculate the -3dB frequency of the transfer v_{out}/v_{in} , where v_{in} is imposed by a voltage source at one end of the resistor, and v_{out} is measured at the other end. (2p)

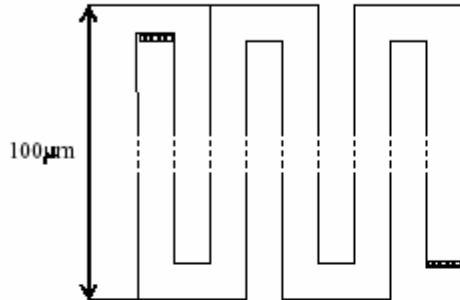
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Problem 1

A resistor is implemented in the 0.35 μm CMOS process in the poly1 layer. The layout is shown in the figure below. The width of the conductor track is 5 μm .

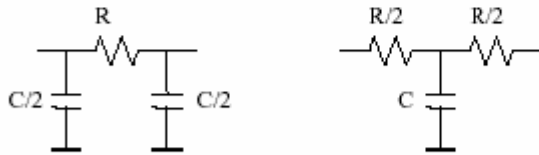
Calculate the resistance including the effects of corners and contacts. (3p)

Calculate the total parasitic capacitance to the substrate including edge-effects. (3p)



Problem 2

For simulation of the resistor of the previous problem different models can be used, differing in the high frequency behavior. We will examine the two models shown below:



C is the total capacitance to the substrate.

Assume one terminal to be connected to ground, calculate the impedance seen between the other terminal and ground for the two different models. (2p)

Plot the magnitude of the impedances vs. frequency in a diagram with log-log axes. (2p)

At what frequency does the impedance of the resistor in problem 1 stop being mainly resistive? (1p)

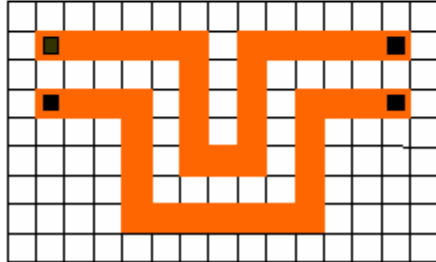
At what frequency do the two models start to give significantly different impedances? (1p)

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Problem 1

The layout of two poly1 resistors is shown in the figure below. The distance between the dotted grid lines is 1 μm .

- Calculate the resistance of the two resistors using the data sheet of the 0.35 μm process. The resistance of the squares at the contacts may be approximated as half that of a regular square. Include the contact resistances (to metal 1). (2p)
- The two resistors are to be matched. Why is this layout not suitable? How can it be improved (draw a new layout)? (4p)



Solutions:

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1. The transistor are in the saturation region ($V_{ds} > V_{gs} - V_t > 0$)

$$C_{gs} = \frac{2}{3}WLC_{ox} = \frac{2}{3} \cdot 100 \cdot 1 \cdot 4.60 \text{ fF} = 0.31 \text{ pF}$$

$$C_{gd} = WC_{gd0} = 21 \text{ fF}$$

$$C_{sb} = WL_{diff}C_{jn} + (W + 2L_{diff})C_{jnp} + WLC_{jn} = 100 \cdot 1.2 \cdot 0.93 + 102.4 \cdot 0.28 + 100 \cdot 1 \cdot 0.93 \text{ fF} = 111.6 + 28.7 + 93 \text{ fF} = 0.23 \text{ pF}$$

Drain is not on bulk potential.

$$C_{db} = \frac{WL_{diff}C_{jn}}{(1+V_{db}/V_{sw})^{0.31}} + \frac{(W+2L_{diff})C_{jnp}}{(1+V_{db}/V_{sw})^{0.31}} = \frac{111.6 \text{ fF}}{(1+1/0.69)^{0.31}} + \frac{28.7 \text{ fF}}{(1+1/0.69)^{0.31}} = 84.5 + 24.2 = 0.11 \text{ pF}$$

$$g_m = \mu C_{ox} \frac{W}{L} (V_{gs} - V_t) = 110 \cdot 10^{-6} \cdot \frac{100}{1} \cdot (1 - 0.50) = 5.5 \text{ mS}$$

$$I_d = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^2 = 1.38 \text{ mA}$$

$$r_{ds} = r_{ds,n} \cdot \frac{I_d}{I_{d,n}} = 30 \cdot 10^6 \cdot \frac{1.0 \mu}{1.38 \cdot 10^{-2}} = 21.7 \text{ k}\Omega$$

$$g_{ds} = \frac{1}{r_{ds}} = 46 \mu\text{S}$$

$$\text{Results: } C_{gs} = 0.31 \text{ pF}, C_{gd} = 21 \text{ fF}, C_{sb} = 0.14 \text{ pF}, C_{db} = 0.11 \text{ pF}, g_m = 5.5 \text{ mS}, g_{ds} = 46 \mu\text{S}$$

2. Some values are taken from the figure an others from data sheet.

$$\left. \begin{array}{l} R_{sp} = 9 \Omega / \square \\ C_{p1} = 0.119 \text{ fF} / (\mu\text{m})^2 \\ C_{sp} = 0.049 \text{ fF} / \mu\text{m} \end{array} \right\} \text{ From data sheet.}$$

$$\left. \begin{array}{l} 12 + 2 \cdot 2.11 + 2 \cdot 0.5 = 17.2 \square \Rightarrow 17.2 \cdot 9 + 2(2 \text{ cont.}) = 156 \Omega \\ \text{area} = 20 \square \cdot 16 (\mu\text{m})^2 \Rightarrow C_{ss} = 0.119 \cdot 20 \cdot 16 \text{ fF} \\ \text{circumference} = 168 \mu\text{m} \Rightarrow C_{sp} = 168 \cdot 0.049 \text{ fF} = 8.2 \text{ fF} \Rightarrow \\ C_s = C_{ss} + C_{sp} = 46 \text{ fF} \end{array} \right\} \text{ From figure.}$$

$$\text{Results: } R = 156 \Omega, C_s = 46 \text{ fF}$$

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Problem 2

a.

From clear thar drawn $W=6 \mu\text{m}$ and $L=1 \mu\text{m}$.

(since a $0.6 \mu\text{m}$ drawn L corresponds to a $0.5 \mu\text{m}$ effective: $W=6 \mu\text{m}$, $L=0.9 \mu\text{m}$)

b.

$$g_{m1} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) = 115 \cdot 10^{-6} \cdot \frac{6}{0.9} \cdot (1 - 0.46) = \underline{414 \mu\text{S}}$$

$$C_{gs} = \frac{2}{3}WLC_{ox} + WC_{gd0} = \frac{2}{3} \cdot 6 \cdot 0.9 \cdot 4.6 \text{ fF} = \underline{17.8 \text{ fF}}$$

$$C_{gd} = W \cdot C_{gd0} = 6 \cdot 0.21 \text{ fF} = \underline{1.3 \text{ fF}}$$

$$f_t = \frac{g_{m1}}{2\pi \cdot (C_{gs} + C_{gd})} = \underline{3.45 \text{ GHz}}$$

c.

Start with C_{sb} :

$$\text{Area} = 6 (\mu\text{m})^2 \quad \text{Perimeter} = 10 \mu\text{m}$$

$$C_{sb} = C_{sb}(0\text{V}) = c_{jn} \cdot 6 + c_{jnp} \cdot 10 = \underline{8.4 \text{ fF}}$$

Then C_{db} , where the reverse bias is 2V:

$$\text{Area} = 3 (\mu\text{m})^2 \quad \text{Perimeter} = 2 \mu\text{m}$$

$$c_{jn2V} = \frac{c_{jn}}{\left(1 + \frac{2 \text{ V}}{V_{jn}}\right)^{0.31}} = \frac{0.93 \text{ fF}/(\mu\text{m})^2}{\left(1 + \frac{2}{0.69}\right)^{0.31}} = 0.61 \text{ fF}/(\mu\text{m})^2$$

$$c_{jnp2V} = \frac{c_{jnp}}{\left(1 + \frac{2 \text{ V}}{V_{sw}}\right)^{0.31}} = 0.23 \text{ fF}/\mu\text{m}$$

$$C_{db} = c_{jn2V} \cdot 3 (\mu\text{m})^2 + c_{jnp2V} \cdot 2 \mu\text{m} = 0.61 \cdot 3 + 0.23 \cdot 2 \text{ fF} = \underline{2.3 \text{ fF}}$$

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No solution available

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Problem 1

R=30k Ω and R=1k Ω/\square for N-well (from data sheet) \rightarrow 30 squares

W=2 μm \rightarrow L=2 μm * 30 squares = 60 μm



Total capacitance at 0V:

$C_{jw} = 0.11 \text{ fF}/(\mu\text{m})^2$, $C_{jwp} = 0.53 \text{ fF}/\mu\text{m}$ (from data sheet)

$$C_{p\text{tot}} \approx WLC_{jw} + (2W+2L) \cdot C_{jwp} = 2 \cdot 60 \cdot 0.11 \text{ fF} + (120 + 4) \cdot 0.53 \text{ fF} = 79 \text{ fF}$$

-3dB frequency:

$$f_{-3\text{dB}} = \frac{1}{2\pi RC} = \frac{1}{2\pi R \cdot C_{p\text{tot}}/2} = 134 \text{ MHz}$$

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No solution available

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No solution available