



Local Oscillator for FM broadcast band 88-108 MHz



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Abstract

In this project describes the design work of the local oscillator for FM broadcast band 88MHz to 108MHz, Our design is implemented by using the Clapp oscillator configuration. The frequency can be tuned by voltage control of varactor BBY40. And the measurement results are also involved in the project.

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1. Introduction

The oscillator is of great importance in the superheterodyne receiver system. Figure 1.1 shows the block diagram of the superheterodyne receiver. In our design, the FM broadcast band is 88- 108MHz, in order to mix down to the IF frequency (10.7MHz), the frequency tuning range in our design is from 98.7MHz to 118.7MHz.

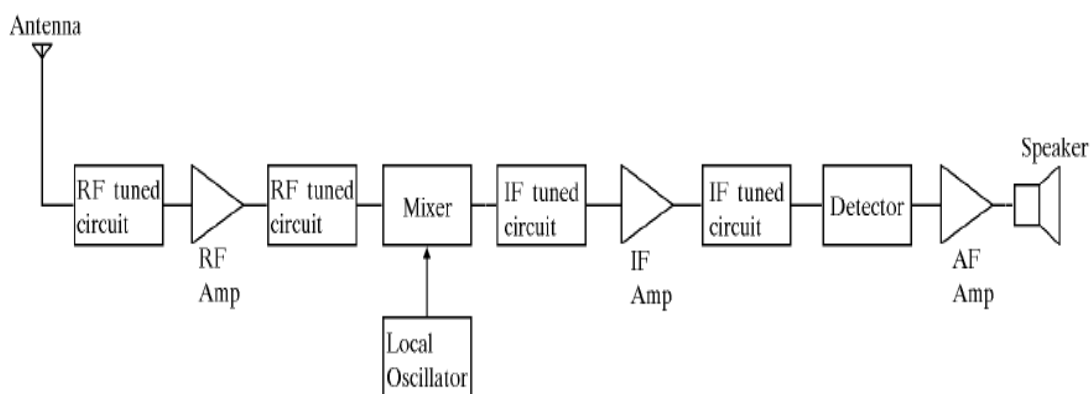


Figure 1.1 The superheterodyne receiver block diagram

1.1 Basic of Oscillators

To be able to analyze the oscillating conditions Black's feedback model is used. Here the oscillator is split into two blocks. One amplifier which is considered to be wideband and one feedback network that is usually frequency selective.[1]

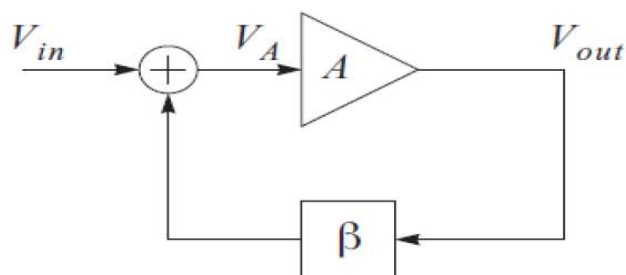


Figure 1.2 Black feedback model for oscillator

The transfer function for the amplifier with feedback can be calculated using the following equation.

$$V_{out} = A \cdot V_A$$

$$V_A = V_{in} + \beta \cdot V_{out} \Rightarrow A_f = \frac{V_{out}}{V_{in}} = \frac{A}{1 - \beta \cdot A}$$

If $|A \cdot \beta| = 1$ and $\angle(A \cdot \beta) = 0^\circ$, the feedback gain A_f will become infinite. And the system will perform continuous oscillation.

There are some configurations of oscillators: Colpitt, Hartley and Clapp Oscillator which is shown in figure 1.3.

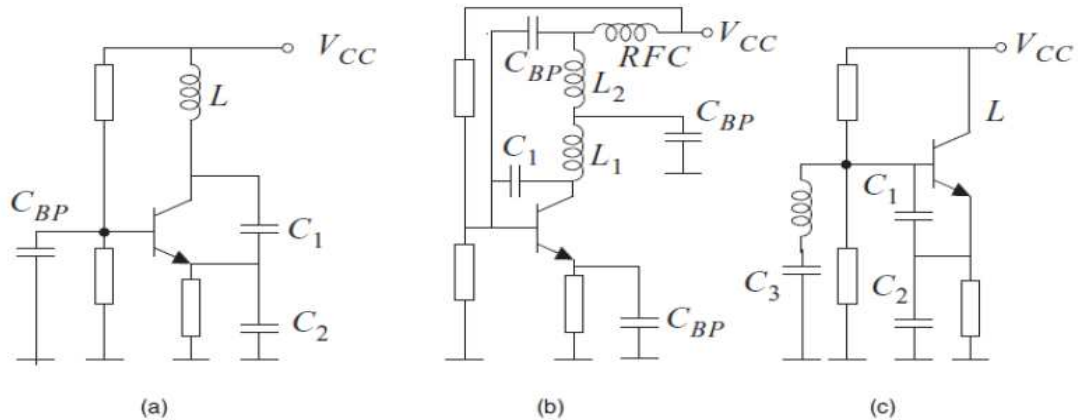


Figure 1.3^[2] Oscillator configurations: (a) Colpitts (b) Hartley (c) Clapp

Colpitts Oscillator with its feedback path through a capacitive voltage divider where two capacitors and one inductor determine the frequency of oscillation, see figure 1.3 (a). Hartley Oscillator use two series-connected coils and a single capacitor. The feedback can be through an inductive tap, see figure 1.3(b).

Clapp oscillators preferred over a Colpitts circuit for constructing a variable frequency oscillator. In a Colpitts Oscillator, the voltage divider contains the variable capacitor (either C1 or C2). This causes the feedback voltage to be variable as well, sometimes making the Colpitts circuit less likely to achieve oscillation over a portion of the desired frequency range. This problem is avoided in the Clapp circuit by using fixed capacitors in the voltage divider and a variable capacitor in series with the inductor^[2].

1.2 Specification

The Local Oscillator is used for a super heterodyne receiver. The tuning is voltage controlled. The specification is given as following.

1. Supply Voltage is 12V.
2. The oscillator frequency should be variable for reception of a specified

frequency band 88-108 MHz.

3. Any harmonics should be at least -16 dBc and other spurious at least -70 dBc.
4. Minimum output power should be 8 dBm.

2. Circuit design

The local oscillator system we designed can be divided into three parts: the oscillator, the buffer and the low pass filter. The schematic of the system is shown in Figure 2.1.

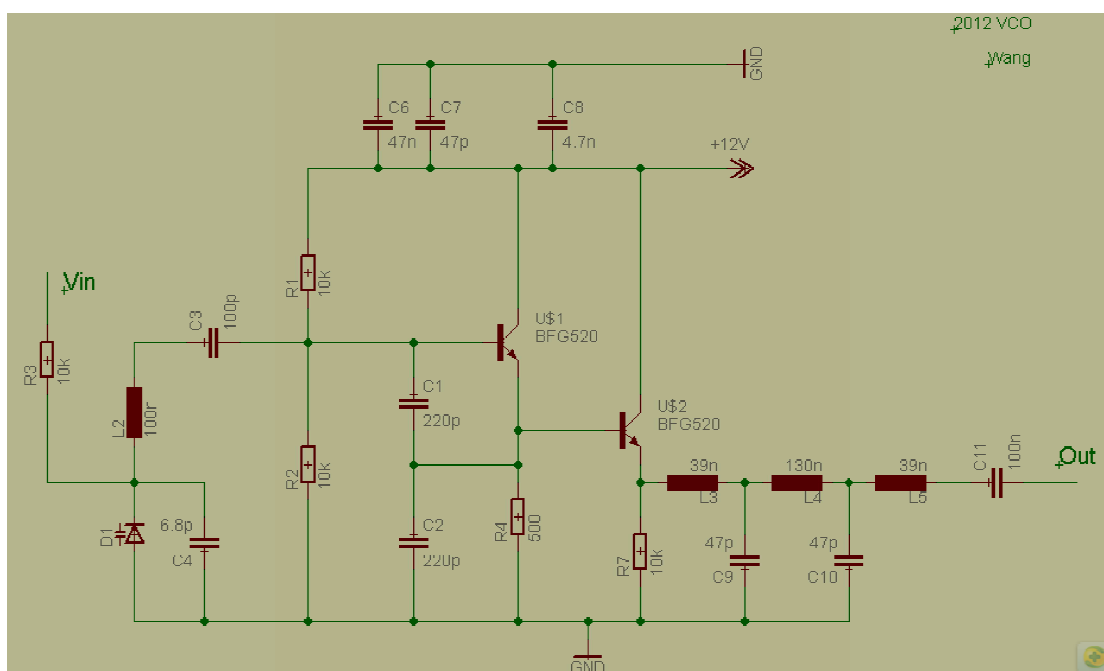


Figure 2.1 the schematic of the oscillator system

2.1 Voltage Controlled Oscillator

A voltage controlled oscillator (VCO), is an oscillator where the principal variable or tuning element is a varactor diode. DC voltage applied to the varactor diode to vary the capacitance applied to the tuned circuit in order to get the desired tuning range.

In our system, we use the bipolar BFG520 in the clapp structure with collector configuration. And a variable capacitance diode named BBY40 is use to achieve the frequency tuning from 98.7MHz to 118.7MHz. And a fixed capacitance is added across the varactor to make the tuning range to that required.

And the oscillator frequency can be written by:

$$\omega^2 L = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4 + C_{var}}$$

We choose the inductance $L=100\text{nH}$, then the total capacitance can be determined.

$$C_{tot\ min} = \frac{1}{(2\pi f_{max})^2 L} = \frac{1}{(2\pi \times 118.7 \times 10^6)^2 \times 100 \times 10^{-9}} = 18\text{pF}$$

$$C_{tot\ min} = \frac{1}{(2\pi f_{min})^2 L} = \frac{1}{(2\pi \times 98.7 \times 10^6)^2 \times 100 \times 10^{-9}} = 26.03\text{pF}$$

$$C_4 + C_{var\ min} = \frac{1}{\frac{1}{C_{tot\ min}} - \frac{1}{C_1} - \frac{1}{C_2} - \frac{1}{C_3}} = 27.42\text{pF}$$

$$C_4 + C_{var\ max} = \frac{1}{\frac{1}{C_{tot\ max}} - \frac{1}{C_1} - \frac{1}{C_2} - \frac{1}{C_3}} = 57.74\text{pF}$$

The varactor BBY40 is controlled by the control voltage and its characteristic is shown in Figure 2.2.

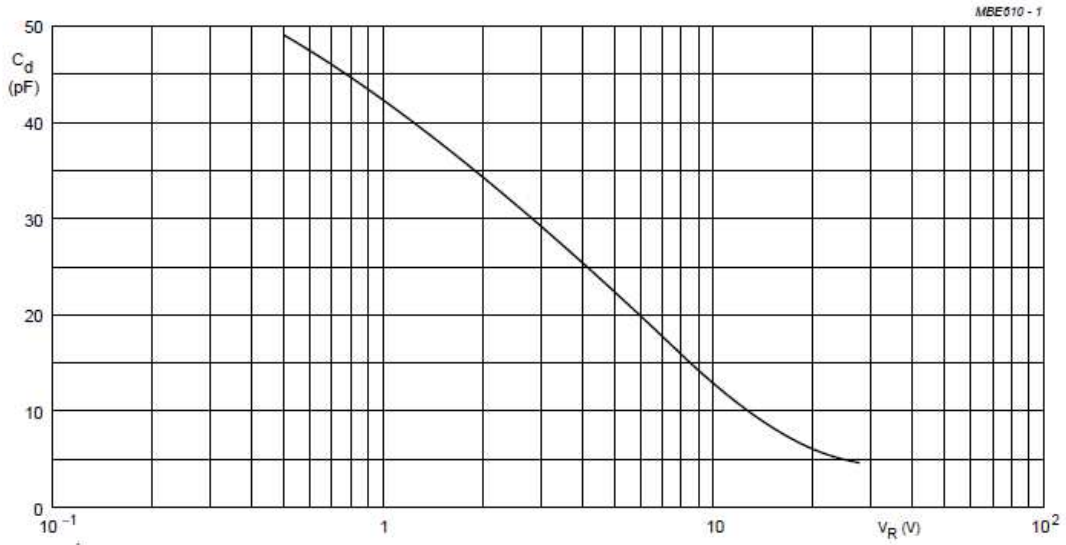


Figure 2.2 Diode capacitance as a function of reverse voltage; typical values [3]

According to its characteristics, we choose $C_4 = 6.8\text{pF}$, and then the range of the varactor and the control voltage which can be determined:

$$C_{var} \in (20.62\text{pF}, 44.9\text{pF})$$

$$V_{control} \in (0.8\text{V}, 6\text{V})$$

For its biasing,

$$V_B = \frac{10K}{10K + 10K} \times 12V = 6V$$

$$I_E = \frac{V_B - 0.7}{500} = 10.6mA$$

2.2 Buffer Amplifier

A buffer amplifier at the output is necessary to isolate the VCO from any output load variation and provide the required output power.

In our design, we used the collector configuration as the buffer amplifier. As we calculated above, the emitter voltage of the first stage is $6V - 0.7V = 5.3V$, which is high enough to drive this buffer stage. So we connect the emitter of the oscillator transistor to the base of the buffer amplifier without adding any other biasing circuit.

2.3 Low Pass Filter

The low pass filter is used for harmonic rejection. And we use the Butterworth filter. Its amplitude function fulfils:

$$A(f) = \frac{K}{\sqrt{1 + \left(\frac{\omega}{\omega_o}\right)^{2n}}} = \frac{K}{\sqrt{1 + \left(\frac{f}{f_o}\right)^{2n}}}$$

Where n is the order of the filter and f_o is a normalization frequency.

The tuning frequency range of the oscillator is from 99.7MHz to 118.7MHz. And in the pass band the amplitude should be equal to or higher than -2dB up to 118.7MHz.

$$A(118.7 \times 10^6) = \frac{K}{\sqrt{1 + \left(\frac{118.7 \times 10^6}{f_o}\right)^{2n}}} = -2dB = 0.7943$$

And the rejection band is defined by the -20dB corner at 200MHz.

$$A(200 \times 10^6) = \frac{K}{\sqrt{1 + \left(\frac{200 \times 10^6}{f_o}\right)^{2n}}} = -20dB = 0.1$$

Combining the results from the two corner we get $n=5$. According to the Butterworth Ladder Filters table, we can get:

$$L_1' = 0.618, C_2' = 1.6180, L_3' = 2.000, C_4' = 1.6180$$

Thus, we can calculate the value of each component:

$$L_1 = 39nH, C_2 = 41pF, L_3 = 127nH, C_4 = 41pF, L_5 = 39nH$$

3.Simulation

Before the implementation, we try to simulate the circuit by using ADS 2011. Figure 3.1 shows the results around 100MHz, and the output power is 9.324dBm and the neighboring harmonic is only about -22dBm, which satisfy the -16dBc requirement.

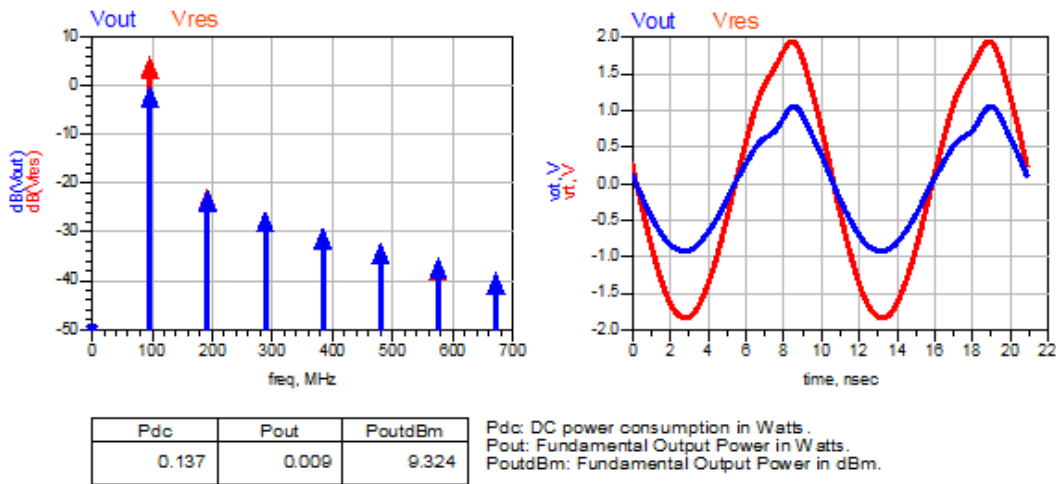


Figure 3.1 The simulation result by using ADS2011

4. PCB design

After we finish the schematic and the simulation, we design the PCB layout by using Eagle. The PCB layout and the final circuit are shown in Figure 4.1 and Figure 4.2 respectively.

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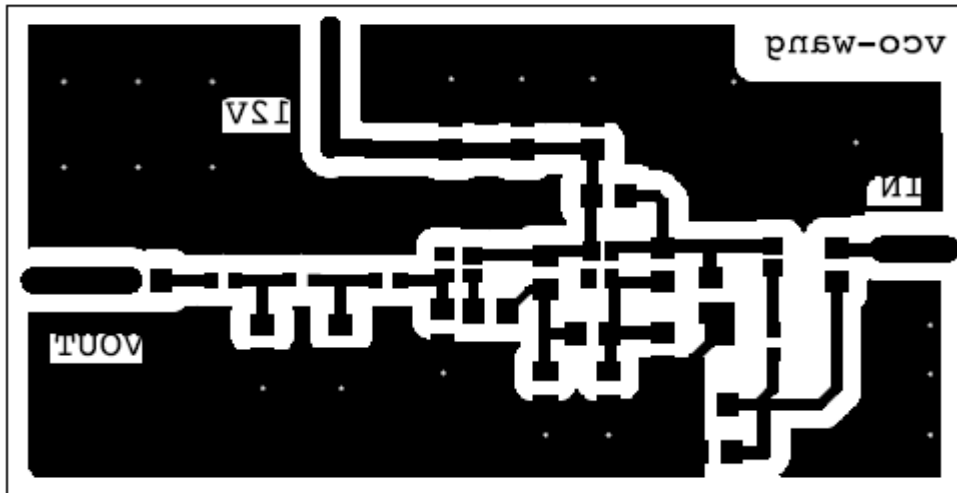


Figure 4.1 The layout of the circuit

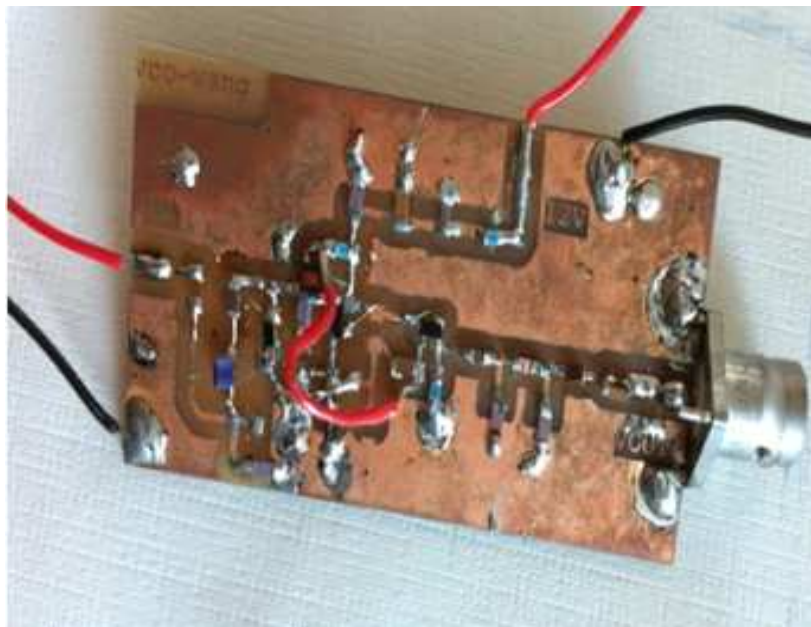


Figure 4.2 The final PCB board

5. Results

Finally, we use the spectrum analyzer to measure the circuit. Figure 5.1 and figure 5.2 shows the output results at frequency 98.7 MHz and 118.7MHz respectively.

Figure 5.3 and Figure 5.4 give the harmonics test.

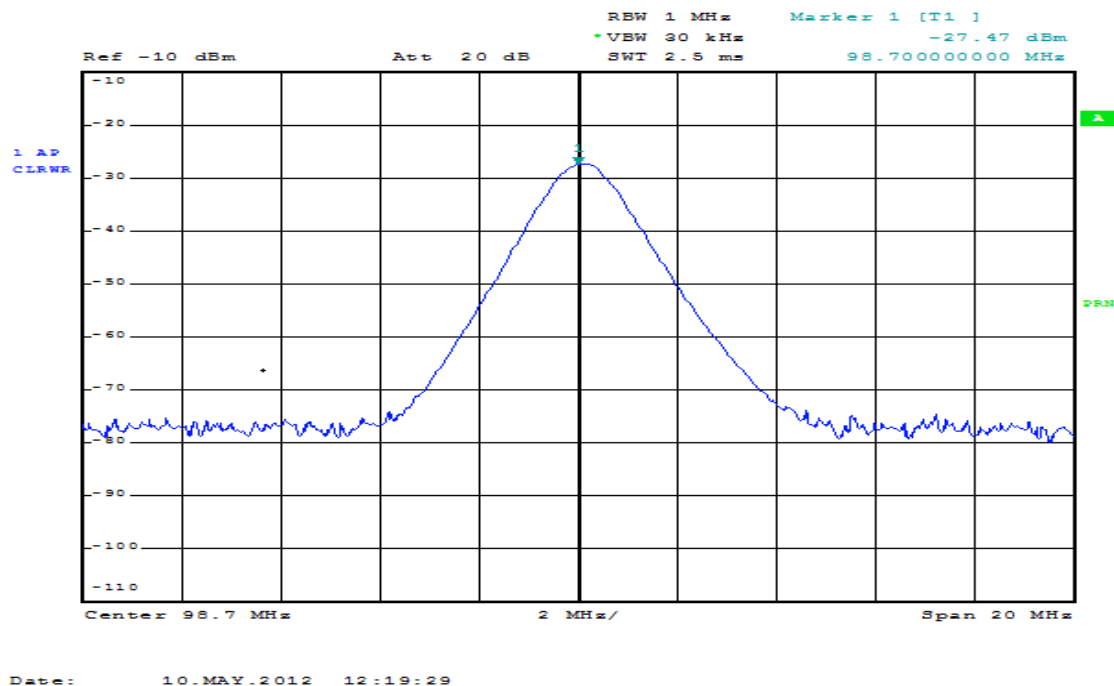


Figure 5.1 the output signal around 98.7 MHz

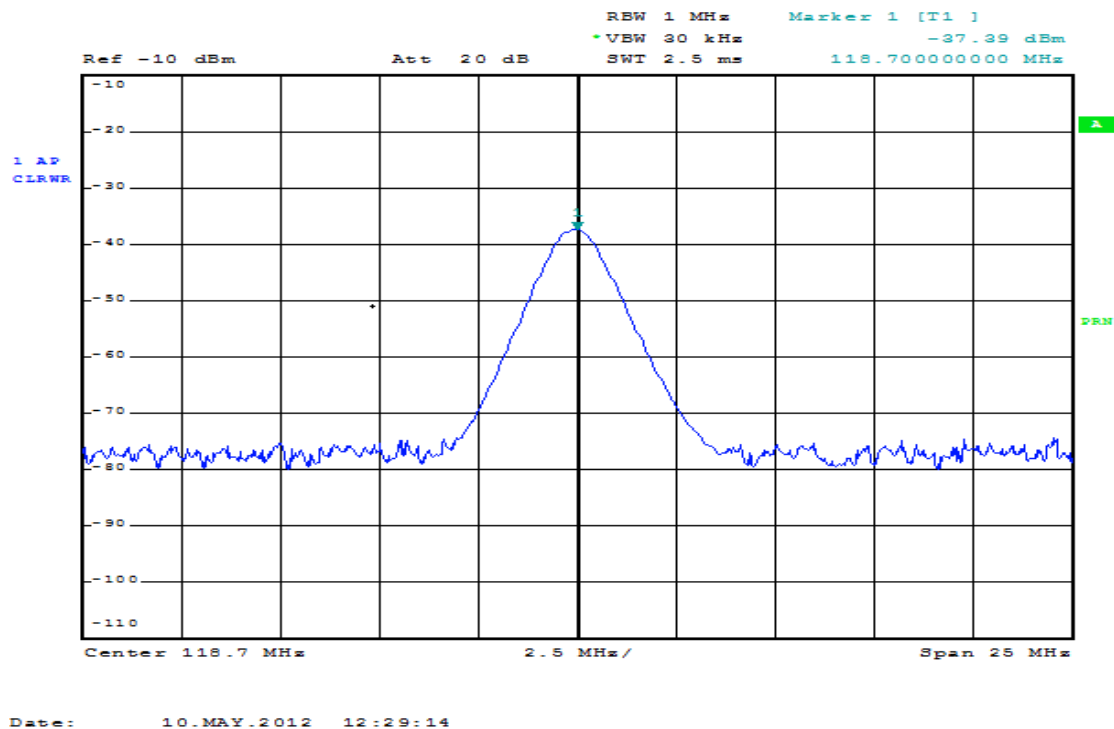
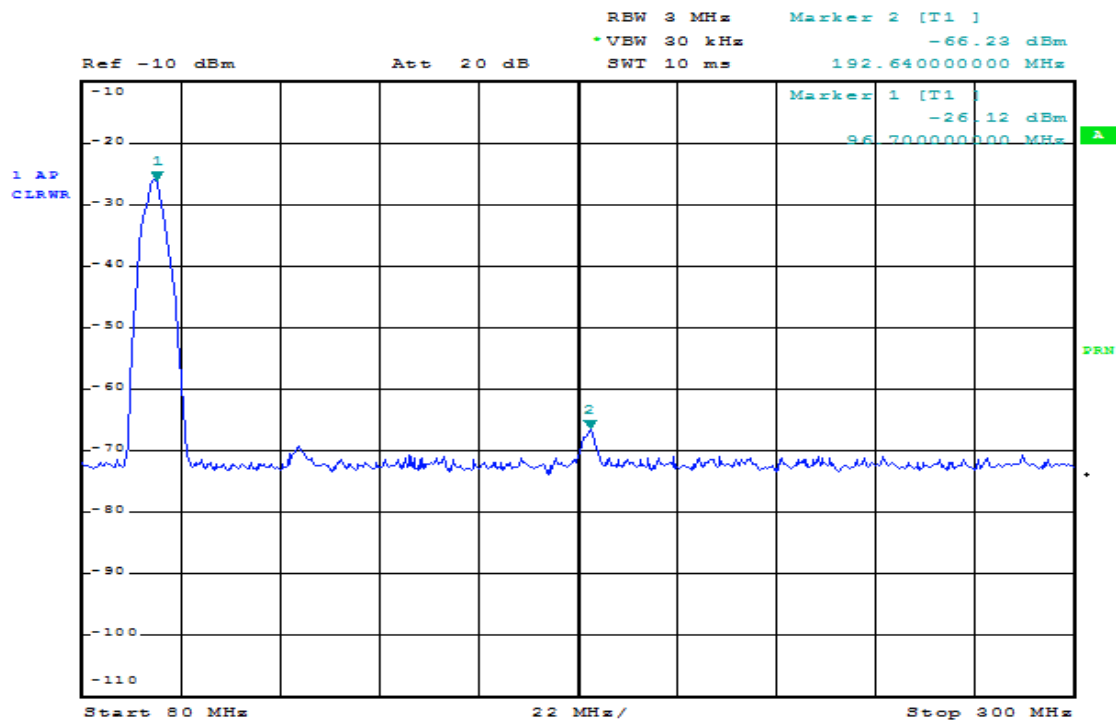


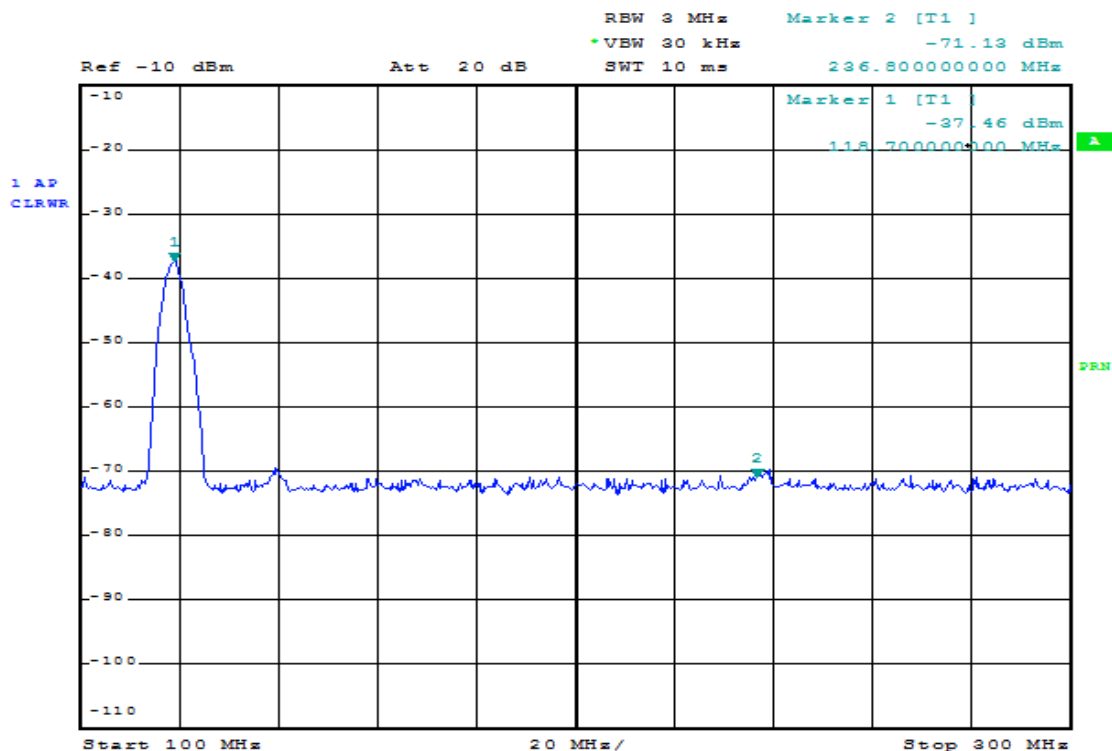
Figure 5.2 the output signal around 118.7 MHz

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Figure 5.3 The harmonics test result around 96.7 MHz



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Figure 5.4 The harmonics test result around 118.7 MHz

From the figure 5.1 and figure 5.2, we can find that the output power for the

fundamental frequency is too weak, just around -30dBm. And there is a significant difference between the simulation and the measurements. This is possible because the transmission lines were not considered in the simulation, which will also affect the circuit. And the low pass filter causes power dissipation as well. To increase the output power, we can change the configuration of the buffer amplifier to get the higher output gain.

From the figure 5.3 and figure 5.4, we can find that the neighboring harmonic is around -70dBm, which meet the requirement.

6. Conclusion

In this project, a local oscillator with the output tuning range from 98.7MHz to 118.7MHz is designed. We designed the schematic and the circuit was simulated by using ADS 2011 and later a PCB layout was created using Eagle. Finally, we used the spectrum analyzer to test the circuit. Besides the output power is too weak, the rest of the results meet the requirement. For the further work, CE configuration amplifier buffer can be used to increase the output power.

We obtained some experience through this project:

1. The DC operating points of the transistor should be well calculated.
2. The layout of the components should be put in the reasonable places to reduce wiring in order to minimize the adverse effect of the transmission line.
3. When doing the layout, it is best to separate the AC part from the DC parts in order to reduce the interaction. And in the DC part, an inductor can be added to block the AC signal.

7. Acknowledgements

We would like to thank our supervisor, Göran Jönsson for his generous support throughout the whole project. His advices were very useful in circuit and layout design. We would also like to extend our thanks to Lars Hedenstierna, who produced our circuit board.

8. Reference

[1] G.Jönsson, Department of Electrosience, Lund University, Slides from the Radio course, 2011

[2] L.Sundström, G.Jönsson, H.Börjesson, Department of Electrosience, Lund University, Radio Electronics, 2004

[3] www.nxp.com