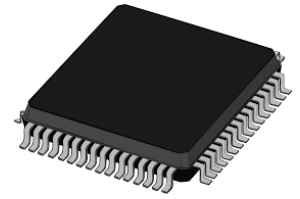# Lab 1

EITP15

Introduction to Altium Designer

Goals
- Getting familiar with the workflow in Altium designer
- To be able to design two layered PCB

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Contents

1 Introduction

During this laboratory exercise the PCB in Figure 1 will be designed. It is a double sided PCB that features a microcontroller[1] (ATmega644PA) that is powered via a linear voltage regulator (TPS79333DBR). Two buttons and two LEDs are connected to the microcontroller. Furthermore all the IO pins are routed to pin headers.
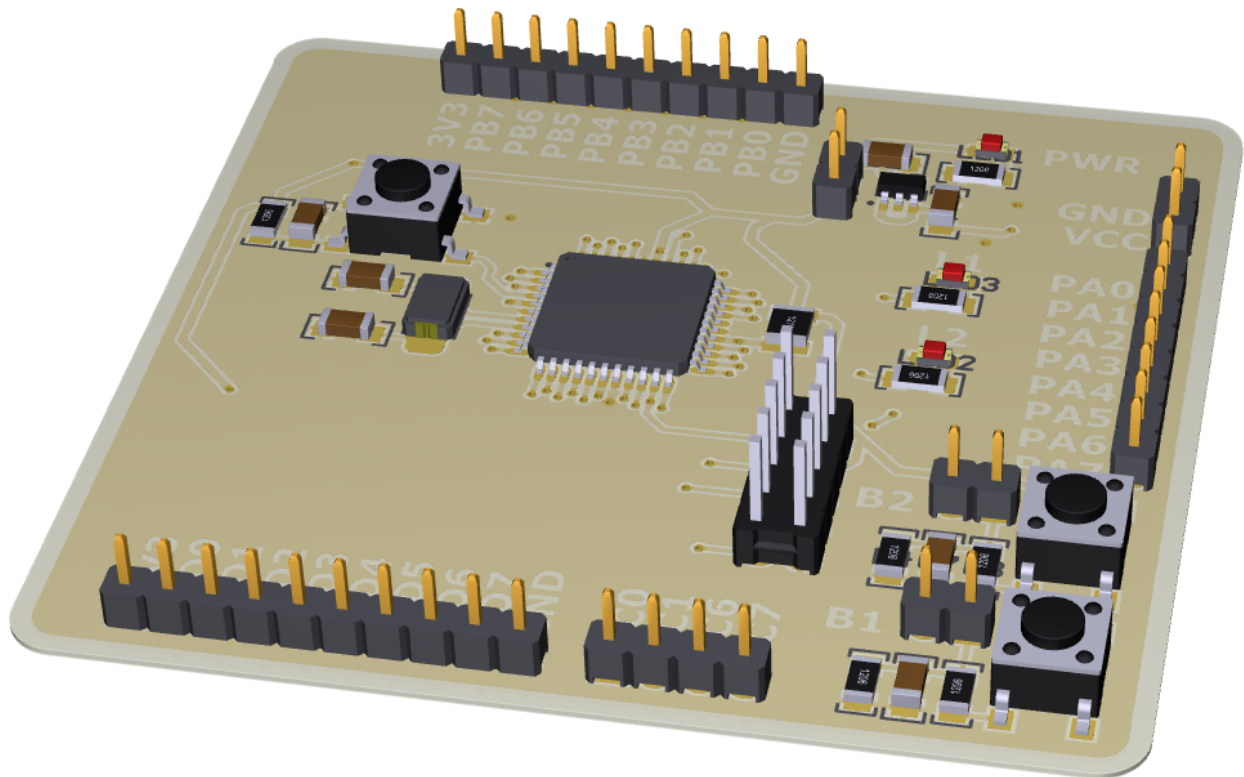

Figure 1: A picture of the PCB that will be designed during this laboratory exercise.

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[1]A microcontroller is a single chip computer, containing a processor, memory and programmable IO peripherals such as IO pins, timers and communication devices amongst others.

1.1 Altium Designer Work Flow

In Altium Designer, and any other PCB design software for that matter, a project is divided into to parts. The first part is the schematic and the second is the PCB layout. The schematic is a logical and often simplified representation of the PCB. It is for that reason here all the components are connected. Each component has a schematic symbol and footprint. The footprint is the physical representation of the schematic symbol and is thus used in the PCB layout.
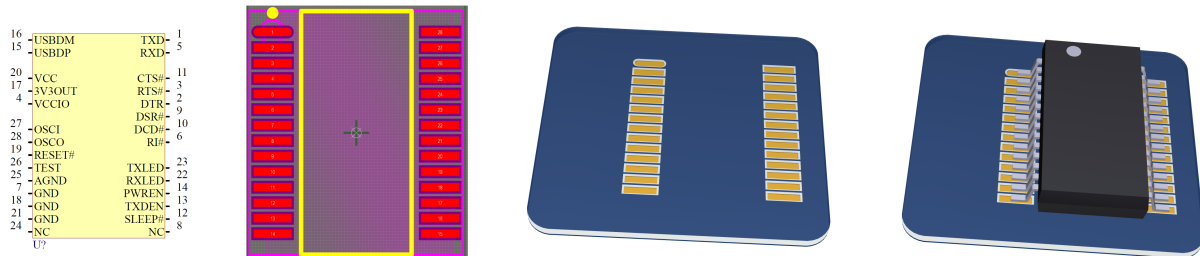

Figure 2: Left - The schematic symbol. Sencond left - The corresponding footprint. Second right - A PCB with the footprint. Right - The PCB with the actual IC mounted.

Each pin in the schematic symbol and each pad[2] in the in the footprint is labeled with a number, see Figure 2 (you will have to zoom in quite a lot to see the number of the footprint's pads). This number is called a *designator*. A connection to the pin with the designator 1 in the schematic yields a connection to the pad with the designator 1 in the PCB layout. Pin and pad designators are local to each component. The components of a PCB project are usually stored in a library. In Altium Designer there are several different types of libraries where each of them has their individual strengths and weaknesses. The type of library that will be used during the lab is called an *integrated library*. It is realtiviely simple to set up and is easy to use and maintain.

The common strategy when designing a PCB is to first complete the schematic and when that is done, start with the physical layout. To use the schematic as blueprint for the layout the schematic has to be annotated and then compiled. When compiling a schematic a netlist is generated. This netlist is a description of how the components are connected. To successfully compile the schematic it has to be annotated. Annotating results in that each component gets a unique component designator. Before annotating the schematic the designator usually consists of a letter followed by a question mark, see the the lower left corner of the schematic symbol in Figure 2. After the annotation the first designator of the same component will be replaced with U1 and the second with U2 and so forth. See Figure 3.

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[2]A pad is an area of copper where a leg/foot of a component will be soldered to the PCB.
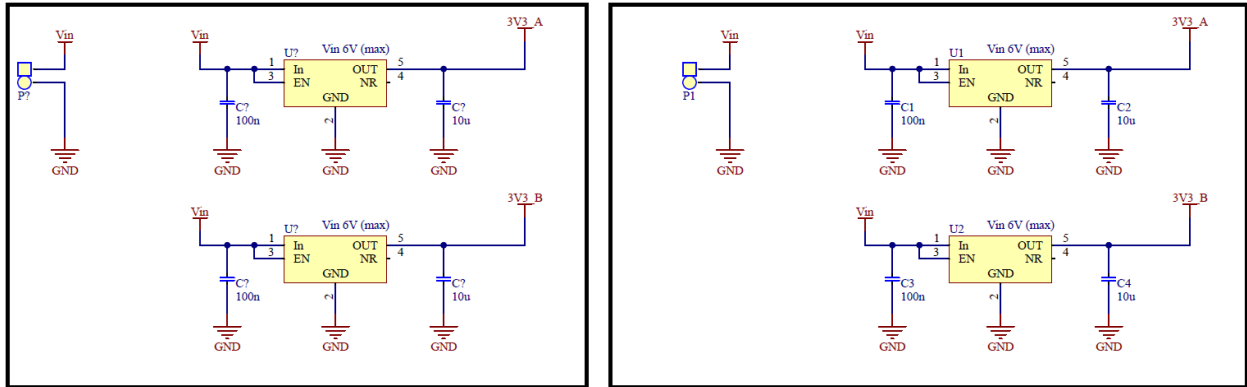
Figure 3: Left - Before annotating. Right - After annotating.

When the generated netlist is imported to the PCB layout all of the used component's footprint will be displayed. See Figure 4.
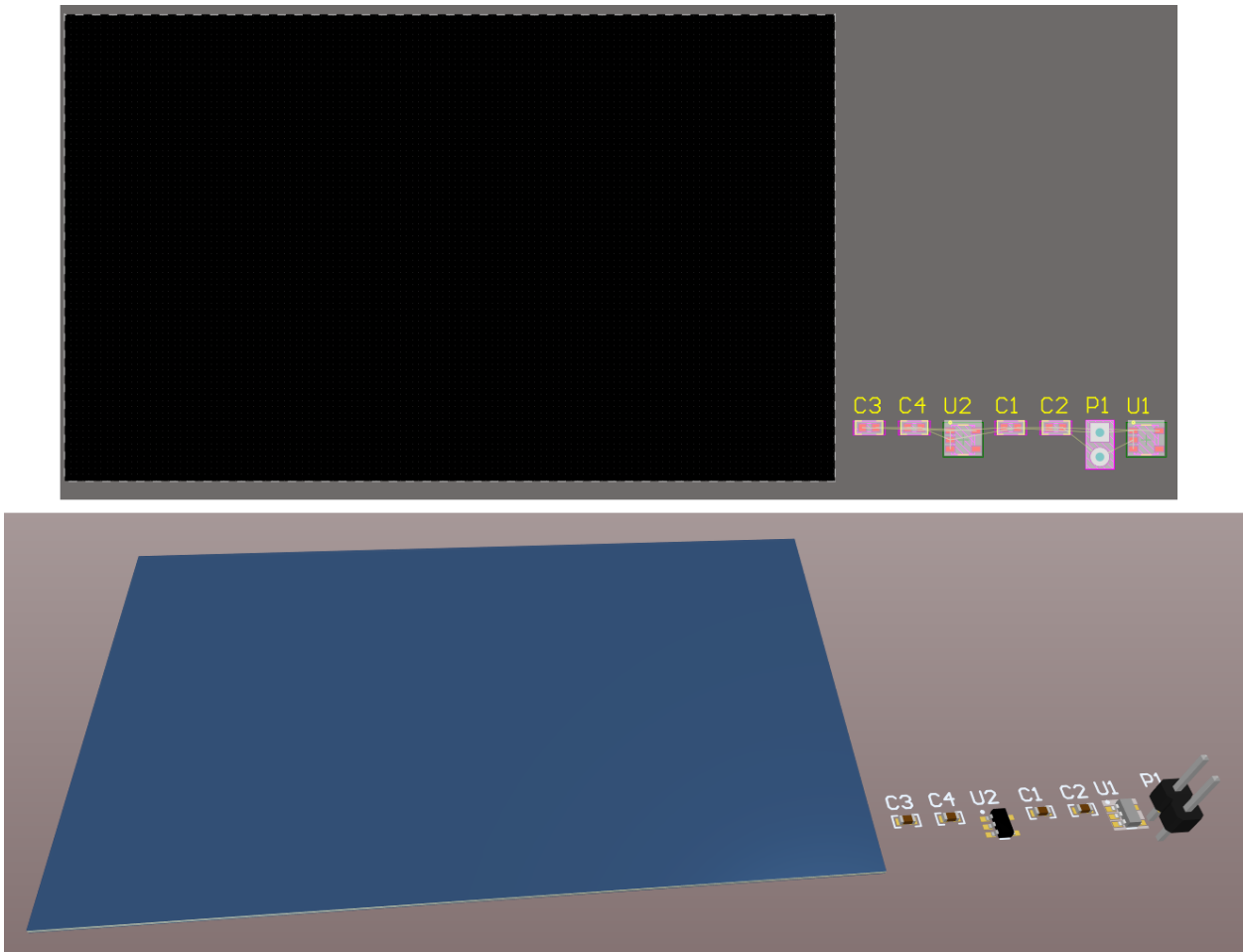

Figure 4: Top - The PCB layout. Bottom - A 3D view of the PCB and the components.

When this netlist is imported to the PCB layout the PCB design rules should be set. This is where you set the clearance between tracks, pads, components and so on. When routing tracks and placing components you will be warned immediately if the design rules has been violated. In Figure 5 the component C5 is placed on component XT1, this of course violates the design rules. Objects that violates the design rules are colored green.
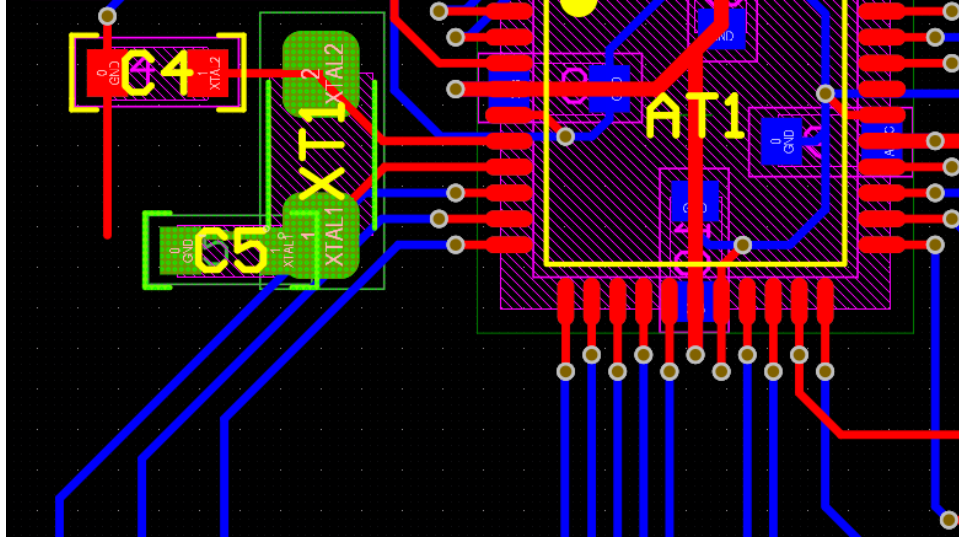

Figure 5: Top - The PCB layout. Bottom - A 3D view of the PCB and the components.

When the design rules has been set the layout and routing work begins. This is in many cases an iterative process and can be challenging, especially when considering high speed electronics.

In Figure 5 some components and tracks are colored red and some blue. The red components and tracks are on the top layer and the blue are placed on the bottom layer. To connect tracks on the top layer and the bottom layer vias are used. A via is a circular pad on both the top and bottom layer with a hole drilled through the center. The hole is copper plated to form a connection between the two pads. In Figure 6 a section of the PCB that will be designed during this lab is shown. The image on the top is the PCB layout in 2D and the image on the bottom is a 3D view of the same section.
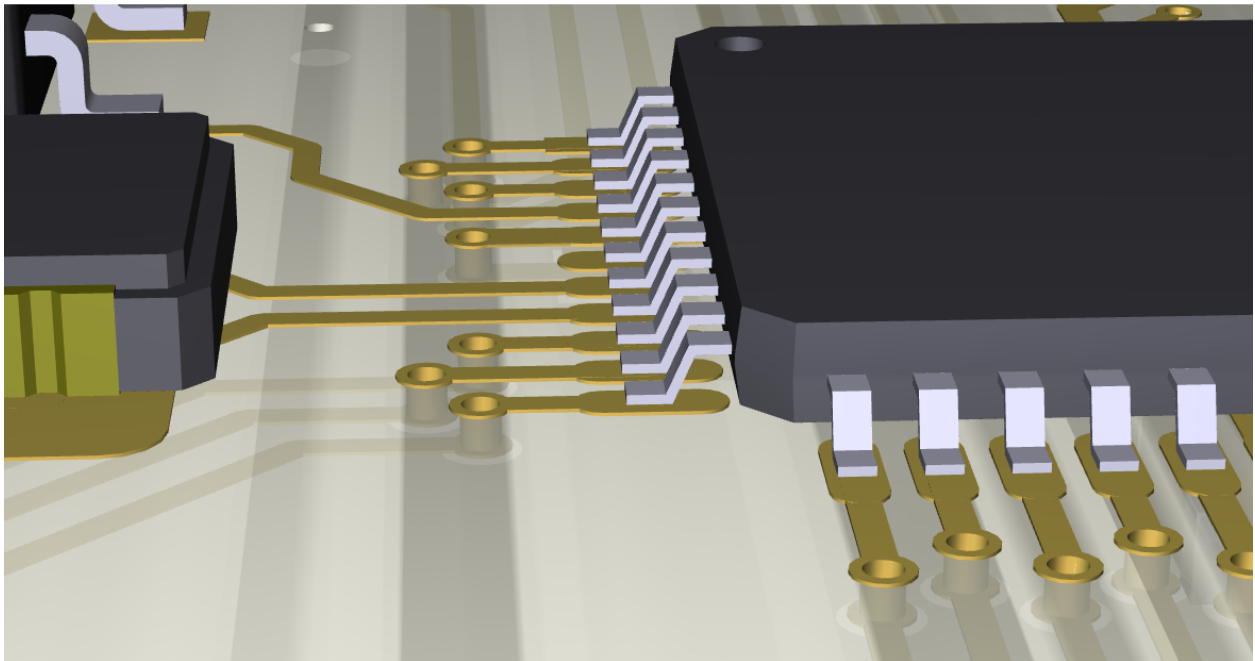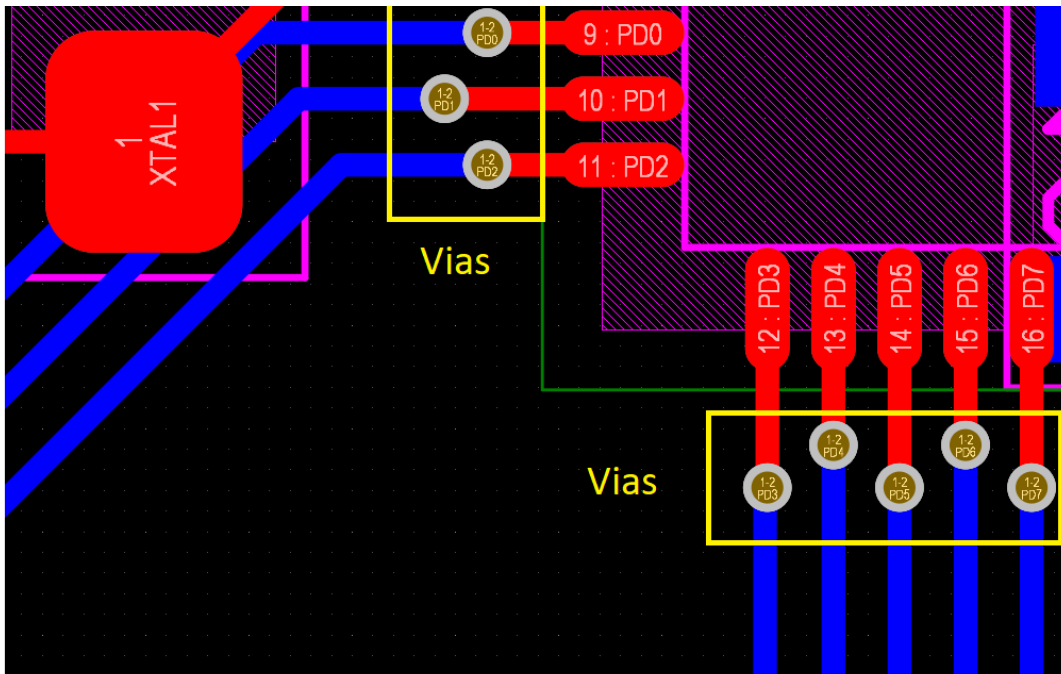
Figure 6: Top - The PCB layout with the vias marked by yellow rectangles. Bottom - A 3D view of the PCB with the PCB core material transparent.

1.2 Setting up Altium Designer

A integrated library containing the schematic symbols and their corresponding footprints that will be used in this lab is available here:
`https://www.eit.lth.se/fileadmin/eit/courses/eitp15/lab/eitp15_lab1_lib.zip`

Altium Designer is installed on all computers in room E:4123. The software can be found in the start menu once you have signed in on the machine. Your project needs to be placed in a folder under the path shown below:
C:\users\<login-id>\Program

If the project is not placed in the specified folder Altium Designer will not work properly. **Please note that it is important that you copy your work to a USB drive or your network drive (H:) before you sign out. Otherwise there is a risk of loosing it.**

Watch the video on the following link to see how to create a project and how to add a schematic, a PCB and how to use the provided library:

`https://youtu.be/gN9cd1uu7sg`

2 Lab assignement: The Schematic

In Figure 7 the schematic of the design is shown. All the necessary components can be found in the provided library. Some of the connections in the schematic is made by net labels. This is a why to connect parts/pins without placing a wire. This can be used to make the schematic more easily read, but should not be over-used.

See Table 1 for the components name in the lab library. The component designator is visible in Figure 7.

Designator	Component Name
AT1	ATmega644PA
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11	1206, capacitor
JT1	Atmel JTAG
L1	Coil
LED1, LED2, LED3	0805, LED
P1, P2, P7, P8	1x2 Pin Header
P3	1x8 Pin Header
P4, P5	1x10 Pin Header
P6	1x4 Pin Header
R1, R2, R3, R4, R5, R6, R7, R8	1206, resistor
TB1, TB2, TB3	Button SMD
VR1	TPS79333DBR
XT1	XTAL TXC 7A

Table 1

Tasks:

- Use the components in the library to make a copy of the schematic in Figure 7.

- Annotate the schematic.

- Compile the schematic.

There are several videos available to guide you. See Table 2 below.

Table 2: Useful videos regarding schematics.

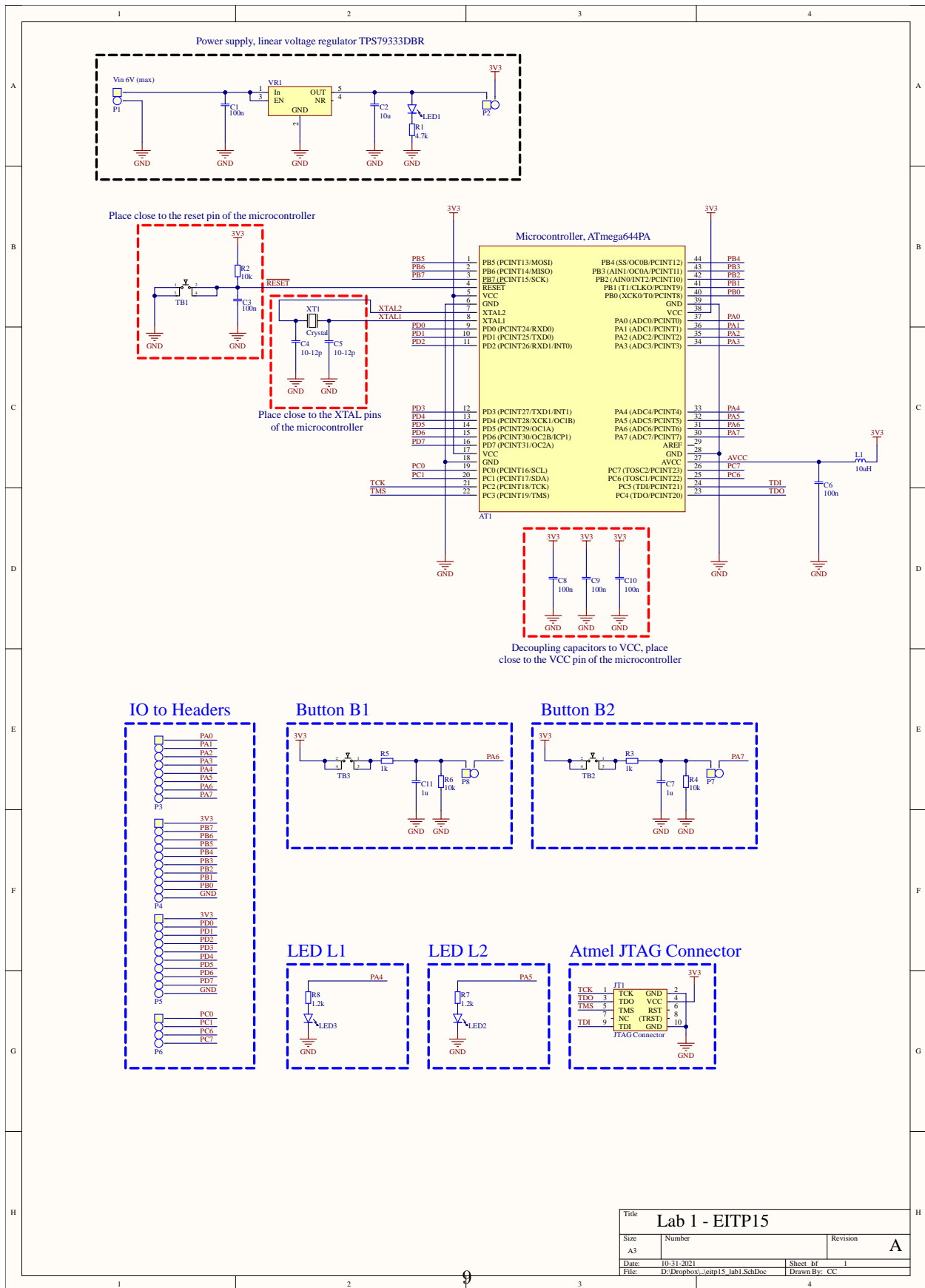| Description	Link
Placing components, wiring and net labels	`https://youtu.be/LQHYGO2MLpI`
Annotate and compile the schematic	`https://youtu.be/Wd3s5h_X7wE`

Figure 7: The schematic of the PCB.

3 Lab assignement: The Layout

Before starting the work regarding the layout there are a couple of things to consider. Some of the components needs to be placed close to the microcontroller. All of these components are inside dashed rectangles coloured red. In general should all decoupling capacitors be placed as close as possible and on the same layer as the the device they are decoupling. This is because it is desirable to reduce the parasitic inductance a PCB track gives rise to. The component labeled `XT1` is a crystal. Crystals are used by oscillators to create clock signal with an precise frequency. By reducing the distance between the crystal and the corresponding IC the risk for corrupting this signal is reduced. The capacitor on the reset track should also be placed relatively close to the reset button. The button and the capacitor should be placed close to the MCU. By doing this it is less likely that the microcontroller is reset by an induced interference.

Tasks:

- Import the compiled netlist.
- Set the design rules.
- Place the components.
- Route the PCB.

Links to useful videos can be found in Table 3 beloork.

Table 3: Useful videos regarding PCB layouts.

Description	Link
Importing the netlist and setting up the design rules	`https://youtu.be/HcDCcFdiwuw`
Cross selection and organize components in the PCB layout	`https://youtu.be/3Wm6NZCQEb8`
Place and route	`https://youtu.be/t-jJME8YkKQ`
Board outline	`https://youtu.be/gQRpAoQhhZQ`
Ground planes	`https://youtu.be/HbPcbnbwUUc`
Grid and measurements	`https://youtu.be/18zgK7TizR4`
Design rule check	`https://youtu.be/FFoDoFPC43Q`

4 Lab assignement: Generating Documentation And Fabrication Files

In this part of the laboratory exercise we will generate the files that are nessesary for fabricating the PCB. These files are often of a format called Gerber. Furthermore we will also generate a PDF of the schematic. The table 4

Table 4: Useful videos regarding generating documentation and fabrications files.

Description	Link
Fabrication files	`https://youtu.be/66xTjiJ7EAM`
Schematic print	`https://youtu.be/hhex5rG9g8o`