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REVIEW

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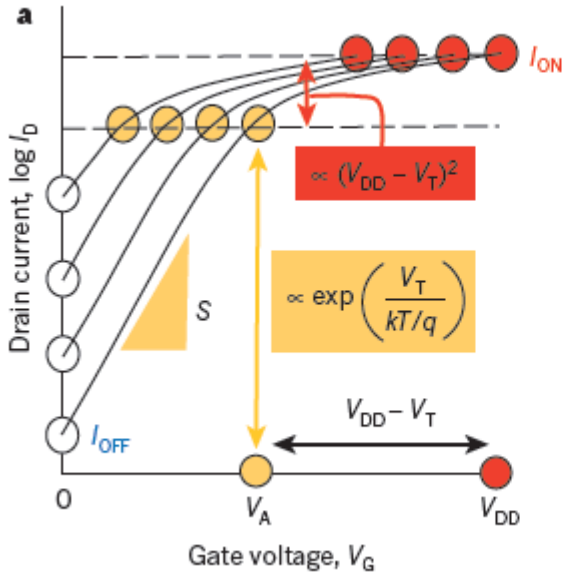
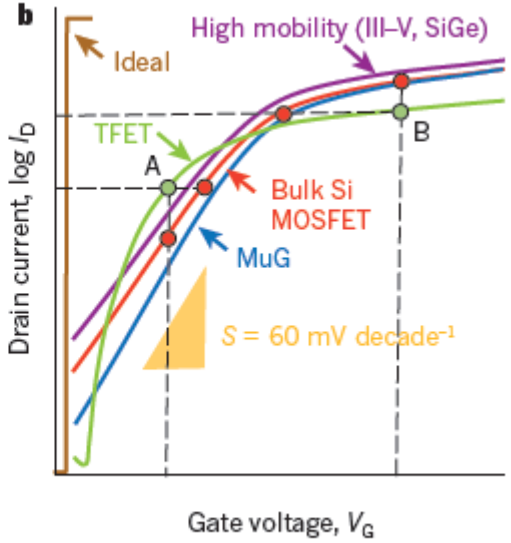
# Tunnel field-effect transistors as energy-efficient electronic switches

Adrian M. Ionescu[1] & Heike Riel[2]

**Power dissipation is a fundamental problem for nanoelectronic circuits. Scaling the supply voltage reduces the energy needed for switching, but the field-effect transistors (FETs) in today's integrated circuits require at least 60 mV of gate voltage to increase the current by one order of magnitude at room temperature. Tunnel FETs avoid this limit by using quantum-mechanical band-to-band tunnelling, rather than thermal injection, to inject charge carriers into the device channel. Tunnel FETs based on ultrathin semiconducting films or nanowires could achieve a 100-fold power reduction over complementary metal-oxide-semiconductor (CMOS) transistors, so integrating tunnel FETs with CMOS technology could improve low-power integrated circuits.**



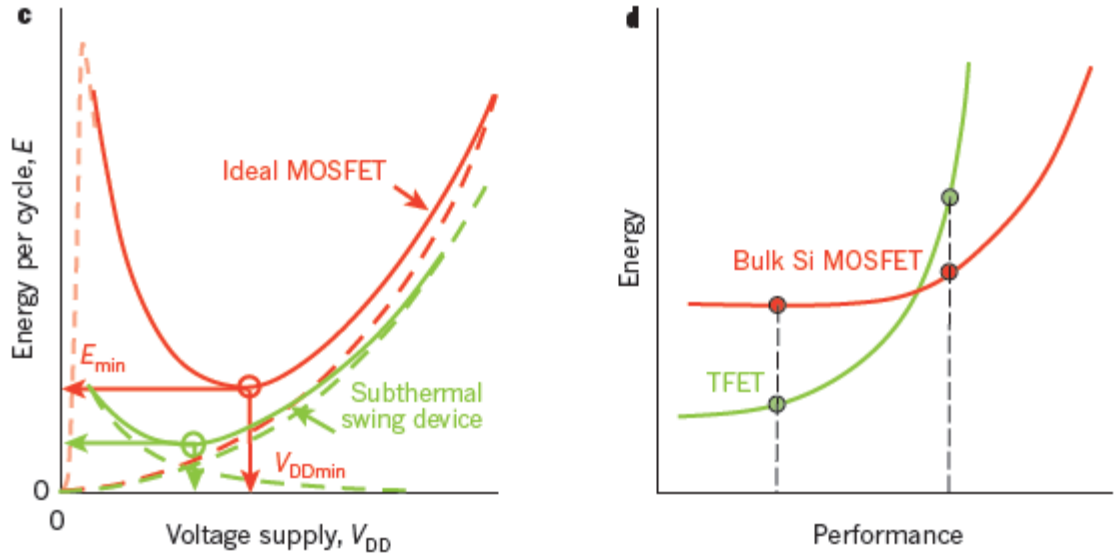




$$S = \underbrace{\frac{dV_G}{d\Psi_s}}_{m}\underbrace{\frac{d\Psi_s}{d(\log_{10} I_D)}}_{n} \cong \left(1 + \frac{C_d}{C_{ox}}\right)\ln 10\frac{kT}{q}$$

$$\rightarrow \frac{kT}{q}\ln 10 \cong 60 \text{ mV decade}^{-1} \mid T = 300 \text{ K}$$

Two a:pproaches to reduce Vdd:
- Reduce Vt to maintain (Vdd-Vt)
- Reduce S

# Energy Required for Switching



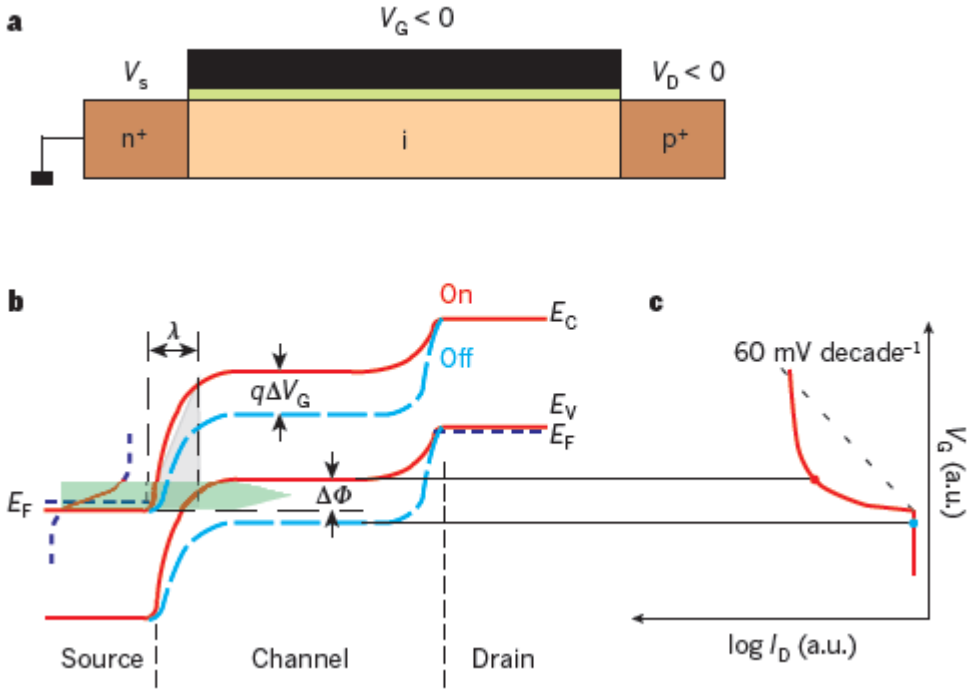

$$E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d C V_{DD}^2 + L_d I_{OFF} V_{DD} \tau_{delay}$$

$$\approx \alpha L_d C V_{DD}^2 = L_d C V_{DD}^2 \frac{I_{OFF}}{I_{ON}} = L_d C V_{DD}^2 \left(\alpha + \frac{I_{OFF}}{I_{ON}}\right)$$

$$\approx L_d C V_{DD}^2 \left(\alpha + 10^{\frac{-V_{to}}{S}}\right)$$

$$P = \alpha L_d C V_{DD}^2 f = I_{OFF} V_{DD} \approx K C V_{DD} = I_{OFF} V_{DD}^3$$

# Principle of Operation



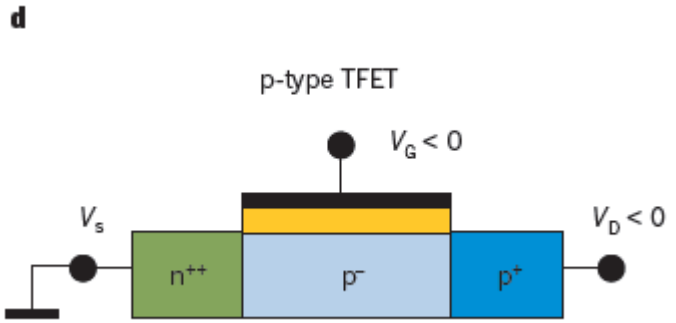

-**On-state:**
Carriers may tunnel from the source to the channel

-**Off-state:**
Tunneling from the source is restricted due to the band gap

**Tunnel injection across triangular barrier**

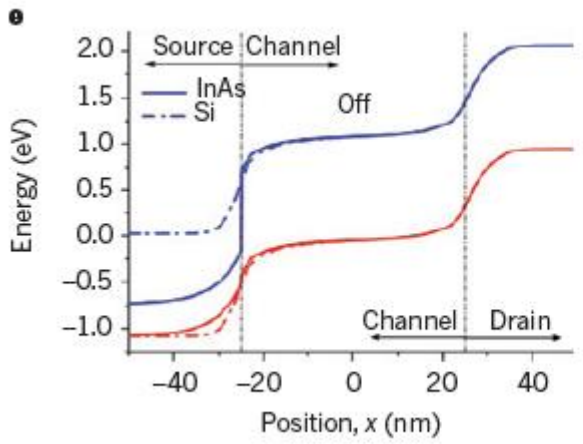
$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\Phi)}\right)$$

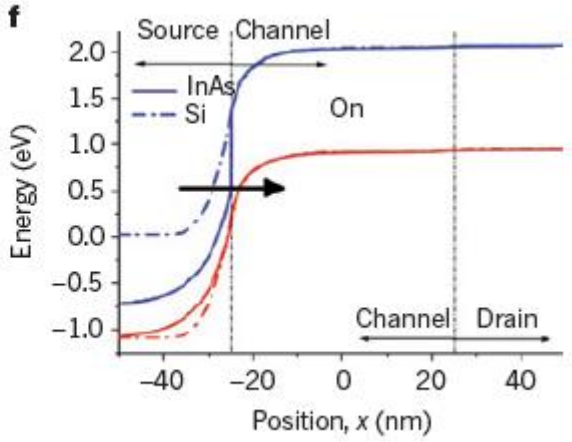
# pFET Implementation



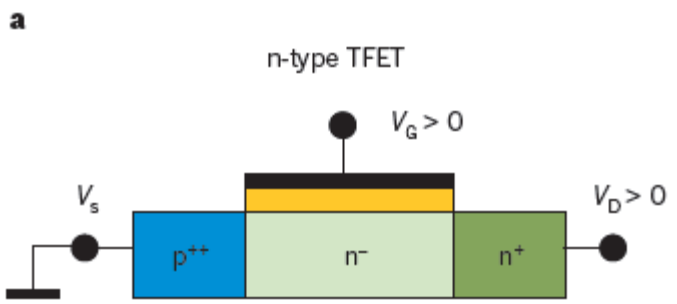

**pFET operation:**
Gate is used to lift the bands in the gate region

**pFET booster:**
Use n++ InAs in the source



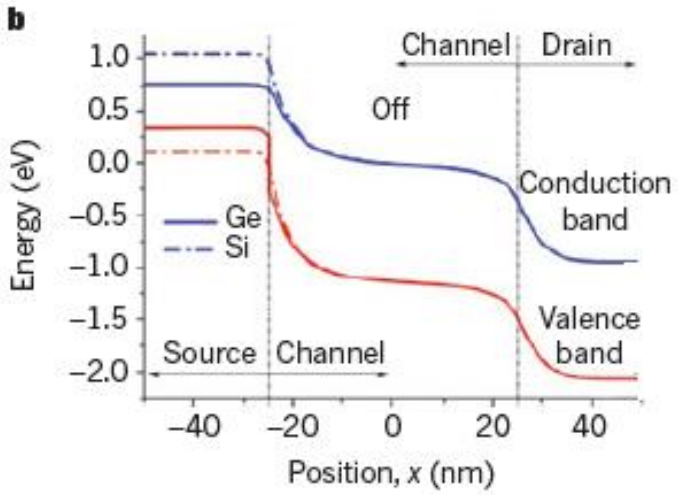



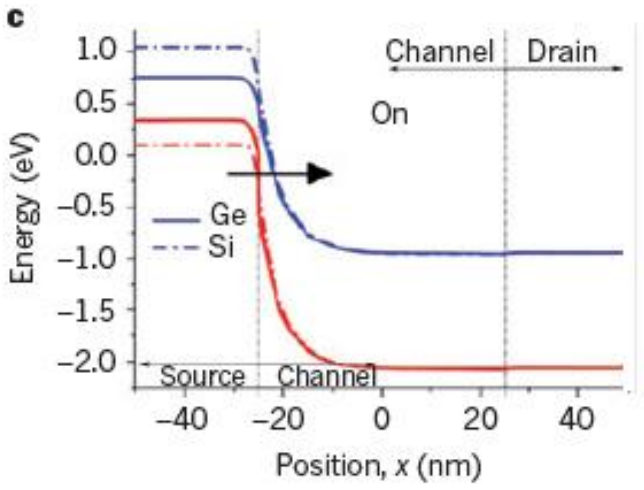
# nFET Implementation



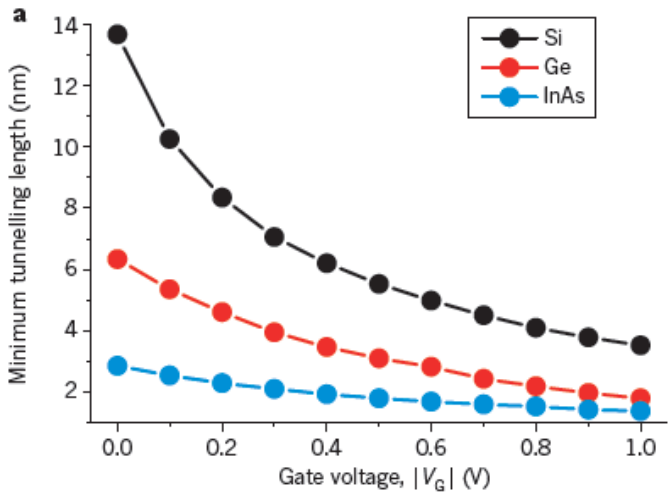

**nFET operation:**
Gate is used to lower the bands
In the gate region

**nFET booster:**
Use p++ Ge in the source



# Materials selection



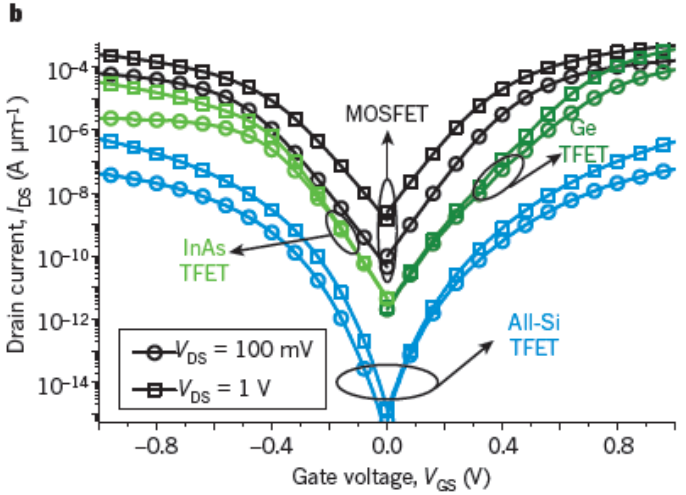




**Figure 4 | Importance of the material system on TFET performance.** **a**, Modulation of the minimum screening tunnelling length with the applied gate voltage in all-silicon (black), Ge-source (red) and InAs-source (blue) TFETs, showing the beneficial effect of a higher tunnelling rate due to the shorter tunnelling length in a heterostructure TFET with a low bandgap source material compared with silicon. By contrast, a higher ratio between the tunnelling length in the off and the on state reflects an improved $I_{ON}/I_{OFF}$. **b**, Corresponding transfer characteristics of a state-of-the-art 65-nm CMOS transistor (black), complementary Ge/InAs TFET (green) and complementary all-Si TFET (blue). The complementary Ge/InAs TFET achieves the best trade-off between a low $I_{OFF}$, a steep subthreshold swing and performance. $I_{DS}$, drain-to-source current; $V_{DS}$, drain-to-source voltage; $V_{GS}$, gate voltage at source.

**Important to reduce the tunneling barrier. Use narrow band gap material or heterostructure design.**

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^{\,3}}}{3q\hbar\,(E_g+\Delta\Phi)}\right)$$

NANO LETTERS
Letter
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# Sub 60 mV/decade Switch Using an InAs Nanowire–Si Heterojunction and Turn-on Voltage Shift with a Pulsed Doping Technique

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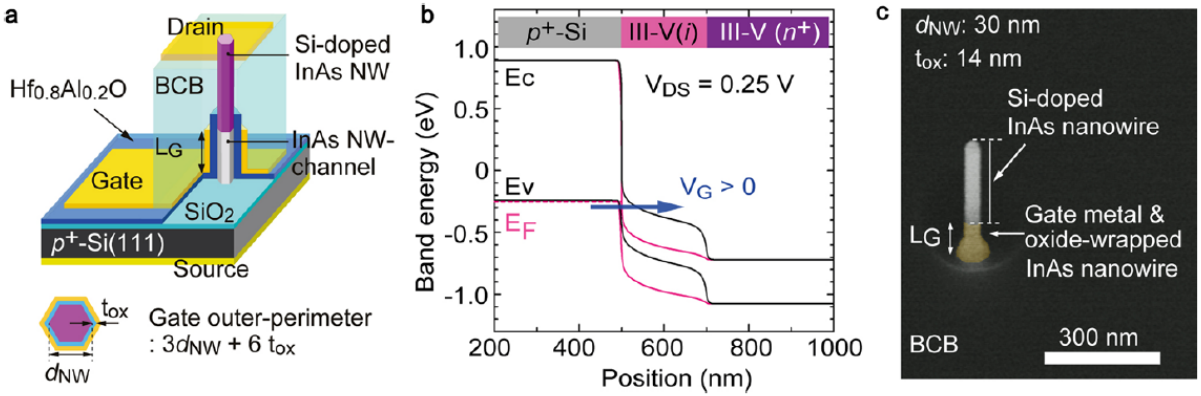



**Figure 1.** (a) Vertical transistor using InAs NW/Si heterojunction. Surrounding-gate configuration of InAs NW/Si heterojunction. Each InAs NW has a Si-doped InAs/undoped InAs stacked junction with a diameter of 30 nm. At the heterojunction, the diameter of the heterojunction is <30 nm because of isotropic wet etching of $SiO_2$. The NW is wrapped with $Hf_{0.8}Al_{0.2}$ gate oxide with a thickness of 14 nm and tungsten gate metal. The drain metal is a Ti/Al/Ti/Au multilayer. The gate length is 200 nm. The outer perimeter of the gate is 174 nm. (b) Band diagram simulated by using the one-dimensional Poisson–Schrödinger equation. Under $V_{DS} > 0$, positive $V_G$ induces Zener tunneling transport from *p*-Si to the III–V NW. (c) Representative SEM image showing the vertical transistor.

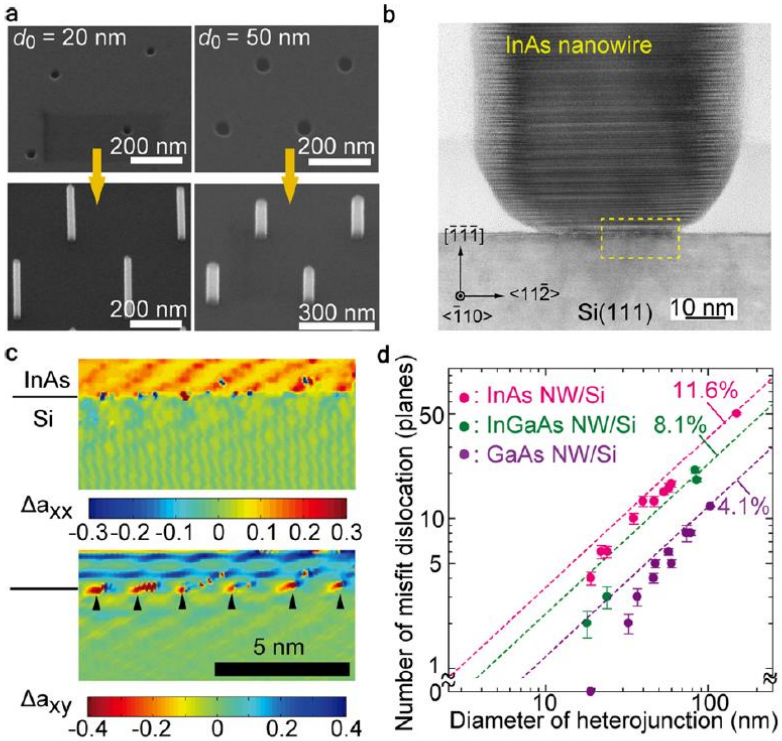



**Figure 2.** (a) Representative SEM images showing selective-area growth of vertical InAs NWs on Si. The NW has a hexagonal pillar shape surrounded by six-sided {−110} planes and a (111)B top surface. (b) Representative TEM image of the heterointerface of InAs NW/Si. The incidence of electron-beam is the <−110> direction. The heterojunction has atomically flat interface. (c) Displacement of latticeconstant for *xx*-direction ($\Delta a_{xx}$) and *xy*-direction ($\Delta a_{xy}$) mappings estimated from a filtered image of dashed squared part in panel b. *xx* is [−1−12] direction, and *xy* is [001] direction. (d) Numbers of misfit dislocation at III−V NW/Si heterojunction with a variation of diameter of heterointerface. Dashed lines are calculated values from the lattice mismatch. The close squares are the experimental data counted from the mapping and the TEM images.

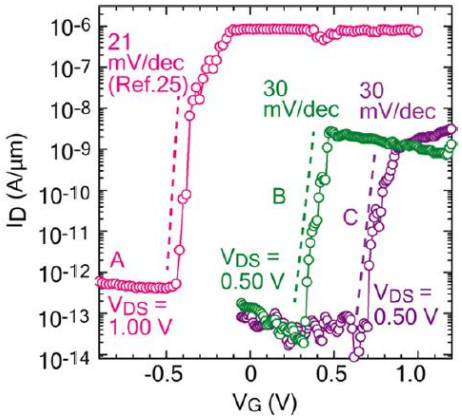



**Figure 3.** (a) Transfer characteristic of a steep-SS transistor using an InAs NW/Si heterojunction. The pink curve (A)[25] is the transfer characteristic of Figure 1 at $V_{DS}$ = 1.00 V. Curves labeled B (as green curve) and C (as purple curve) show the steep-SS characteristic at $V_{DS}$ = 0.50 V using an InAs NW/Si heterojunction with a Zn pulse doped InAs NW-channel segment with a 1 s pulse at 29 s intervals and Zn-pulse doped InAs NW-channel with a 2 s pulse at 28 s intervals.

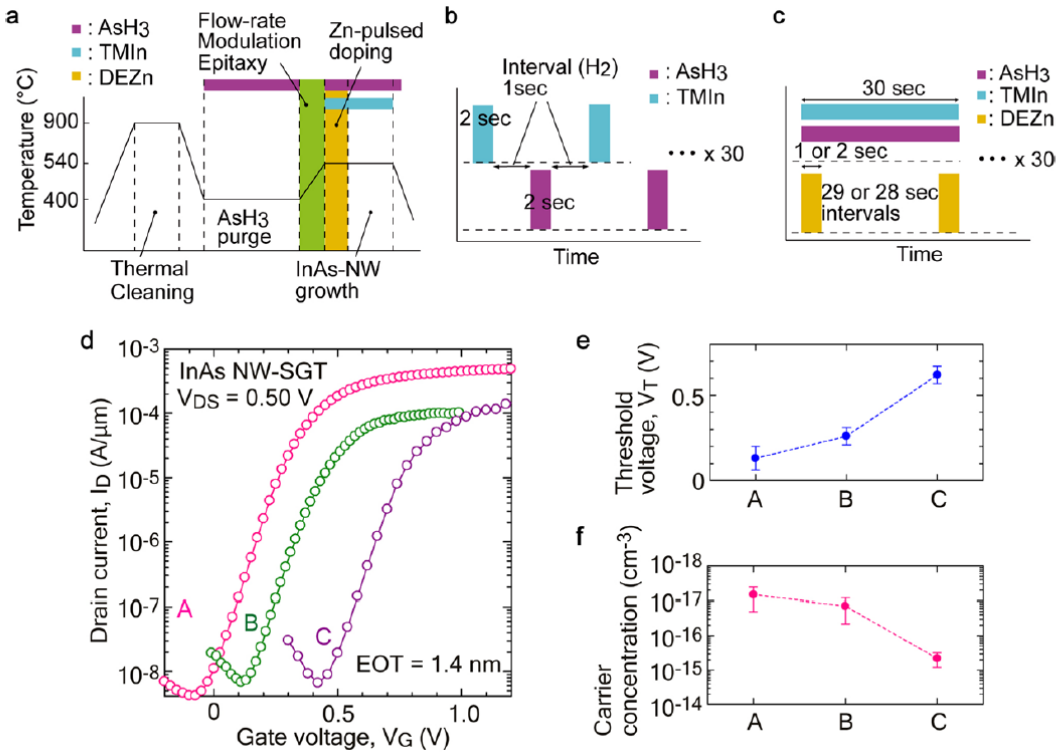



**Figure 4.** (a) Growth sequence for aligning vertical InAs NWs on Si with the Zn-pulse doping technique. (b) Schematic diagram of flow-rate modulation epitaxy. TMIn (2 s) and $AsH_3$ (2 s) are alternately supplied with an interval of $H_2$ (1 s). This sequence is repeated 30 times. (c) Diagram of Zn-pulse doping technique. DEZn (1 or 2 s) are alternately supplied with an interval of 29 or 28 s. This sequence is repeated six times to make pseudointrinsic InAs channel region. (d) The curve labeled A (pink plots) is the transfer characteristic of InAs NW-SGT with an undoped segment. Curves labeled B and C show transfer properties of InAs NW-SGTs with a Zn-pulse doped InAs NW-channel segment with a 1 s pulse with 29 s intervals (green plots) and with 2 s pulse with 28 s intervals (purple plots). (e) Variation of $V_T$ of an InAs NW vertical SGT with a different InAs NW-channel segment. (f) Variation of $N_D$ estimated from the $V_T$.

# Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs

Siyuranga O. Koswatta, Mark S. Lundstrom, *Fellow, IEEE*, and Dmitri E. Nikonov, *Senior Member, IEEE*

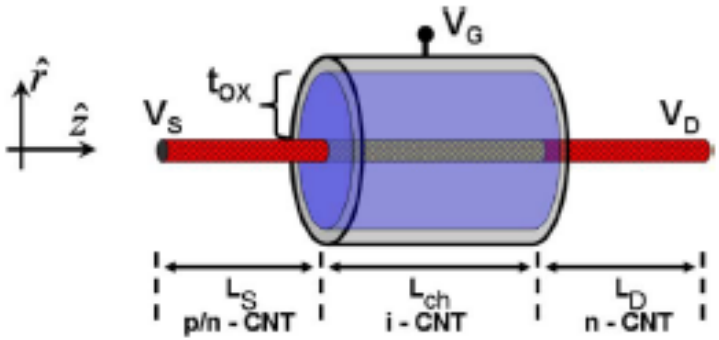
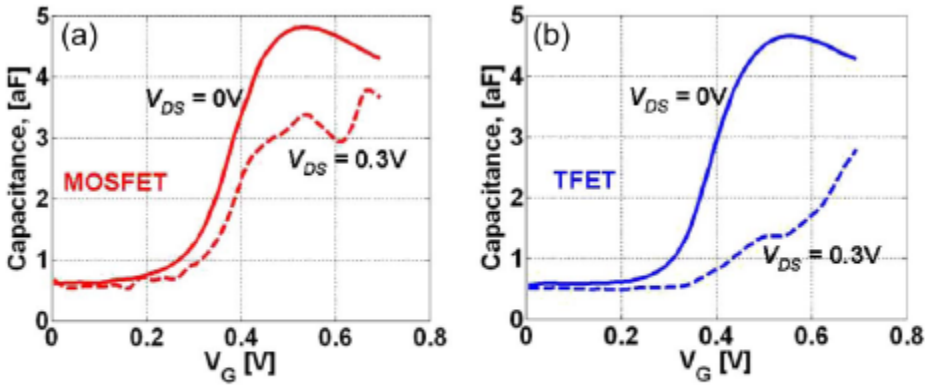



Fig. 1. Modeled device geometry used in this paper with cylindrically symmetric wrap-around gate electrode (see text for device parameters). The high-$k$ oxide is removed from source/drain regions in order to reduce the fringing fields that adversely affect the drive current for the p-i-n TFET.

Nanotube used for the modelling

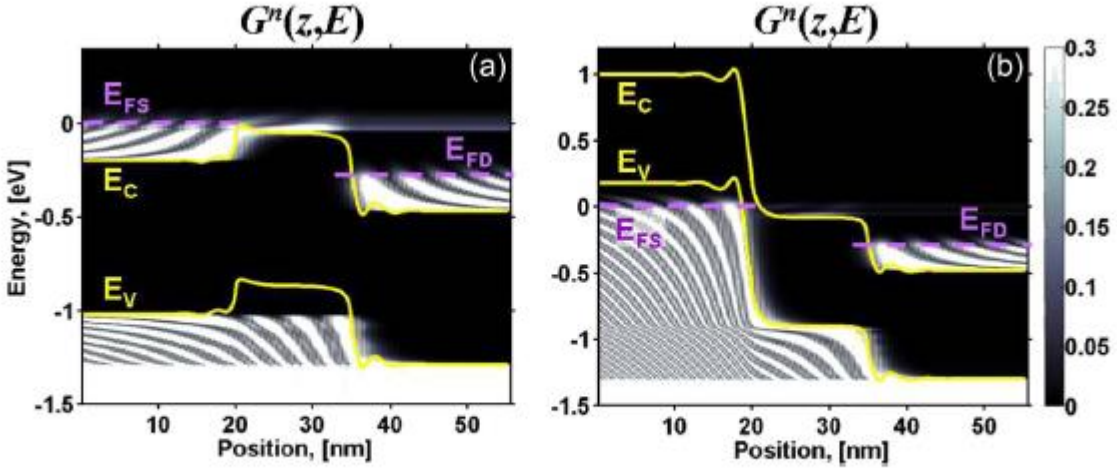
15 nm gate length

# Simulated Data




Reduced capacitance

Fig. 2. Total gate capacitance ($C_{\rm tot}$) versus $V_{\rm GS}$ comparison for (a) MOSFET and (b) TFET under dissipative transport. At small $V_{\rm DS}$, both devices show similar characteristics. However, at larger $V_{\rm DS}$, a fundamentally different behavior is observed; for the TFET device, capacitance remains small until larger gate biases are applied.




Less carriers in the channel

Fig. 3. Energy-position-resolved electron distribution [i.e., diagonal elements of $G^n$ in (5)] for (a) MOSFET and (b) TFET under ballistic transport at $V_{\rm GS} = 0.5$ V, $V_{\rm DS} = 0.3$ V. A significantly higher occupation of channel states is observed for the former.



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# Comparison MOSFETs and TFETs

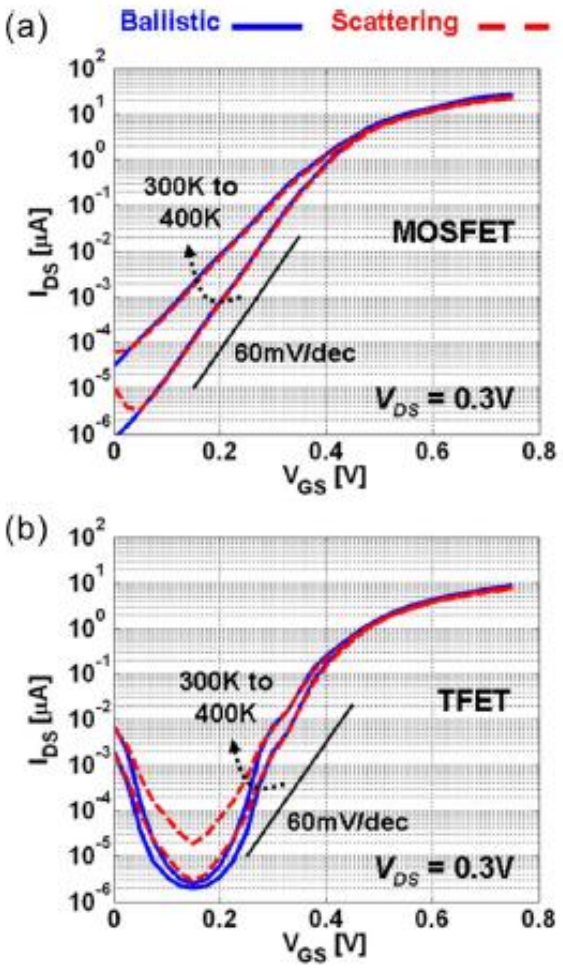



Fig. 5. $I_{DS}$–$V_{GS}$ dependence on temperature for (a) MOSFET and (b) TFET under ballistic and dissipative transport. The latter has reduced temperature dependence under ballistic conditions. Phonon-assisted tunneling can, however, degrade the subthreshold characteristics.

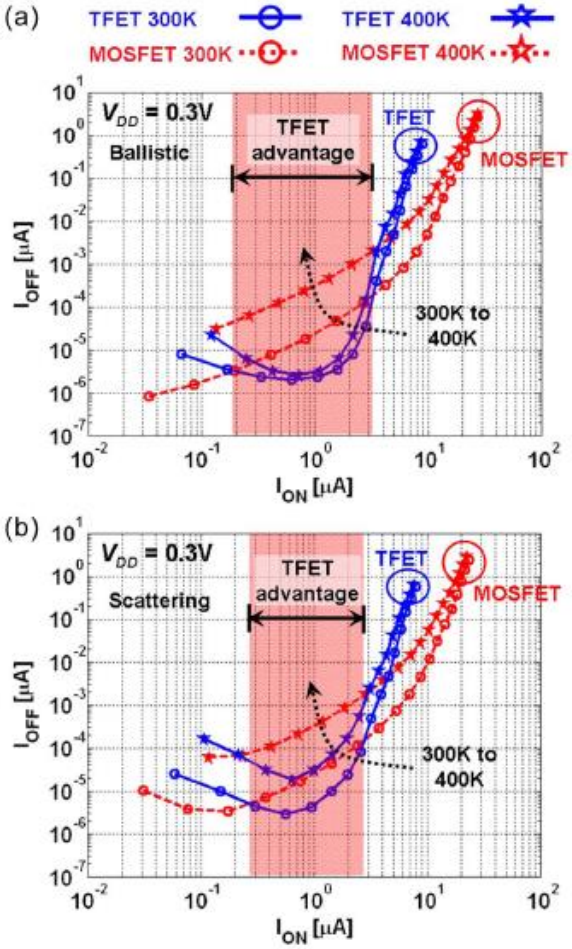
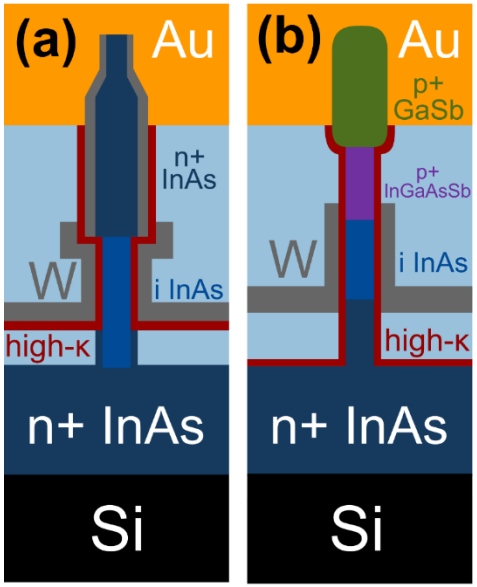
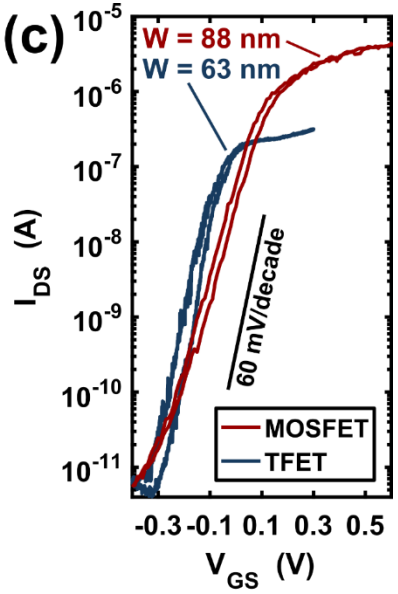



Fig. 6. $I_{OFF}$ versus $I_{ON}$ dependence on temperature at $V_{DD} = 0.3$ V under (a) ballistic and (b) dissipative transport. Shaded region is where the TFET has an advantage over the MOSFET due to larger $I_{ON}$ with a smaller $I_{OFF}$. Temperature dependence of $I_{OFF}$ for the TFET is also smaller than that for the latter.

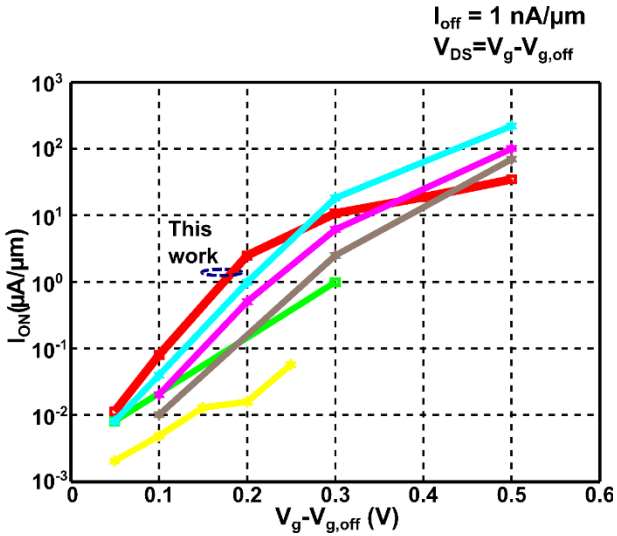
# TFET Characteristics




TFET:
- InGaAs [8]
- This work

MOSFET:
- InAs GAA NW [14]
- InGaAs 30 nm [13]
- Si SOI 22 nm [15]
- Si FinFET 16 nm [16]




## *TFET benefits*

- **Higher drive current at 0.2-0.3 V overdrive**
- **Option for power saving!**

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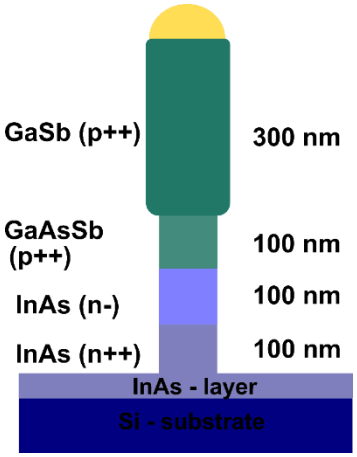
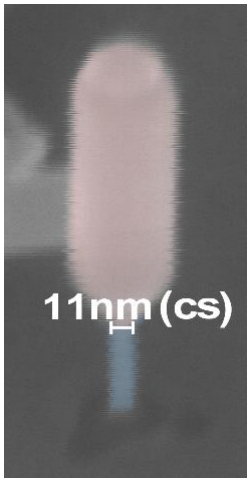
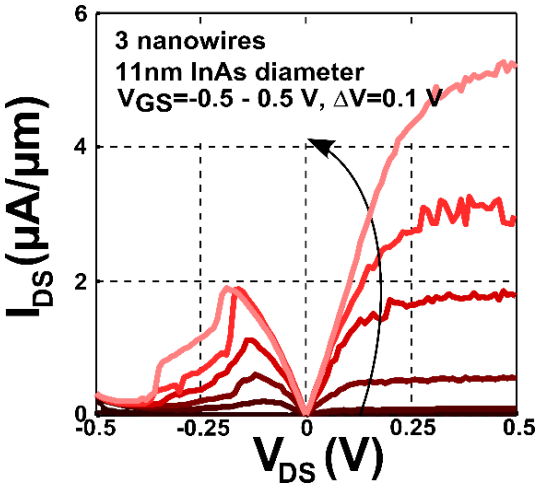
# TFET Process

- VLS growth combined with top-down processing
- Digital etching
  - ozone surface oxidation
  - citric acid oxide etching
- Diameter scaling down below 10 nm
- Typical diameter 20 nm
- No etching of GaSb is observed

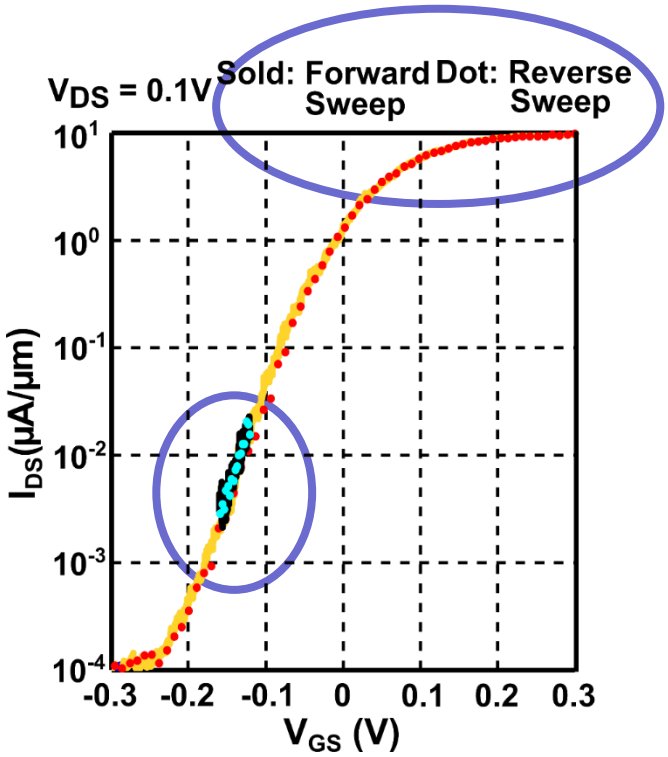


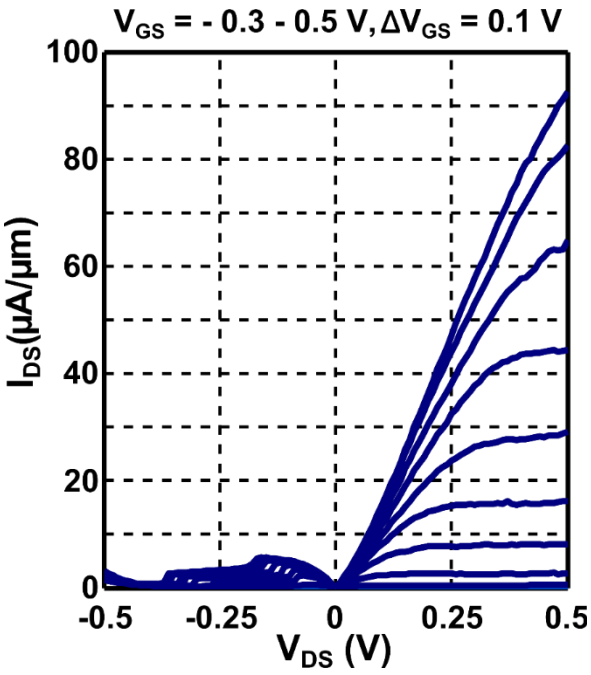
# Hysteresis/Measurement Reliability

- Sweep in forward and backward direction
- Using different voltage ranges
- Small hystersis of 5.4 mV
- Subthreshold swing independent of sweep direction and range



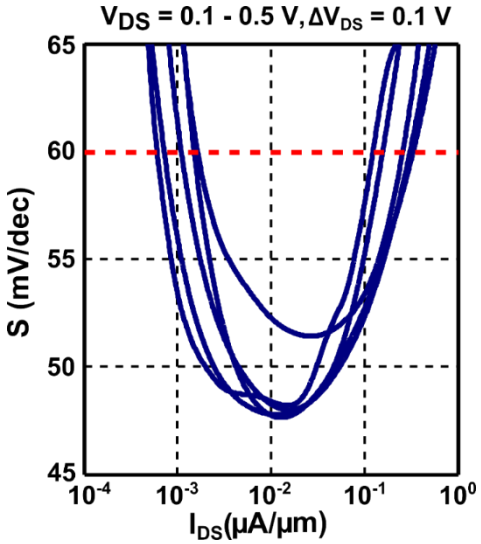
# Output Characteristics

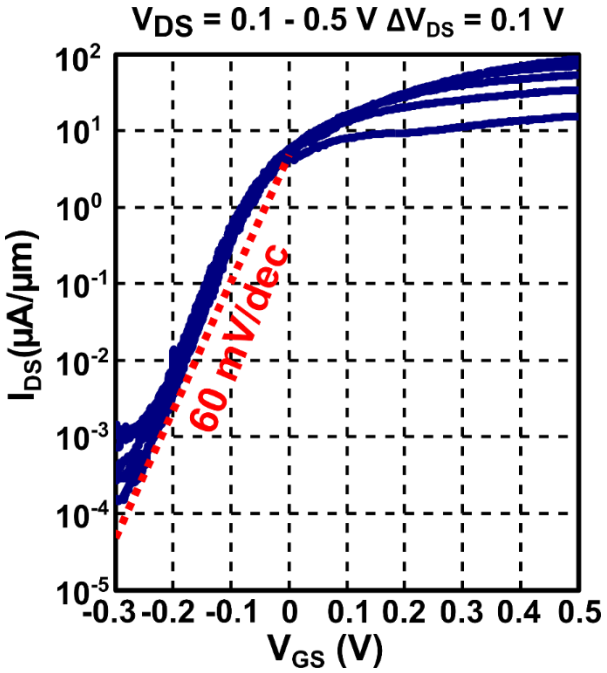
- **Strong NDR in reverse bias with PVR 14.8**
- **High quality junction**
- **$I_{DS}$= 92 µA/µm at $V_{DS}$= $V_{GS}$= 0.5 V**
- **Weak superlinear behaviour**



# Transfer Characteristics

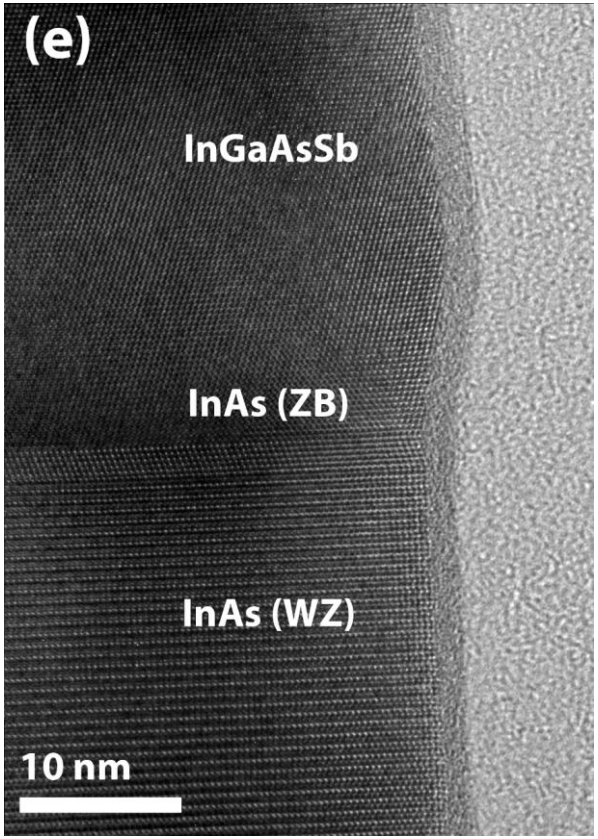
- **Sub 60 mV/decade operation at $I_{DS}$ ~ 1-300 nA/µm**
- **Good electrostatic control (DIBL 25 mV/V), 5 mV Hysteresis**
- **Gate-current <$I_{DS}$/100**
- **$S_{min}$ = 48 mV/dec at 0.3 V**
- **$I_{60}$= 0.31 µA/µm at 0.3 V**

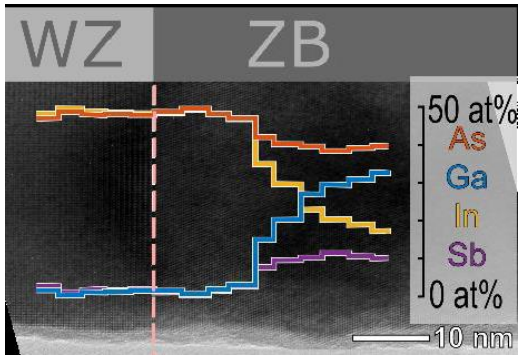


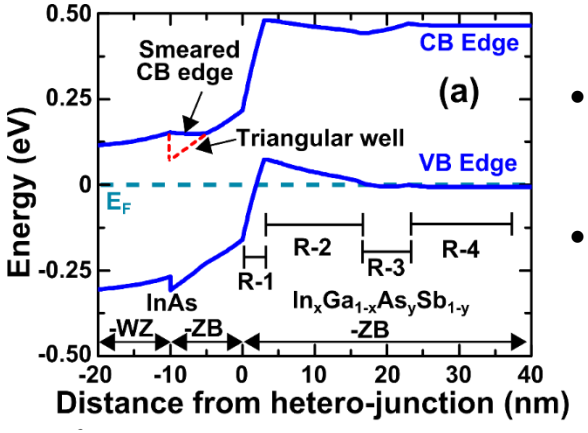




*E. Memisevic et al., IEDM 2016*

# Materials Characterization



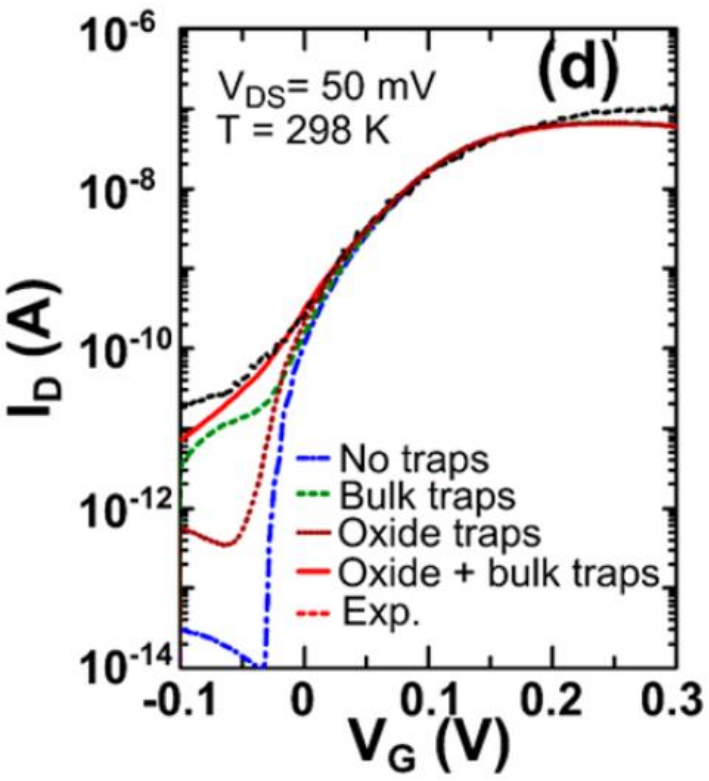




- **Nanowire with WZ-ZB InAs transition**
- **Slowly varying composition gradient with transition over about 20 nm**
- **Strong strain field within heterostructure (2-3%)**
- **28% Sb in InGaAsSb**

*E. Memisevic et al., Nano Lett 2017*

# Where are the Defects?

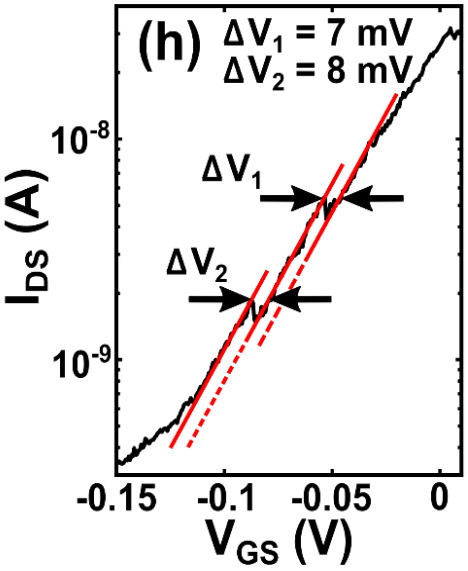


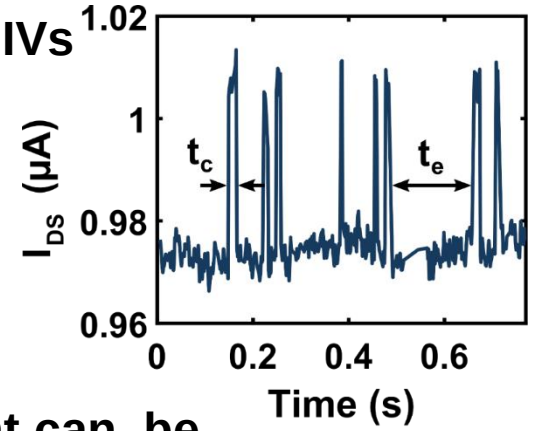

- **Excellent fit by TCAD modeling (ETH)**
- **Bulk trap main contribution to leakage current**
- **Oxide traps have vanishing influence besides electrostatic effect**

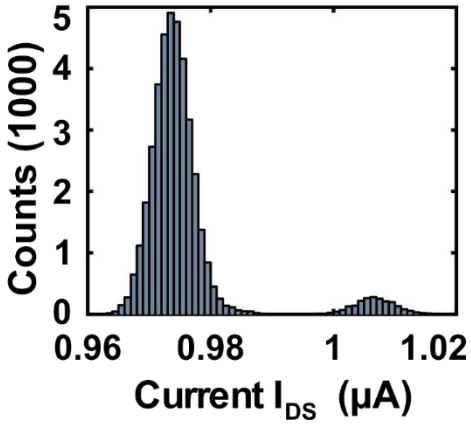
*E. Memisevic et al.,*
*Nano Lett 2017*

# Defects within the Oxide

**Multiple jumps detected in some IVs**



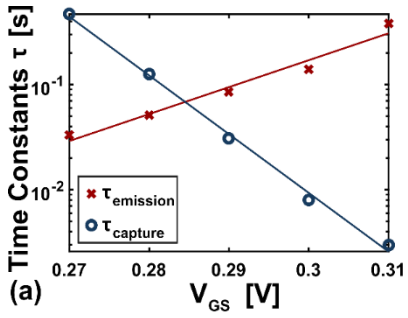



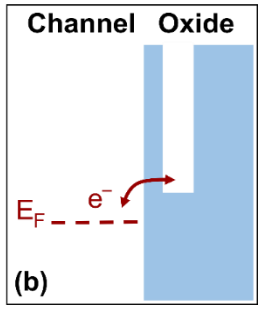




**Each event can be viewed as RTN**

**Time constants fit with model of defects within oxide**

$$\tau_{c/e} = \tau_0 \, exp(z/\lambda)$$




*E. Memisevic et al., Nano Letters 2017*
*M. Hellenbrand et al ESSDERC 2017*