Contents: Power and Delay

CMOS Static and Dynamic Power Consumption:
J Rabaey et al ”Digital Integrated Circutis”

Integration of III/V HEMTs on Si :
S Datta et al IEEE Electron Dev. Lett. 28, 2007 p 685 ” Ultrahigh-Speed 0.5 V Supply ...”

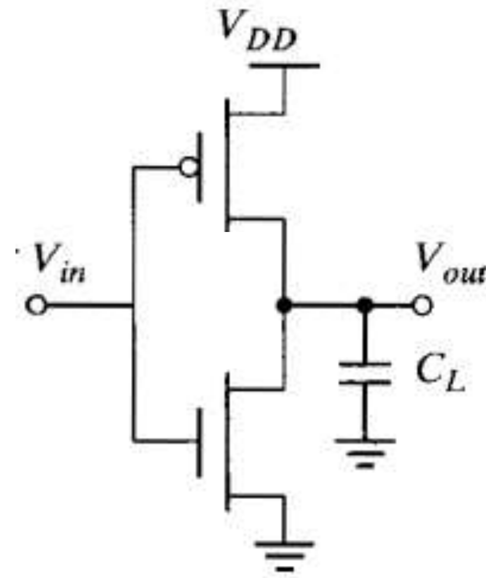
HEMTS for Beyond-CMOS:
D-H Kim et al IEEE Trans. Electron Dev. 54, 2007 p 2606 ” Logic Suitability of 50 nm ...”

CMOS Dynamic and Static Power Consumption

Advantages with CMOS:

Full logic swing
High noise margin
Superior robustness
Low steady state power consumption

Robust low-power digital technology



V_{out}=V_{in} for next stage
C_L both parasitics and gate capacitance

Dynamic Power Consumption

Advantages with CMOS:

Full logic swing
High noise margin
Superior robustness
Absence of steady state power consumption

Calculate the charging energy during one switching event!

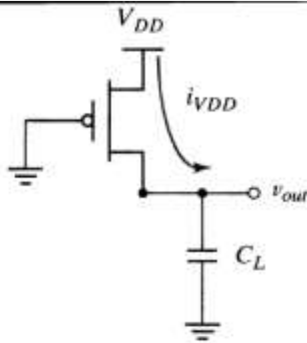


Figure 5-25 Equivalent circuit during the low-to-high transition.

Calculate the charging energy:

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t) V_{DD}\, dt = V_{DD} \int_0^{\infty} C_L \frac{dv_{out}}{dt}\, dt = C_L V_{DD} \int_0^{VDD} dv_{out} = C_L V_{DD}^2$$

Calculate the stored energy:

$$E_C = \int_0^{\infty} i_{VDD}(t) v_{out}\, dt = \int_0^{\infty} C_L \frac{dv_{out}}{dt} v_{out}\, dt = C_L \int_0^{VDD} v_{out}\, dv_{out} = \frac{C_L V_{DD}^2}{2}$$

Dynamic Power Consumption

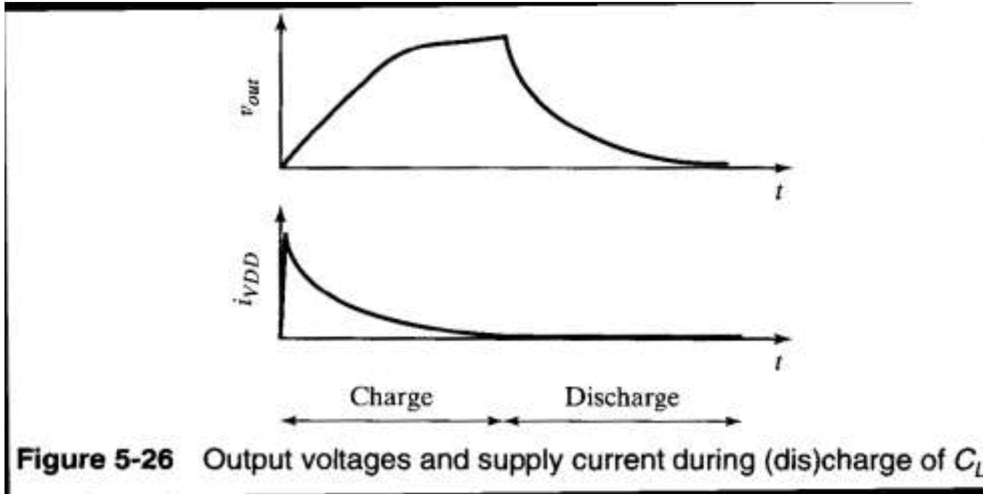


Figure 5-26 Output voltages and supply current during (dis)charge of C_L.

During charging (low-to-high transition) half energy is stored on capacitor, half energy is dissipated in the transistor

During discharging (high-to-low transition) half energy is stored on capacitor, the stored energy (half energy) is dissipated in the transistor

$$P_{dyn} = C_L V_{DD}^2 f_{0->1}$$

Example: 50 nm CMOS
f=2 GHz C_L=3 fF/gate
V_{DD}=1.0 V
P_{dyn}=6 μW

Note: Not all transistors active!
(effectively reduces frequency)
Voltage scaling reduces P_{dyn}
Scaling reduces gate capacitance, but increases parasitic capacitance!

Direct-Path Current Power Consumption

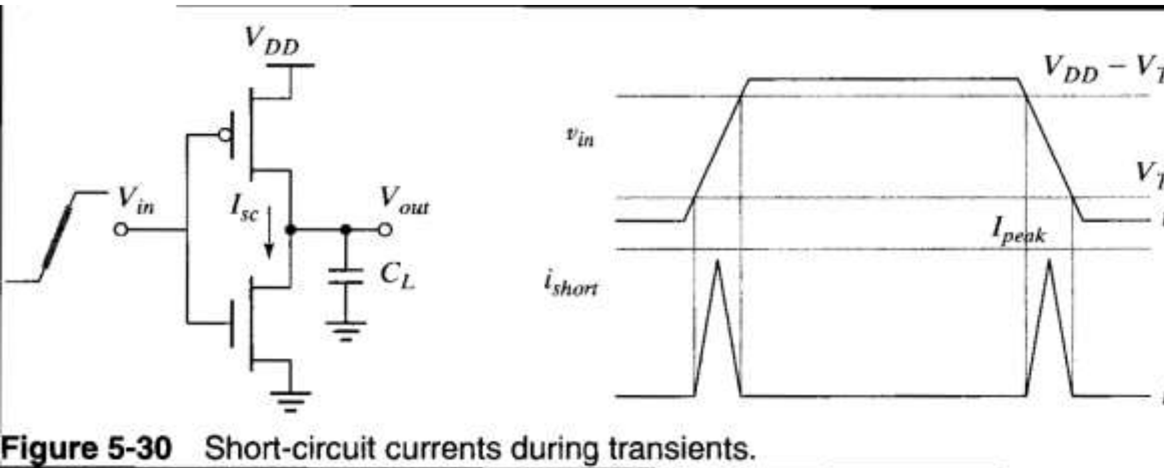


Figure 5-30 Short-circuit currents during transients.

During the finite time switching, a direct current is flowing in the transistor pair

Assume triangular current peaks

$$E_{dp} = V_{DD} \frac{I_{peak} t_{sc}}{2} + V_{DD} \frac{I_{peak} t_{sc}}{2} = t_{sc} V_{DD} I_{peak}$$

$$P_{dp} = t_{sc} V_{DD} I_{peak} f = C_{sc} V_{DD}^2 f$$

This is typically a minor part of the power consumption

Static Power Consumption: Drain Leakage

Leakage current typically 10-100 pA/μm^2. Drain area 50 nm^2 and 1 billion gates with V_{DD}=1.0 V gives 0.5 μW.

$$P_{stat} = I_{stat} V_{DD}$$

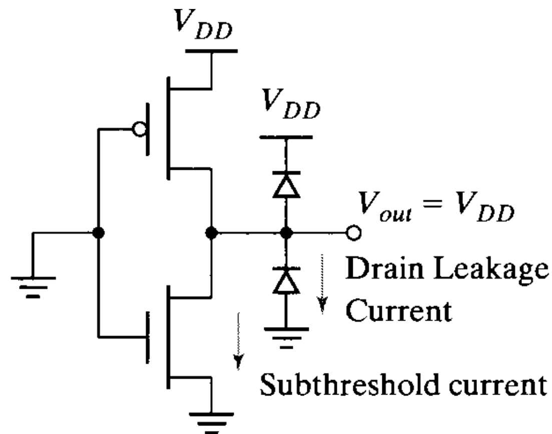


Figure 5-34 Sources of leakage currents in CMOS inverter (for V_{in} = 0 V).

Solution:
Use NWs to reduce channel leakage
Use SOI technology to reduce contact leakage

Static Power Consumption: Subthreshold Leakage

As the drive voltage is reduced, the threshold voltage should also be scaled (recall $V_t \sim V_{DD}/3$!). This implies that the subthreshold current is substantially increased.

Consider a 50 nm NMOS transistor with SS of 60 mV/dec. and V_t=0.4 V. At V_{GS}=0 V it consumes about 10^{-12} A. Reducing the threshold to 0.2 V increased the current a factor 300! In a 1 billion transistor operating at 1 V, we get a power consumption of $10^9 \times 300 \times 10^{-12} \times 1.0$=300 mW!

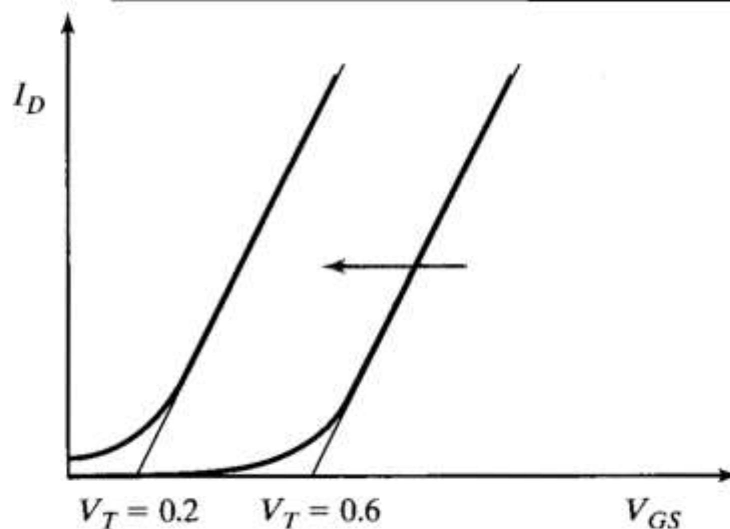


Figure 5-35 Decreasing the threshold increases the subthreshold current at $V_{GS} = 0$.

Threshold voltage key parameter to balance on- and off-state

Fundamental transistor problem!

Put It All Together!

Dynamic
during switching

Direct
during switching

Total leakage
current

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = \left(C_L V_{DD}^2 + V_{DD} I_{peak} t_s \right) f_{0->1} + V_{DD} I_{leak}$$

Typically dominant

Can be reduced

Will be more important
in scaled technologies

The Power-Delay Product

Introduce the power-delay product
as a quality measure of a logic gate:

$$PDP = P_{av} t_p$$

If the gate is switched at full speed, the PDP corresponds
To the average energy consumed per switching event
(0->1 or 1->0 transition)

$$PDP = C_L V_{DD}^2 f_{\max} t_p = \frac{C_L V_{DD}^2}{2}$$

Better, The Energy-Delay Product

Introduce the energy-delay product, which balances the performance and energy consumption!

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$

t_p is the propagation delay (gate delay) and $f_{max} = 1/(2t_p)$

Voltage Dependence on EDP!!!

$$EDP = PDP \times t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$

$$t_p \approx \frac{\alpha C_L V_{DD}}{(V_{DD} - V_T)^2}$$

$$EDP = \frac{\alpha C_L^2 V_{DD}^3}{2(V_{DD} - V_T)^2}$$

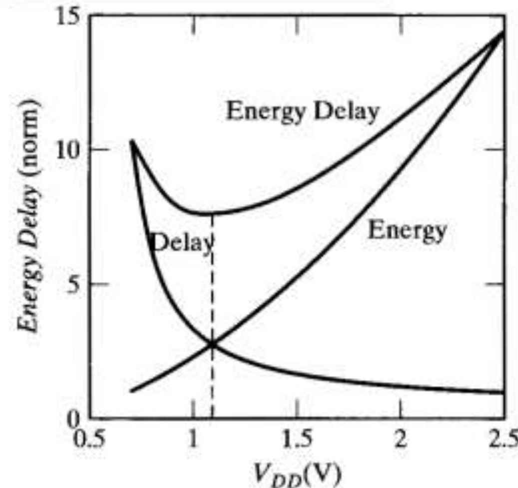


Figure 5-36 Normalized delay, energy, and energy-delay plots for CMOS inverter in 0.25-μm CMOS technology.

Increase V_d:

Speed improves (higher current)
Energy increases (more charge)
Optimum!

Extra (model validation):

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = \ln 2 \times C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

RC-time constant during switching

$$t_{pHL} = \ln 2 \times \frac{3}{4} \frac{C_L V_{DD}}{(W/L)_n \left(\mu_n \varepsilon_{ox} / t_{ox}\right)\left(V_{DD} - V_{Tp}\right)^2}$$

Use transistor equations to derive the effective transistor resistance

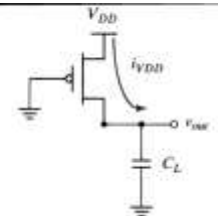


Figure 5-25 Equivalent circuit during the low-to-high transition.

Nanoelectronics: Power and Delay

IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 8, AUGUST 2007 685

Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate

Suman Datta, *Senior Member, IEEE*, G. Dewey, J. M. Fastenau, *Member, IEEE*, M. K. Hudait, D. Loubychev, W. K. Liu, *Senior Member, IEEE*, M. Radosavljevic, W. Rachmady, and R. Chau, *Fellow, IEEE*

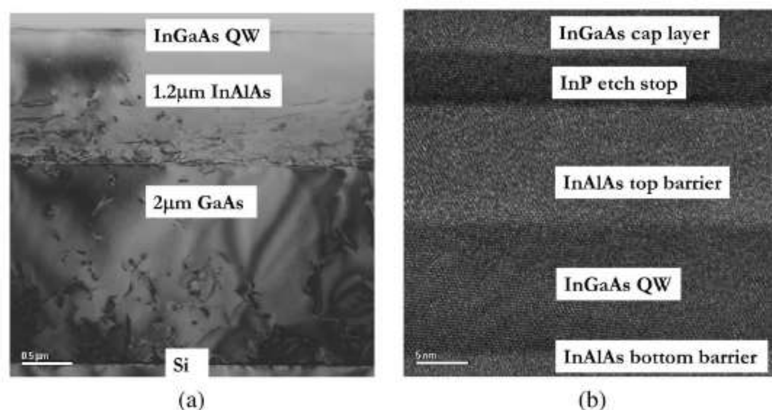


Fig. 1. Cross-sectional TEM images of $In_{0.7}Ga_{0.3}As$ QW structures on Si using metamorphic buffer architecture: (a) Entire layer structure. (b) magnification of $In_{0.7}Ga_{0.3}As$ QW along with bottom and top barrier layers. The misfit dislocations are predominantly contained in the buffer layer.

- buffer layer techniques are available
- comparable mobility

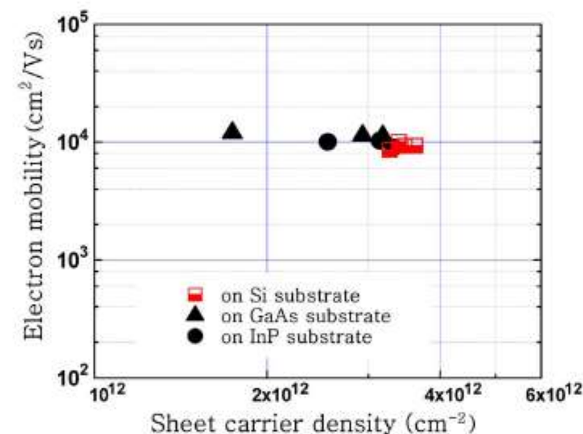


Fig. 2. Electron mobility versus sheet carrier density in n-channel $In_{0.7}Ga_{0.3}As$ QW device layers grown on Si, GaAs, and InP substrates. In all cases, $In_{0.52}Al_{0.48}As$ is the bottom and top barrier layer.

Comparable RF-data!

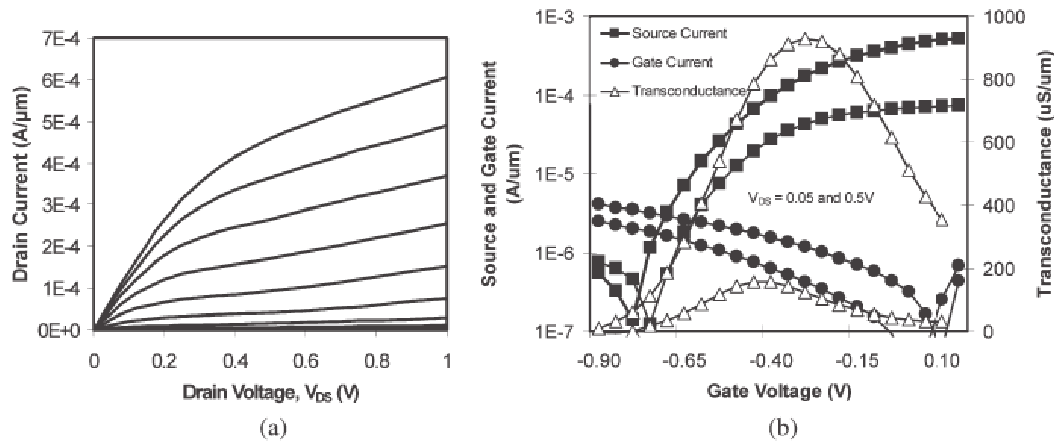


Fig. 3. (a) Output characteristic for 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistor on 3.2-μm metamorphic buffer on silicon (gate voltage V_G is swept from 0.0 to −0.8 V in −0.1-V steps). (b) Transfer characteristic for 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistor on 3.2-μm buffer on silicon with $V_{DS} = 0.5$ and 0.05 V. Peak transconductance g_m for this device was 930 $\mu S/\mu m$ at $V_{DS} = 0.5$ V.

- well behaved IV characteristics!
- good DC numbers at 80 nm Lg
- comparable RF data to lattice matched devices

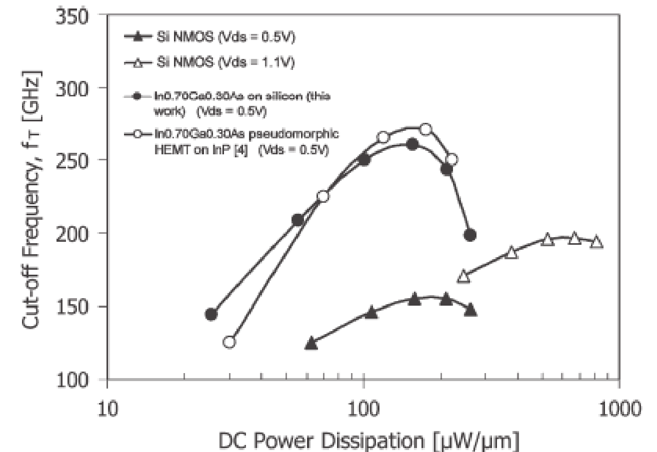


Fig. 4. Plot of deembedded unity gain cutoff frequency as a function of dc power dissipation for 0.5-V V_{DS} 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistors on both silicon and InP substrates, benchmarked against 60-nm L_g silicon NMOS transistors at $V_{DS} = 0.5$ and 1.1 V.

Logic Suitability of 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs for Beyond-CMOS Applications

Dae-Hyun Kim, Jesús A. del Alamo, Jae-Hak Lee, and Kwang-Seok Seo

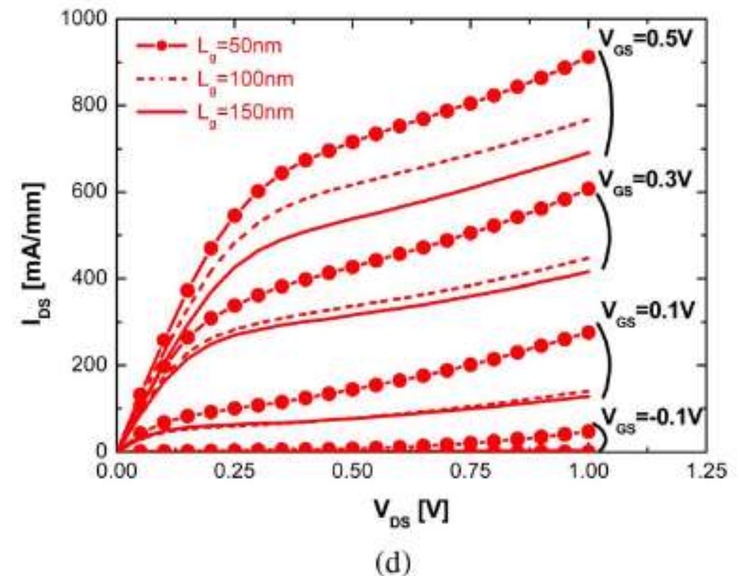
Layer	Material	Thickness
n+ Cap	InGaAs, x = 0.53	20 nm
Stopper	InP	6 nm
Barrier	InAlAs, x = 0.52	8 nm
δ-doping	Si	-
Spacer	InAlAs, x = 0.52	3 nm
Channel	InGaAs, x = 0.53	3 nm
	InGaAs, x = 0.7	8 nm
	InGaAs, x = 0.53	4 nm
Buffer	InAlAs, x = 0.52	500 nm
3 Inch S. I. InP Substrate		

Fig. 1. Epitaxial layer structure of the $In_{0.7}Ga_{0.3}As$ HEMTs that are fabricated in this paper.

TABLE I
DETAILED GATE STRUCTURAL INFORMATION FOR FOUR TYPES OF $In_{0.7}Ga_{0.3}As$ HEMTs THAT ARE FABRICATED IN THIS PAPER

	Type-A	Type-B	Type-C	Type-D
Barrier	$InP/In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$	$In_{0.52}Al_{0.48}As$
Stack	Ti/Pt/Au	Ti/Pt/Au	Pt/Ti/Mo/Au	Buried-Pt/Ti/Mo/Au
t_{ins} [nm]	17	11	11	7
Φ_B [eV]	~ 0.4	~ 0.6	~ 0.7	~ 0.8

- 4 types of transistors
- Schottky barrier and insulator thickness
- good DC characteristics
- weak scaling with gate length



(d)

Scaling with Schottky barrier and insulator thickness

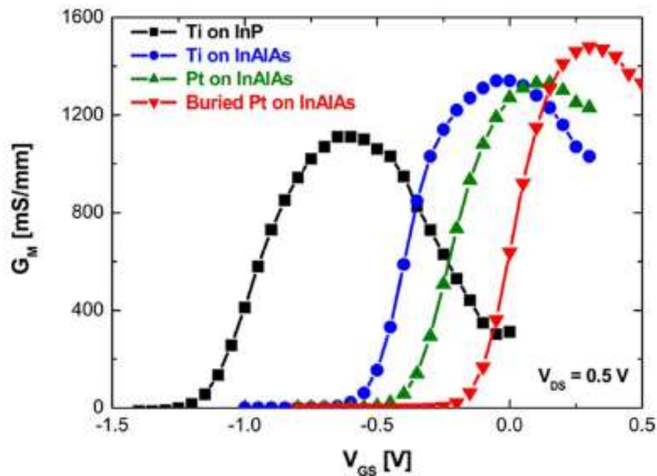


Fig. 5. Transconductance (G_m) characteristics of all 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs at $V_{DS} = 0.5$ V.

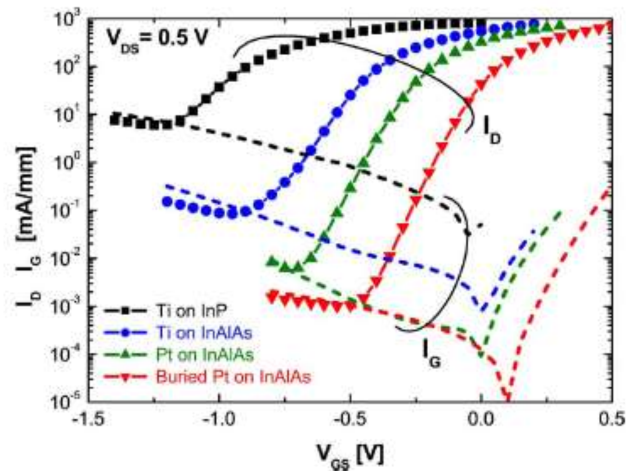


Fig. 6. Semilog plot of I_D and I_G of all 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs at $V_{DS} = 0.5$ V.

- Tight control needed to improve the performance

TABLE II
SUMMARY OF LOGIC FIGURES OF MERIT FOR FOUR TYPES OF 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs

	V_T [V]	DIBL [mV/V]	S [mV/dec]	I_{ON}/I_{OFF}
Type-A	-1.10	300	200	63
Type-B	-0.65	220	130	1×10^3
Type-C	-0.55	180	100	7.2×10^3
Type-D	-0.20	160	86	1.7×10^4

Improved speed and/or reduced power consumption

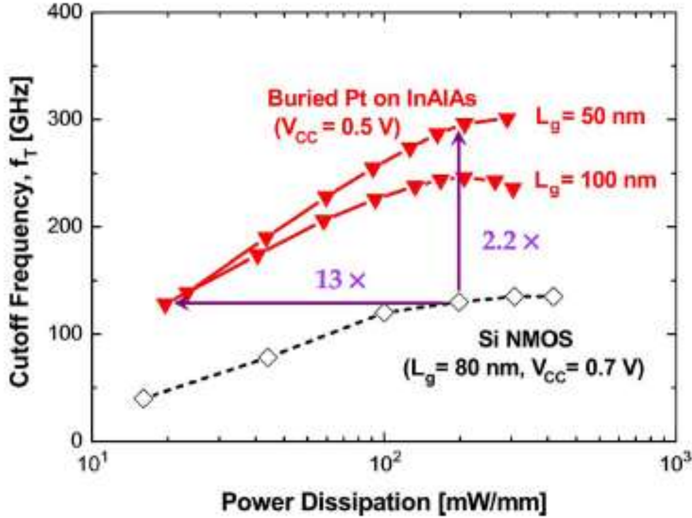


Fig. 11. Cutoff frequency (f_T) of our 50- and 100-nm type D $In_{0.7}Ga_{0.3}As$ HEMTs and 80-nm Si MOSFETs as a function of the dc power dissipation.

- Depending on bias condition benefits can be found in the areas of speed and/or power dissipation

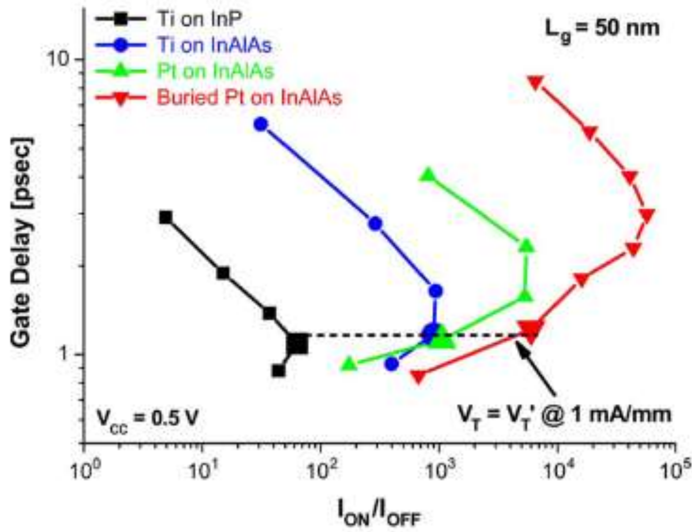


Fig. 14. Gate delay (CV/I) of all 50-nm $In_{0.7}Ga_{0.3}As$ as a function of I_{ON}/I_{OFF}.

- Well selected technology is required to maximize Ion/Ioff ratio

22FFL: A High Performance and Ultra Low Power FinFET Technology for Mobile and RF Applications

B. Sell, B. Bigwood, S. Cha, Z. Chen, P. Dhage, P. Fan, M. Giraud-Carrier, A. Kar, E. Karl, C.-J. Ku, R. Kumar, T. Lajoie, H.-J. Lee, G. Liu, S. Liu, Y. Ma, S. Mudanai, L. Nguyen, L. Paulson, K. Phoa, K. Pierce, A. Roy, R. Russell, J. Sandford, J. Stoeger, N. Stojanovic, A. Sultana, J. Waldemer, J. Wan, W. Xu, D. Young*, J. Zhang, Y. Zhang and P. Bai

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	High Performance Logic Transistor			Low Power Logic Transistor			Ultra Low Power Logic Transistor	Analog Transistor			High Voltage Transistor		
Device	ULVT	LVT	LPLVT	HP	Nom	LP	LL	AL	AL	AL	TGLV	TGMV	TGHV
VDD [Volt]	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	1.2	1.5	1.8
Gate Pitch [nm]	108	108	108	108	108	108	144	144	216	270	216	216	270
Fin Pitch [nm]	45	45	45	45	45	45	45	45	45	45	45	45	45
Tox	Thin	Thin	Thin	Thin	Thin	Thin	Thick	Thin	Thin	Thin	Thick	Thick	Thick
Performance Metric	NMOS/PMOS Idsat/Ioff [mA/um]							GM*Rout			NMOS/PMOS Idsat [mA/um]		
Value	1.24/1.22 @ 0.7V, 10nA/um			0.81/0.81 @ 0.7V, 100pA/um			0.10/0.10 @ 0.7V, 1pA/um	47	54	60	0.77/ 0.61	1.01/ 0.87	1.11/ 1.02

Table 1. Transistor design rules and electrical characteristics for logic, analog and high voltage transistors developed for 22FFL.

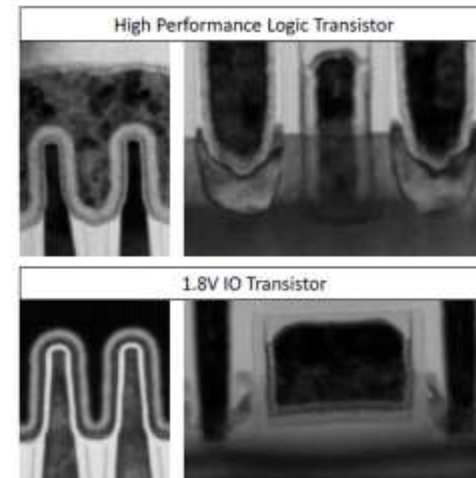

Fig. 1. Fin and gate cut TEMs of logic and 1.8V IO transistors.

22FFL: A High Performance and Ultra Low Power FinFET Technology for Mobile and RF Applications

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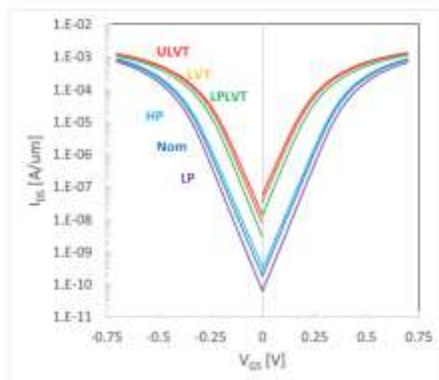

Fig. 5. I_{DS}-V_{GS} curves demonstrating low subthreshold slope and DIBL for all logic devices.

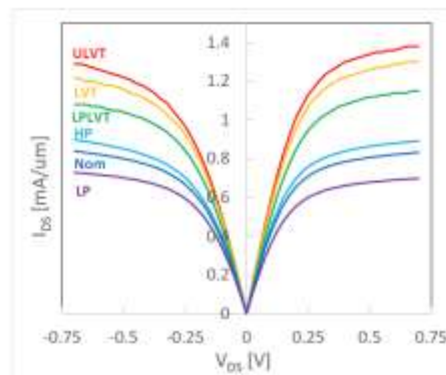

Fig. 6 Balanced I_{DS}-V_{DS} characteristics for all logic transistors.

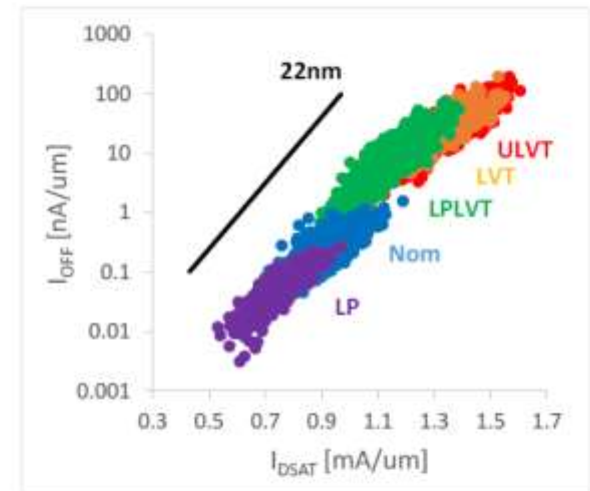

Fig. 3. NMOS I_{Dsat} vs. I_{off} showing 57% gain over 22nm HP transistors presented in [1].

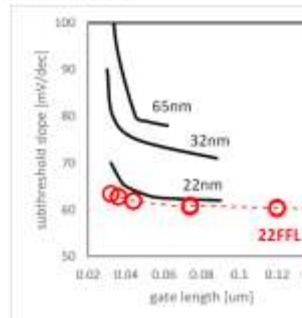

Fig. 7. Channel length dependence of thin subthreshold slope compared to previo technologies.

Improved speed and/or reduced power consumption

Intel 22nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology

H.-J. Lee, S. Rami, S. Ravikumar, V. Neeli, K. Phoa, B. Sell, and Y. Zhang
Logic Technology Development, Intel Corporation, Hillsboro, Oregon, USA, email: hyung-jin.lee@intel.com

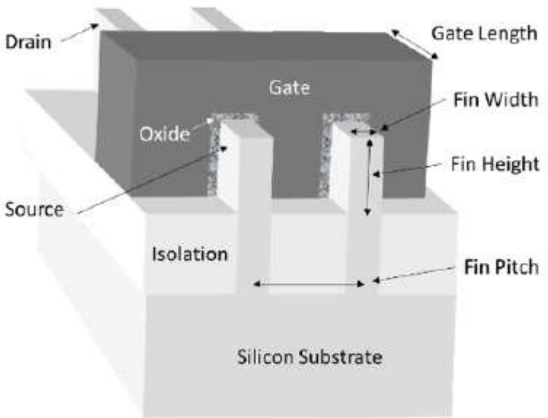

Figure 1: 3D view of FinFET device structure

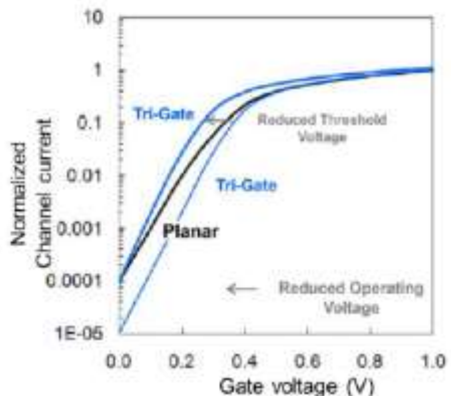

Figure 2: I-V curves of FinFET and Planar demonstrating DIBL improvement by FinFET technologies

- Tri-gates optimized for RF-operation

Parasitics are Limiting Performance at Scaled Nodes

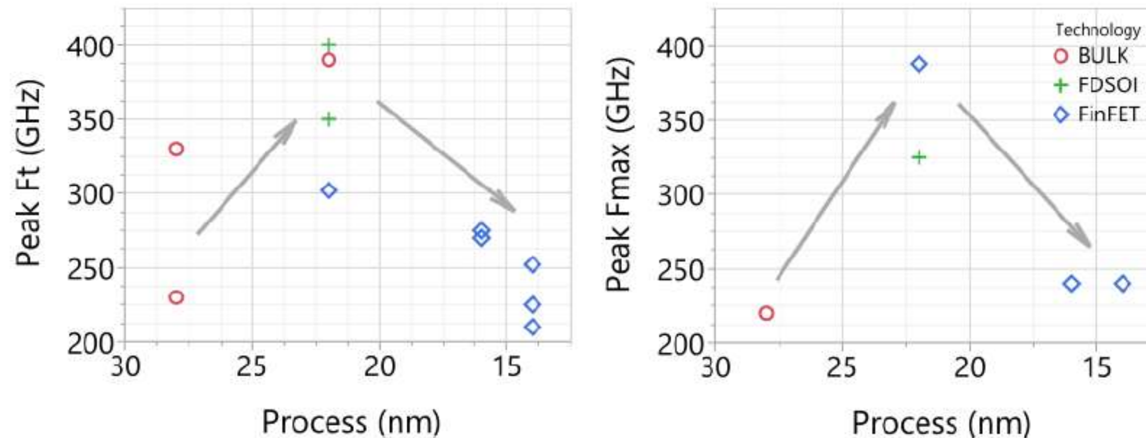

Figure 5: f_t and f_{max} trends by process node: both ft and fmax reach the peak performance around 20 ~ 25nm due to the excessive parasitic capacitance by high density interconnect

- Currently best performance is obtained at about 20 nm node!

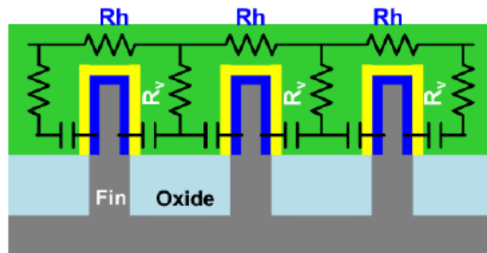

Figure 3: FinFET gate resistance structure: Horizontal resistance (R_h) and Vertical resistance (R_v) surrounding fin structures

- Parasitics are related to gate resistance and capacitances (lack of space)