Lecture 2: Scaled CMOS

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Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications

Robert Chau, *Fellow, IEEE*, Suman Datta, *Member, IEEE*, Mark Doczy, Brian Doyle, Ben Jin, Jack Kavalieros, Amlan Majumdar, Matthew Metz, and Marko Radosavljevic

Transistor evolution:

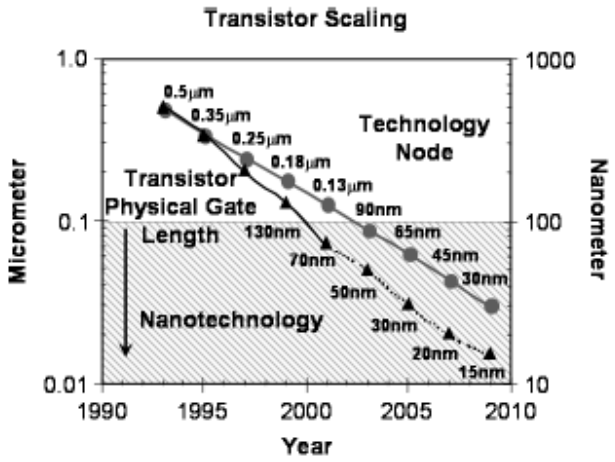


Fig. 1. Scaling of transistor size (physical gate length) with technology node to sustain Moore's Law. Nodes with feature size less than 100 nm can be referred to as nanotechnology. By 2011, the gate length is expected to be at or below 10 nm. Transistor scaling will be enabled by integration of emerging nanotechnology options on to the Si platform.

Four key metrics for logics:

Speed
Intrinsic speed (CV/I)

Switching energy
Energy-delay product ($CV/I*CV^2$)

Scalability
Subthreshold slope vs L_g

Off-state leakage
CV/I vs I_{on}/I_{off}

Method for benchmarking

Typical nanotube characteristics:

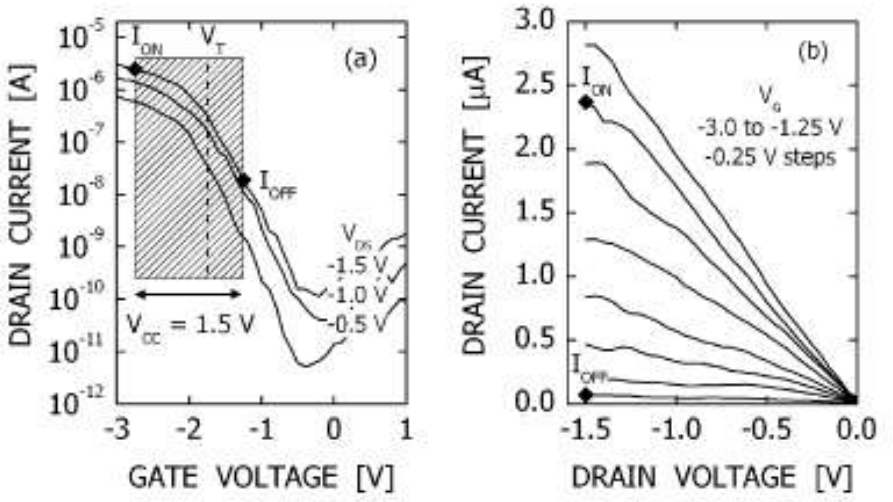


Fig. 3. Example (a) I_D–V_G and (b) I_D–V_{DS} characteristics of a CNT FET illustrating our benchmarking procedure. The V_{CC} choice is made by selecting the highest available V_{DS}, which, in this example, is 1.5 V. The shaded box in (a) is anchored around $V_G = V_T$, as discussed in the text. The width of the box denotes the V_G swing of 1.5 V, which is consistent with the V_{CC} choice. The values of I_{ON} and I_{OFF} are shown as black diamonds in both (a) and (b).

Definition of data points:

$|V_{DS}|=V_{CC}$

V_g 2/3 above V_t gives I_{on}
V_g 1/3 below V_t gives I_{off}
Calculate/measure the capacitance

Cylindrical devices:

$$C_{TOTAL}^{-1} = C_{OX}^{-1} + C_{QM}^{-1}$$

$$C_{OX} = 2\pi\varepsilon_0\varepsilon_r / \ln(2h/R)$$

Normalization by width $2\pi R$

Gate Delay

NMOS:

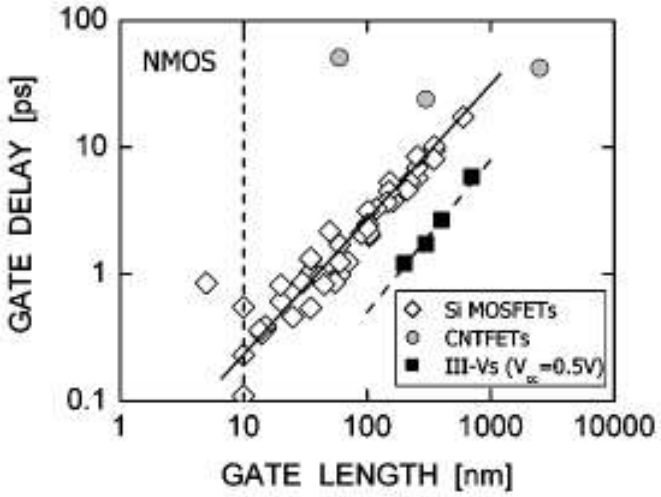


Fig. 5. Gate delay (intrinsic device speed, CV/I) versus transistor physical gate length of NMOS devices.

PMOS:

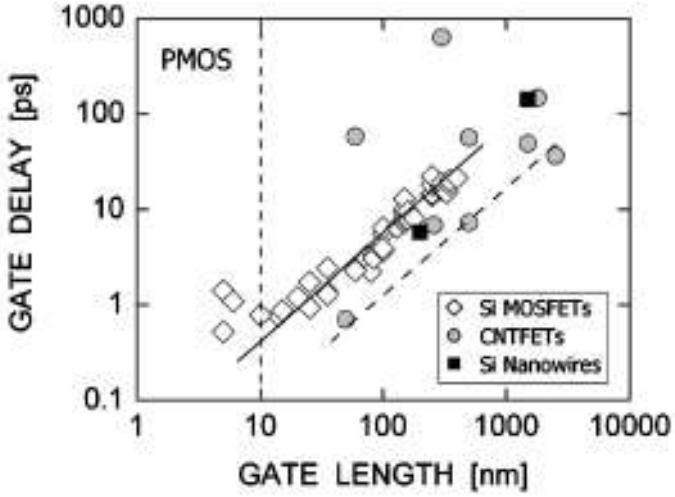


Fig. 4. Gate delay (intrinsic device speed CV/I) versus transistor physical gate length of PMOS devices.

III/V NMOS have better performance!

Energy-delay product

NMOS:

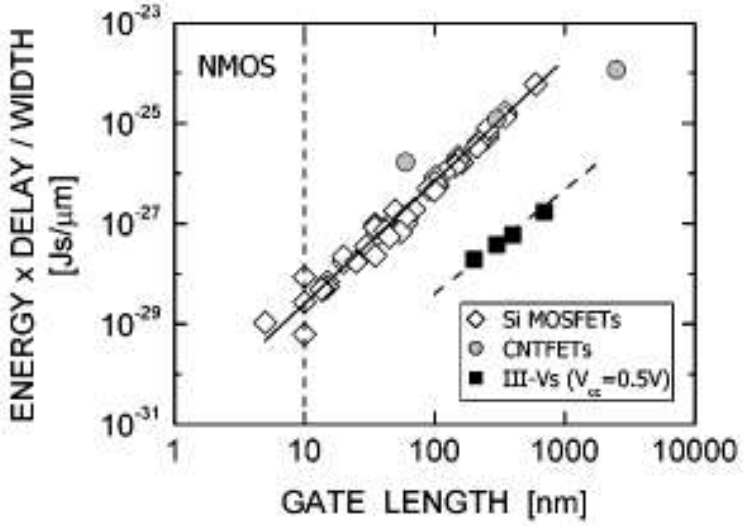


Fig. 7. Energy-delay product per device width versus transistor physical gate length of NMOS transistors.

PMOS:

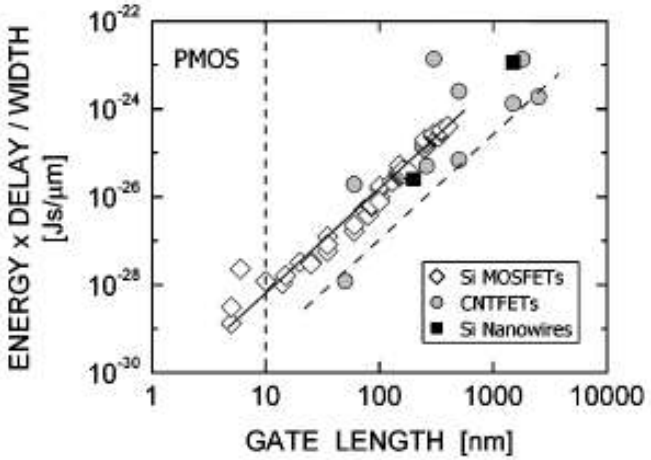


Fig. 6. Energy-delay product per device width versus transistor physical gate length of PMOS transistors.

III/V NMOS have better performance!

Scalability and leakage

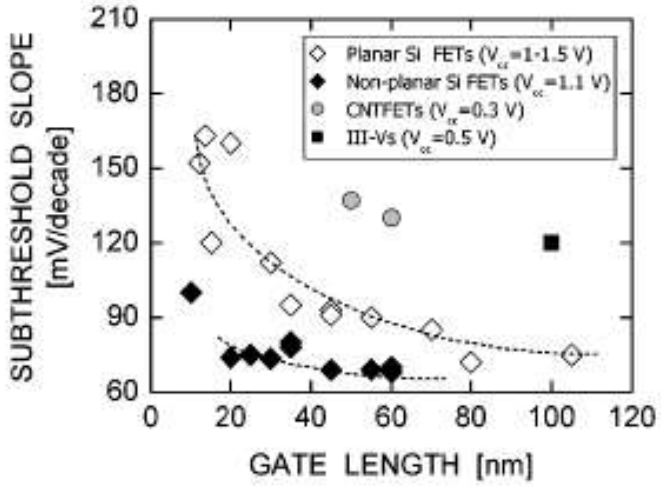


Fig. 8. Subthreshold slope versus transistor physical gate length. The planar and nonplanar Si FETs as well as the III–V planar devices are n-channel transistors, while the CNT FETs are p-channel transistors.

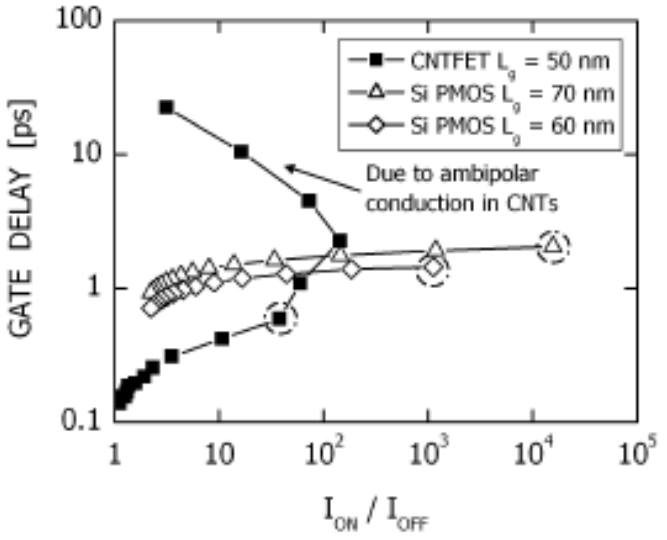


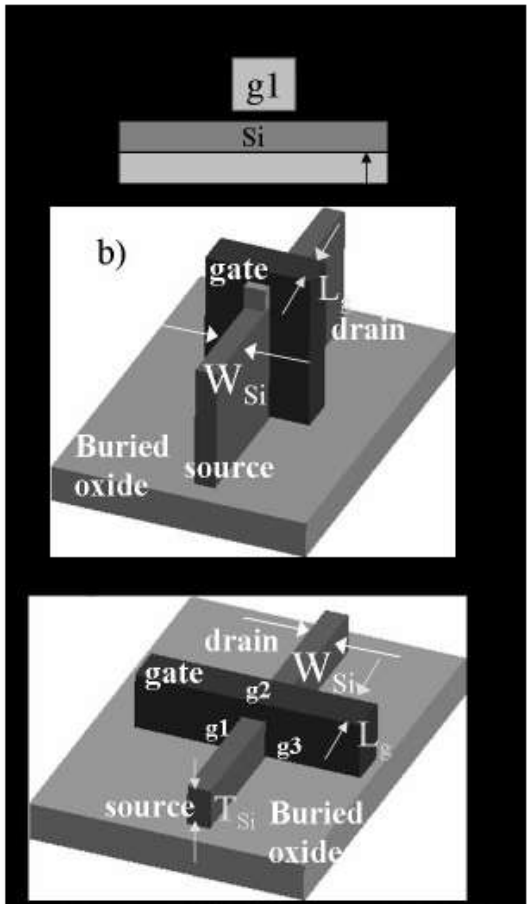
Fig. 11. Gate delay (intrinsic device speed, CV/I) versus on-to-off state current ratio I_{ON}/I_{OFF} of Si PMOS transistors with $L_g = 60$ nm and 70 nm at $V_{CC} = 1.3$ V, and a CNT PMOS transistor with $L_g = 50$ nm and $V_{CC} = 0.3$ V [15]. The three circled points were used in the PMOS CV/I versus L_g plot in Fig. 4, where the V_G swing is anchored around $V_G = V_T$.

IEEE ELECTRON DEVICE LETTERS, VOL. 24, NO. 4, APRIL 2003 263

High Performance Fully-Depleted Tri-Gate CMOS Transistors

B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, *Member, IEEE*, A. Murthy, R. Rios, *Member, IEEE*, and R. Chau, *Senior Member, IEEE*

Advanced Device Architectures:



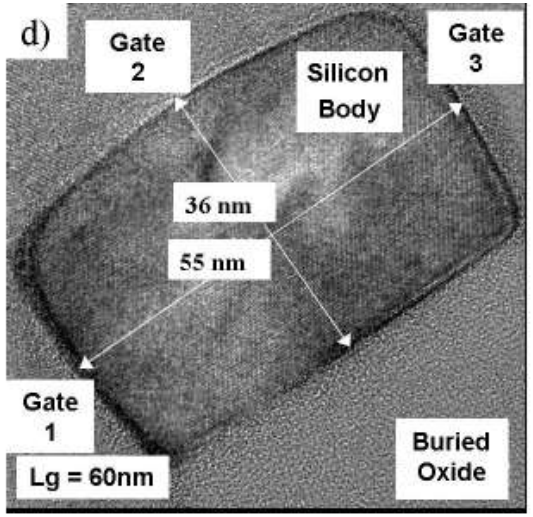
Planar single gate

Double-gate
(fin width one third of gate length)

Tri-gate
(body thickness about gate length)

CMOS

Si body of Tri-gate transistor



Performance of 60 nm gate length

I_{on}=0.52 mA/μm
I_{off}=24 nA/μm
SS=69.5 mV/dec

I_{on}=1.14 mA/μm
I_{off}=70 nA/μm
SS=68 mV/dec

DIBL=48 mV/V

DIBL=41 mV/V

DIBL=$V_{g@Vd=1.3V}$-$V_{g@Vd=0.05V}$/(1.3-0.05)
V_g taken at I_d=0.1 μA/μm

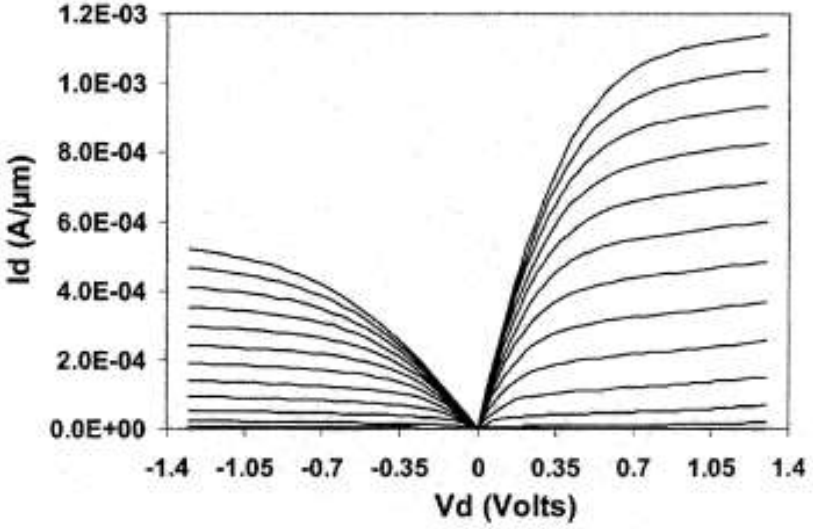


Fig. 3. I_d–V_d characteristics of the 60 nm N- and P-MOS devices of Fig. 2. The gate voltage was ramped to 1.3 V in increments of 0.1 V.

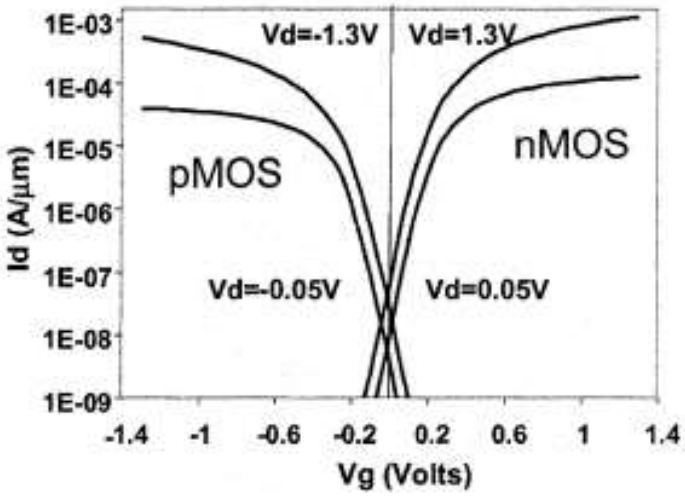


Fig. 2. I_d–V_g characteristics of 60 nm gate length NMOS and PMOS transistors. The current I_d is normalized to the width (Z) in all cases, where $Z = 2 * T_{Si} + W_{Si}$.

15 Å oxide thickness

Comparable to well-optimized planar devices!

Vol 441|25 May 2006|doi:10.1038/nature04796 nature

LETTERS

Ge/Si nanowire heterostructures as high-performance field-effect transistors

Jie Xiang[1]*, Wei Lu[1]*, Yongjie Hu[1], Yue Wu[1], Hao Yan[1] & Charles M. Lieber[1,2]

- Ge/Si core shell nanowires
- 15 nm core
- p-type conduction
- High-k dielectrics (ZrO_2)
- ballistic transport
- 500 nm mean free path

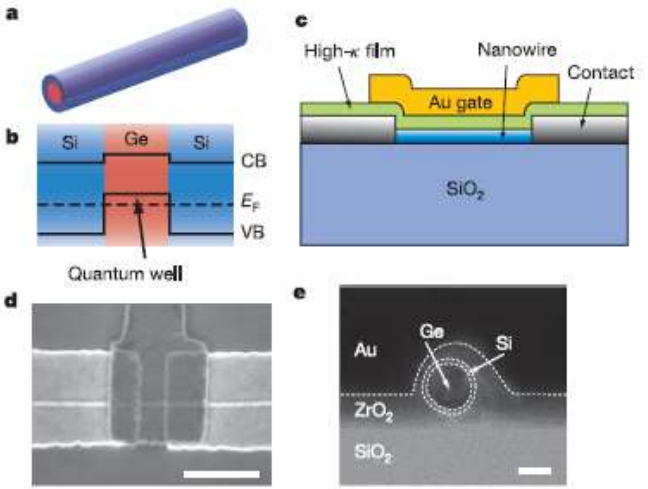
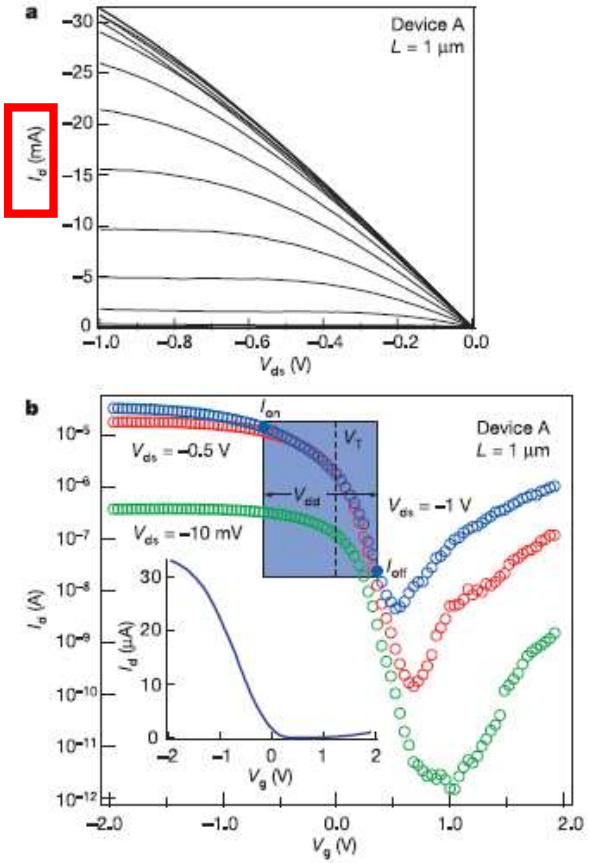


Figure 1 | Ge/Si core/shell NWFET. **a**, Schematic of a Ge/Si core/shell nanowire. **b**, Cross-sectional diagram showing the formation of hole-gas in the Ge quantum well confined by the epitaxial Si shell, where CB is the conduction band and VB is the valence band. The dashed line indicates the Fermi level, E_F. The valence band offset of ~500 meV between Ge and Si serves as a confinement potential to the hole-gas as discussed previously[7]. **c**, Schematic of the NWFET device with high-κ dielectric layer and Au top gate. **d**, Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar, 500 nm. **e**, Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Dotted lines are guides to the eye showing boundaries between different materials denoted in the image. The nanowire is tilted off the imaging axis. Scale bar, 10 nm.

Device Characteristics



L_g=1 μm
g_m=26 μS
I_{dmax}=35 μA
Benchmark at 1V:
I_{on}=14 μA
g_m= 1.4 mS/μm
I_{on}=0.71 mA/μm

L_g=0.19 μm
g_m=60 μS
I_{dmax}=91 μA
Benchmark at 1V:
I_{on}=37 μA
g_m= 3.3 mS/μm
I_{on}=2.1 mA/μm
mobility=730 cm^2/V
SS=100 mV/dec.

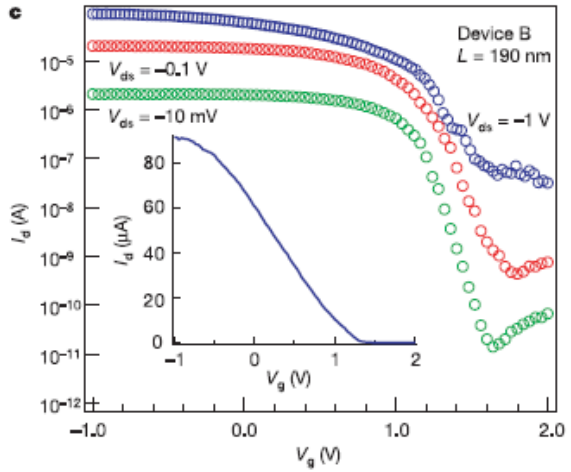


Figure 2 | Characteristics of high-performance Ge/Si NWFET. **a**, I_d–V_{ds} data for device A ($L = 1\,\mu m$, 4 nm HfO_2 dielectric) with $V_g = -2$ to 2 V in 0.25 V steps from top to bottom. **b**, I_d–V_g for device A with blue, red, and green data points corresponding to V_{ds} values of −1, −0.5 and −0.01 V, respectively. The leakage current through the gate electrode (I_g) is $<10^{-10}$ A, which excludes I_g as source of increase in I_d at $V_g > \sim 0.5$ V. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V. The blue-shaded area defines the 1 V gate voltage window described in the text, where V_T was determined from the intercept of the tangent of maximum slope (linear transconductance) region of the I_d–V_g curve[11]. **c**, I_d–V_g data for device B ($L = 190$ nm, 4 nm HfO_2 dielectric) with blue, red and green data points corresponding to V_{ds} values of −1, −0.1 and −0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V.

Device Performance

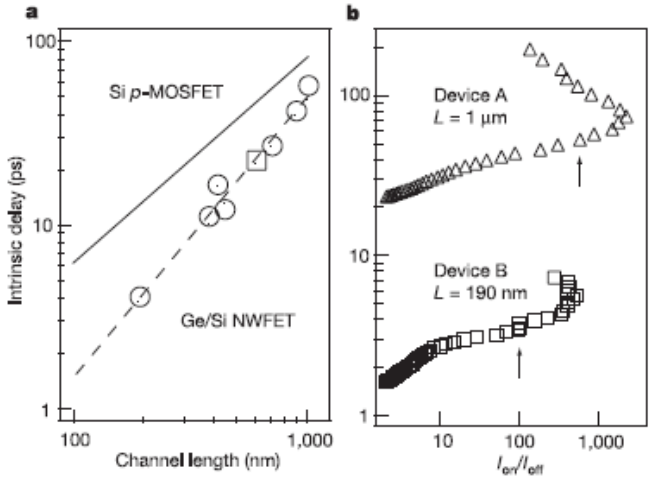


Figure 3 | Benchmark and comparison of Ge/Si FETs. **a**, Intrinsic delay τ versus channel length for seven different Ge/Si nanowire devices with HfO_2 dielectric (open circle) and ZrO_2 dielectric (open square). Data for devices A and B are included. The I_{on} values were measured at $V_{g(on)} = V_T - 0.7V_{dd}$, as discussed in the text. The dashed line is a fit to the data points while solid line is the Si *p*-MOSFET results from ref. 4. **b**, Intrinsic delay versus on/off ratio for the two devices in Fig. 2. Arrows indicate the values of intrinsic delay used in **a**.

V_T shift due to different work functions

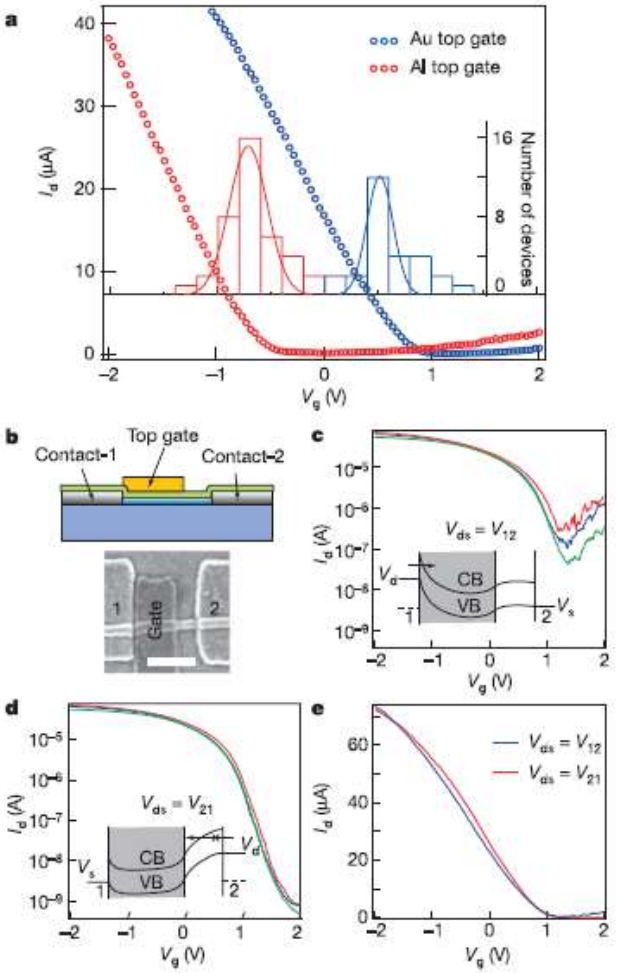


Figure 4 | Control of threshold voltage and ambipolar conduction through device design. **a**, I_d–V_g curves for two $L = 300$ nm devices with Au (blue) and Al (red) top gate electrodes ($V_{ds} = -1$ V). Inset shows histogram of V_T with the same V_g axis for a total of 68 $L = 300$ nm devices with Au (blue) and Al (red) top gates. Solid lines correspond to gaussian fits to the two distributions. **b**, Schematic and SEM image of the asymmetrical gate structure designed to suppress ambipolar conduction. Scale bar, 300 nm. **c**, I_d–V_g of partially gated device with ambipolar conduction; bias was applied to contact 1 ($V_{ds} = V_{12}$). Inset, schematic of band bending in the NWFET at finite bias. Arrow denotes electron injection at the drain contact. **d**, I_d–V_g for $V_{ds} = V_{21}$. Inset, schematic of band bending with electron injection denoted by arrow. The red, blue and green curves in **c** and **d** correspond to V_{ds} values of −1, −0.8 and −0.6 V, respectively. **e**, Linear scale I_d–V_g ($V_{ds} = -1$ V) for the devices in **c** and **d**. The two devices have the same peak $g_m = 35\,\mu S$ and $I_{d(max)} = 73\,\mu A$.

Gate delay:

-L_g=1 μm => τ=57 ps
-L_g=0.19 μm => τ=4 ps

Nanoelectronics: Si Nanowires

IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 3, MARCH 2007

Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors

W. W. Fang, N. Singh, *Member, IEEE*, L. K. Bera, H. S. Nguyen, S. C. Rustagi, *Senior Member, IEEE*, G. Q. Lo, *Member, IEEE*, N. Balasubramanian, *Member, IEEE*, and D.-L. Kwong, *Senior Member, IEEE*

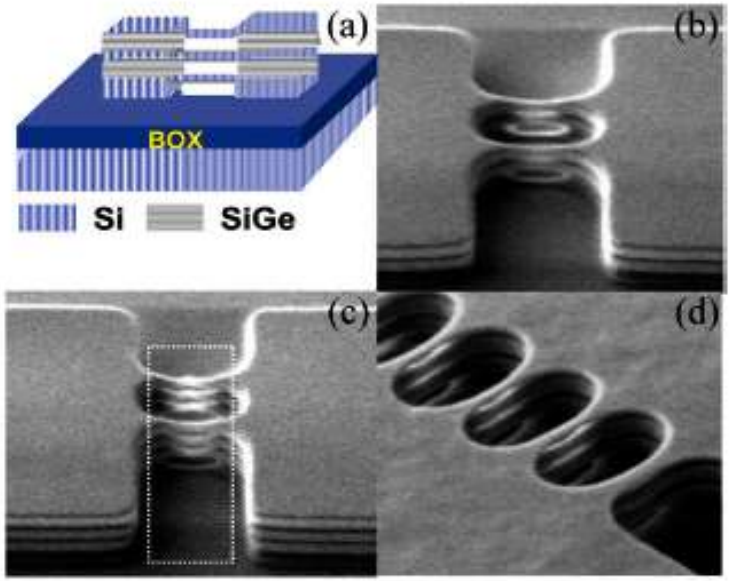


Fig. 1. Tilted view SEM images after release of stacked NW. (a) Schematic of SiGe NW stacks after oxidation and release. (b) 2X laterally arrayed three-stacked NWs. (c) 2X laterally arrayed four-stacked NWs with the dashed line indicating the gate layout. (d) 5X laterally arrayed four-stacked NWs.

-Ge condensation technigue

-- SiGe oxidizes faster than Si

-patterning of 100 nm fins

- cyclic oxidation and etching to 20-30 nm diameter wires

- 350 nm gate length, t_{ox} 4 nm

- i-Si and implantation of S/D regions

Device characteristics

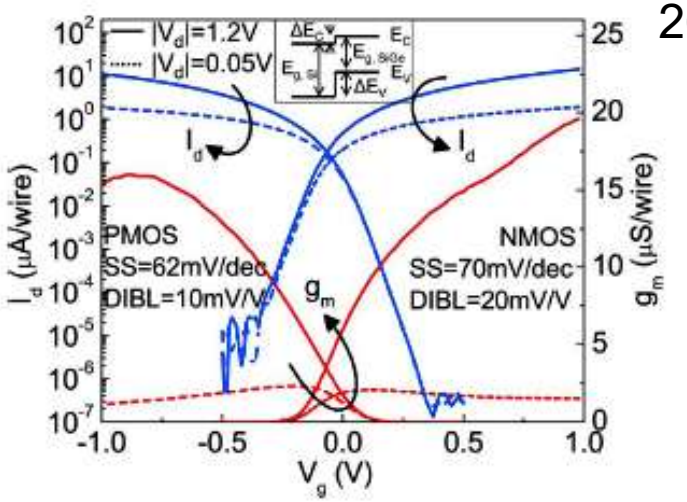


Fig. 2. Per NW I_d–V_g and g_m–V_g plots for stacked NW n-FETs and p-FETs with $L_g = 500$ nm and NW diameter ~30 nm.

265 mS/mm

159 mA/mm

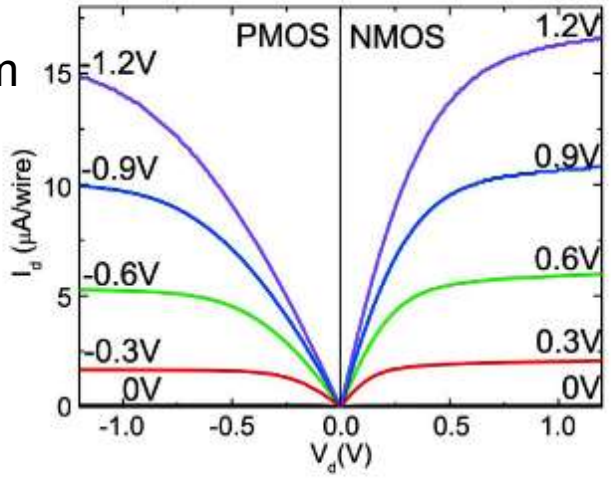


Fig. 3. Per NW I_d–V_d plot for n-FETs and p-FETs with gate overdrive voltage varying in steps of 300 mV.

Performance scales with number of wires in stack!
Surface is Ge rich
Hole accumulation at the surface and electrons in the core
Difference in scattering affects g_m

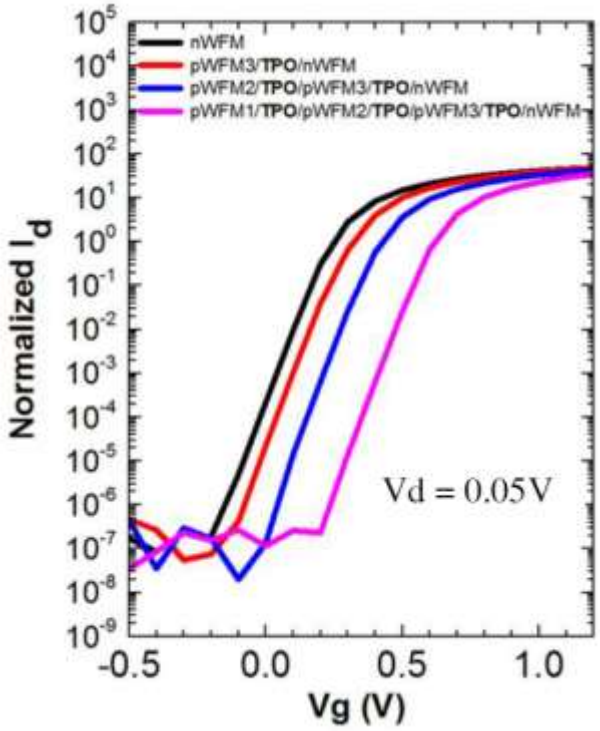
Status 2019: Device Development

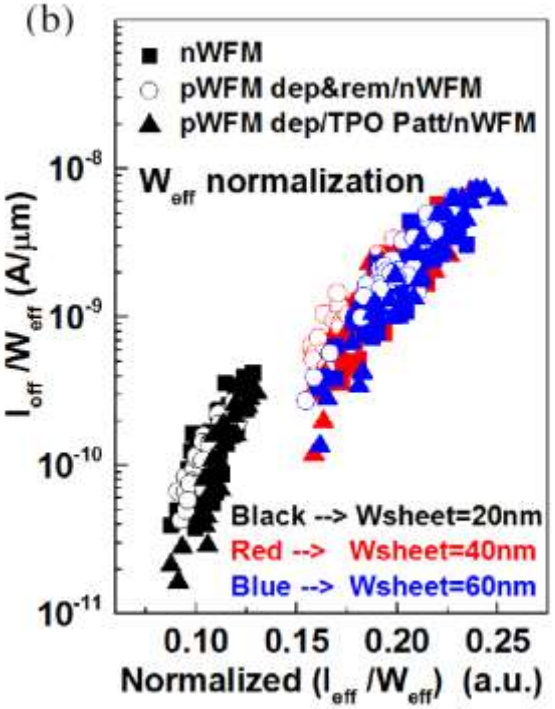
Multiple-Vt Solutions in Nanosheet Technology for H igh Performance and Low Power Applications

R. Bao, K. Watanabe, J. Zhang, J. Guo, H. Zhou, A. Gaul, M. Sankarapandian, J. Li, A. R. Hubbard, R. V ega, S. Pancharatnam, P. Jamison, M. Wang, N. Loubet, V. Ba sker, D. Dechene, D. Guo, B. Haran, H. Bu, M. Khare
IBM Semiconductor Technology Research, Albany, NY, email: rbao@us.ibm.com

High-k and metals
to tune work function
Introduced between
The nanowires

Device characteristics





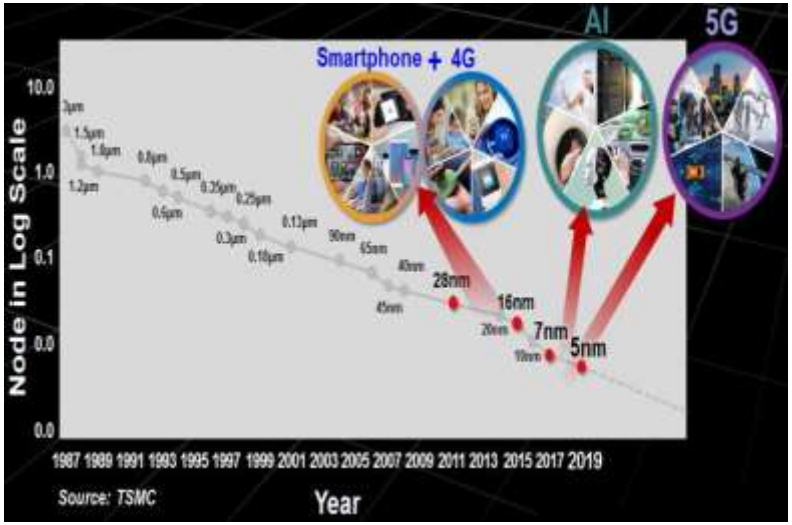
Different metal schemes used to vary transistor V_t
Not much space but still possible

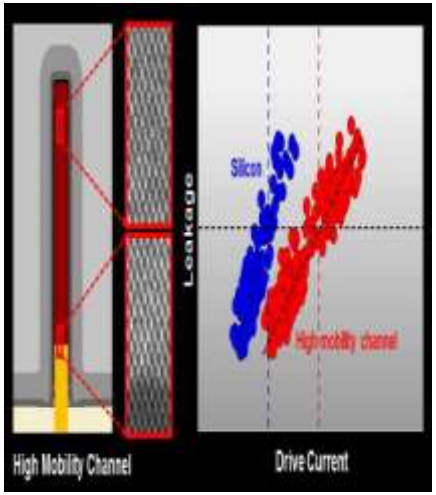
TSMC 5 nm node 2020

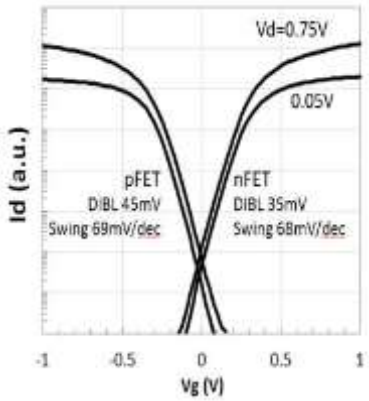
5nm CMOS Production Technology Platform featuring full-fledged EUV, and High Mobility Channel FinFETs with densest 0.021μm² SRAM cells for Mobile SoC and High Performance Computing Applications

Geoffrey Yeap, S.S. Lin, Y.M. Chen, H.L. Shang, P.W. Wang, H.C. Lin, Y.C. Peng, J.Y. Sheu, M. Wang, X. Chen, B.R. Yang, C.P. Lin, F.C. Yang, Y.K. Leung, D.W. Lin, C.P. Chen, K.F. Yu, D.H. Chen, C.Y. Chang, H.K. Chen, P. Hung, C.S. Hou, Y.K. Cheng, J. Chang, L. Yuan, C.K. Lin, C.C. Chen, Y.C. Yeo, M.H. Tsai, H.T. Lin, C.O. Chui, K.B. Huang, W. Chang, H.J. Lin, K.W. Chen, R. Chen, S.H. Sun, Q. Fu, H.T. Yang, H.T. Chiang, C.C. Yeh, T.L. Lee, C.H. Wang, S.L. Shue, C.W. Wu, R. Lu, W.R. Lin, J. Wu, F. Lai, Y.H. Wu, B.Z. Tien, Y.C. Huang, L.C. Lu, Jun He, Y. Ku, J. Lin, M. Cao, T.S. Chang, S.M. Jang

Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C. Email: gyeap@tsmc.com







Nanoelectronics: Si Nanowires

18% increase in drive current!
IEDM 2019