Nanoelectronics

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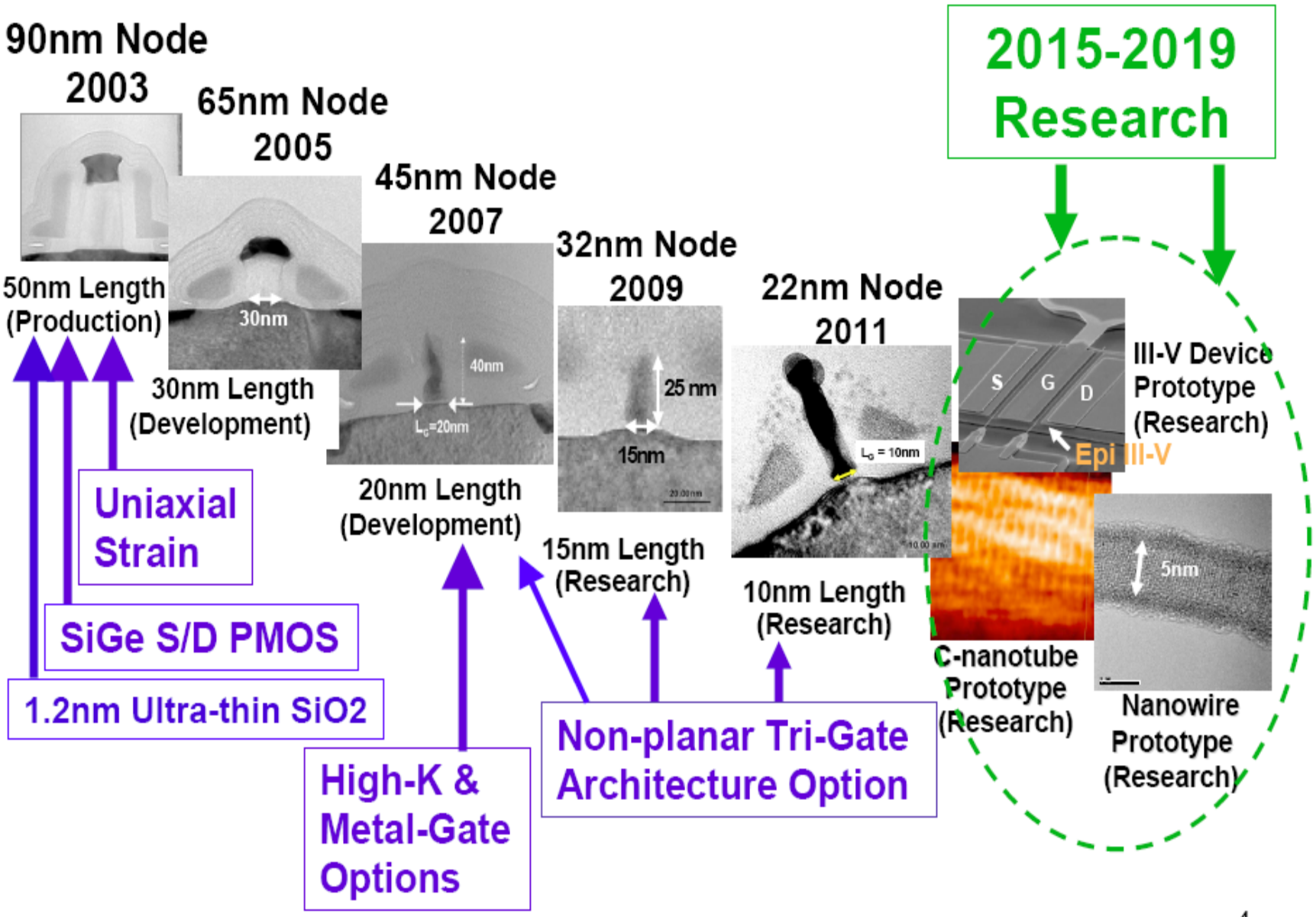
Research-oriented course

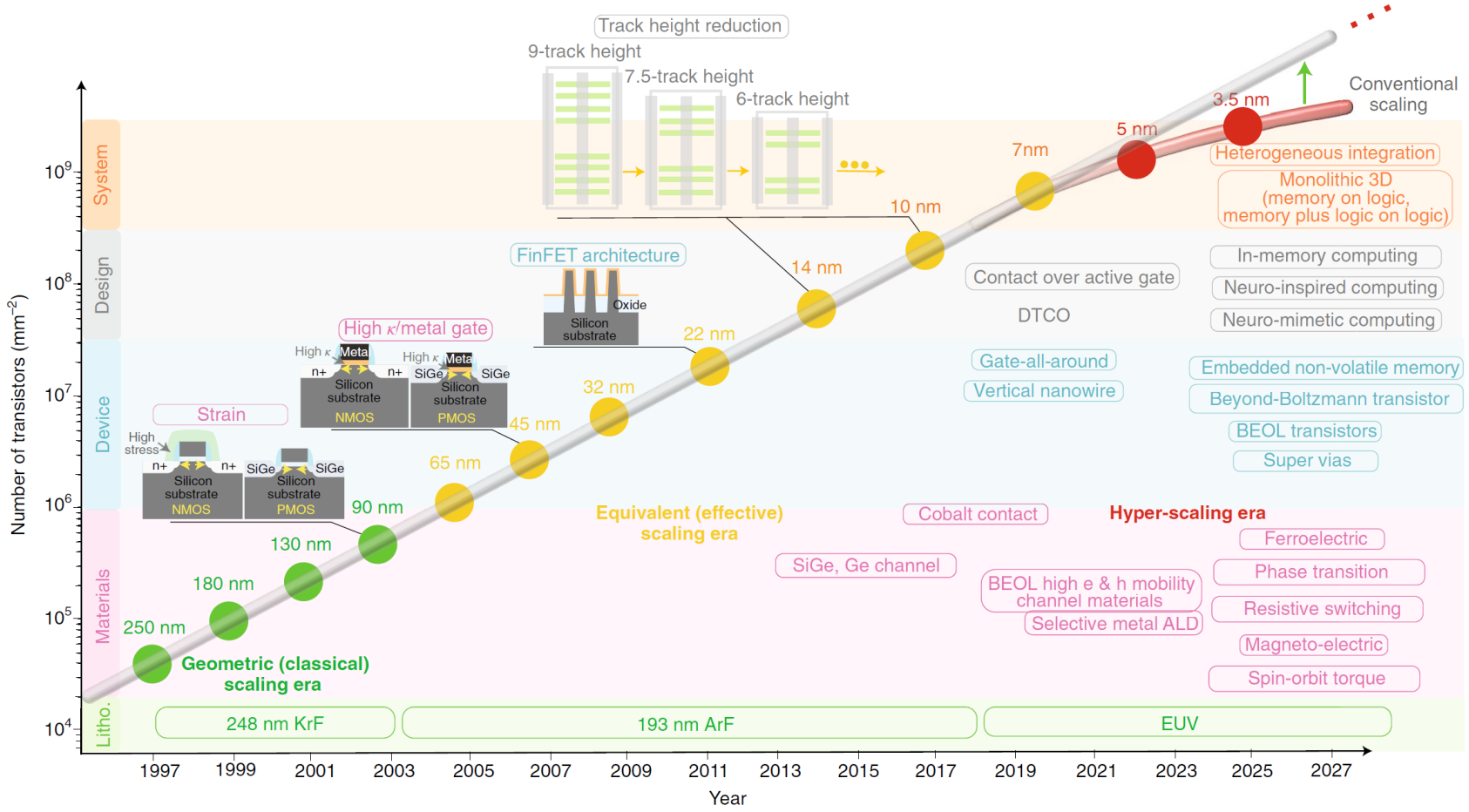
Learning by reading research articles
- Identify key facts from articles
- Use commencial simulation tool to identify transistor benefits in circuit
- Writing short research article

Transistor Scaling and Research Roadmap



Robert Chau, Intel, ICSICT 2004

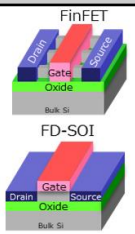
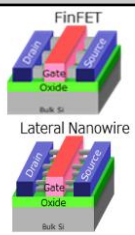
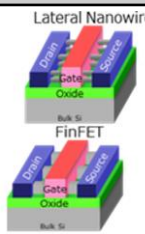
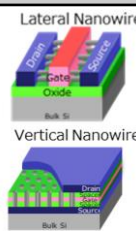
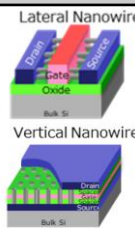
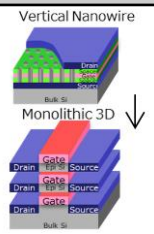
Scaling Laws 2018…



Vertical III-V Nanowires in the Roadmaps

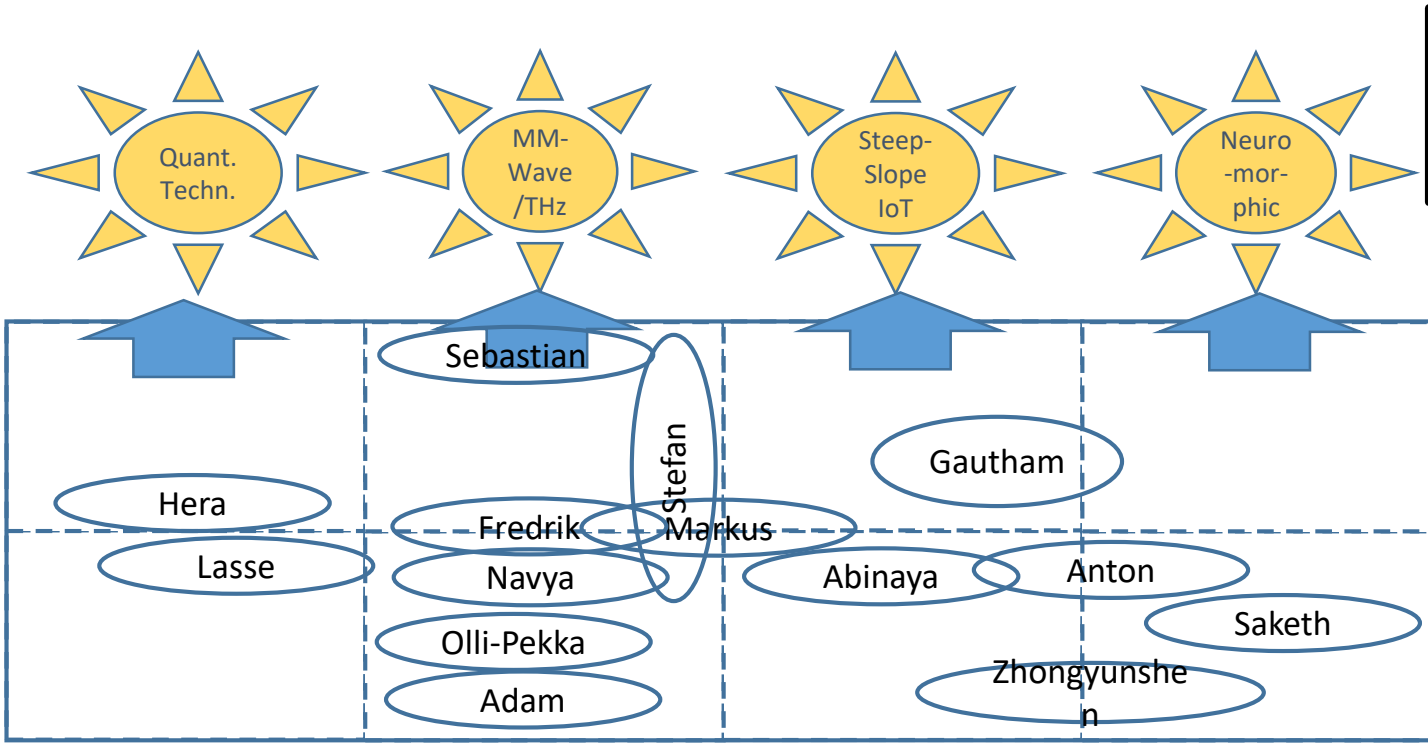
Lateral and vertical III-V nanowires are part of IRDS Roadmap!
Lund University has demonstrated state-of-the-art performance devices!
How to take advantage of our demonstrated knowledge basis?

Adapted from IRDS, *Logic core device technology roadmap, More Moore report*, 2017

Year	2017	2019	2021	2024	2027	2030
Device Structures						
Channel	Si	SiGe25%	SiGe50%	Ge, **III-V**, TFET, 2D	Ge, **III-V**, TFET, 2D mat	Ge, **III-V**, TFET, 2D mat

Courtesy of C. Convertino IBM

Nanoelectronics 2030-45



Basic Engineering Science
Focus on Pre-Competitive Efforts

Application Specific Technology

III-V Technology Platform

Lateral and Vertical NWs
Complex oxides
BEOL

Science and technology on internationally competetive level
Attract industrial funding

Current Trends in Device Scaling

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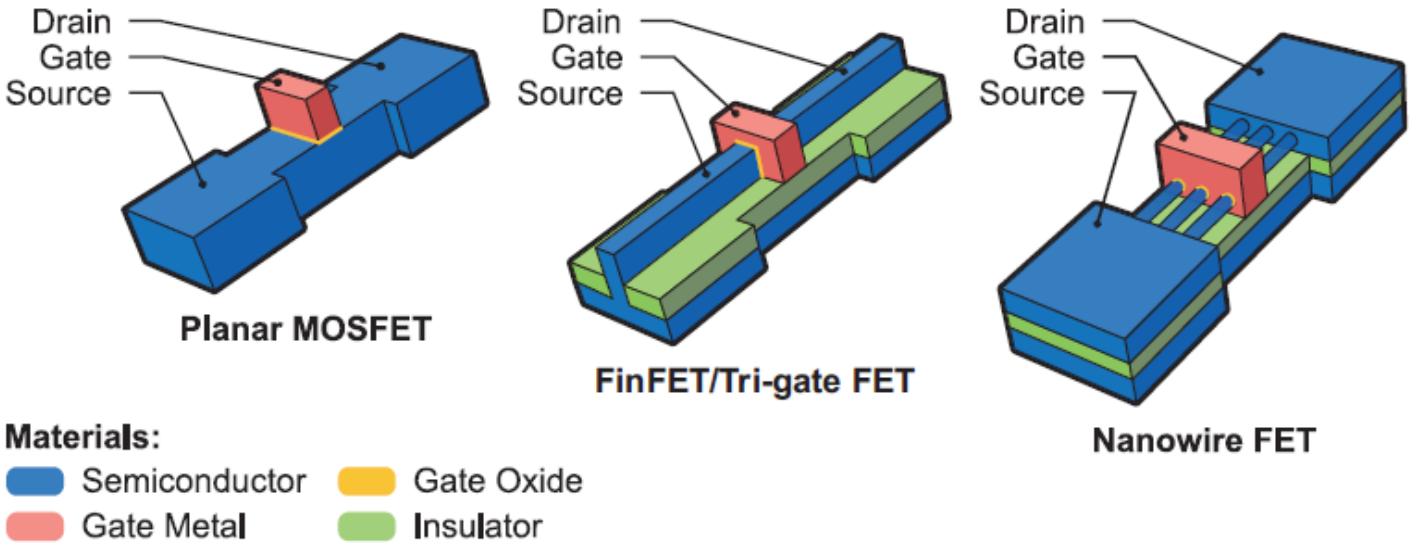
Nanowires are a natural extension of the transistor evolution



Riel et al, MRS Bulletin 2014

Why III-V Nanowires

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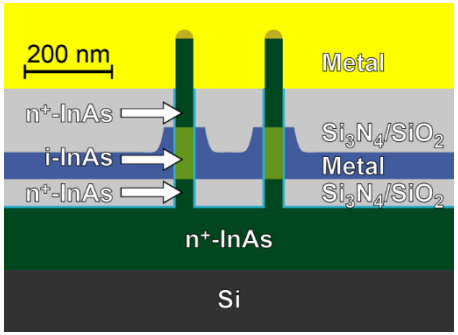
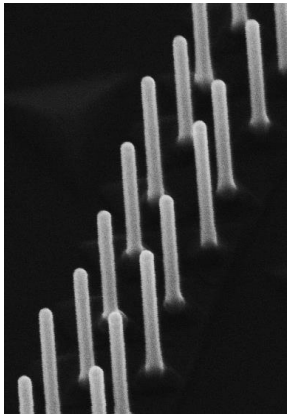
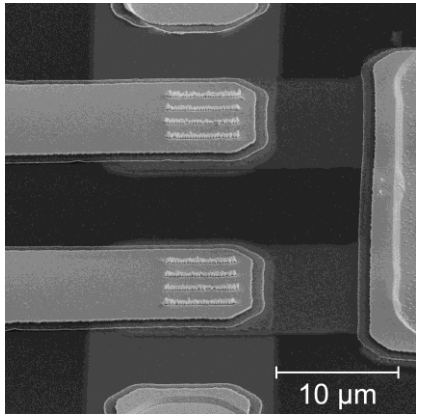
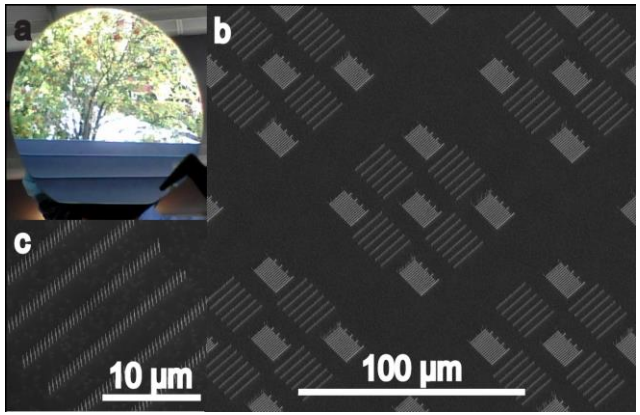
Why III-V Nanowires?

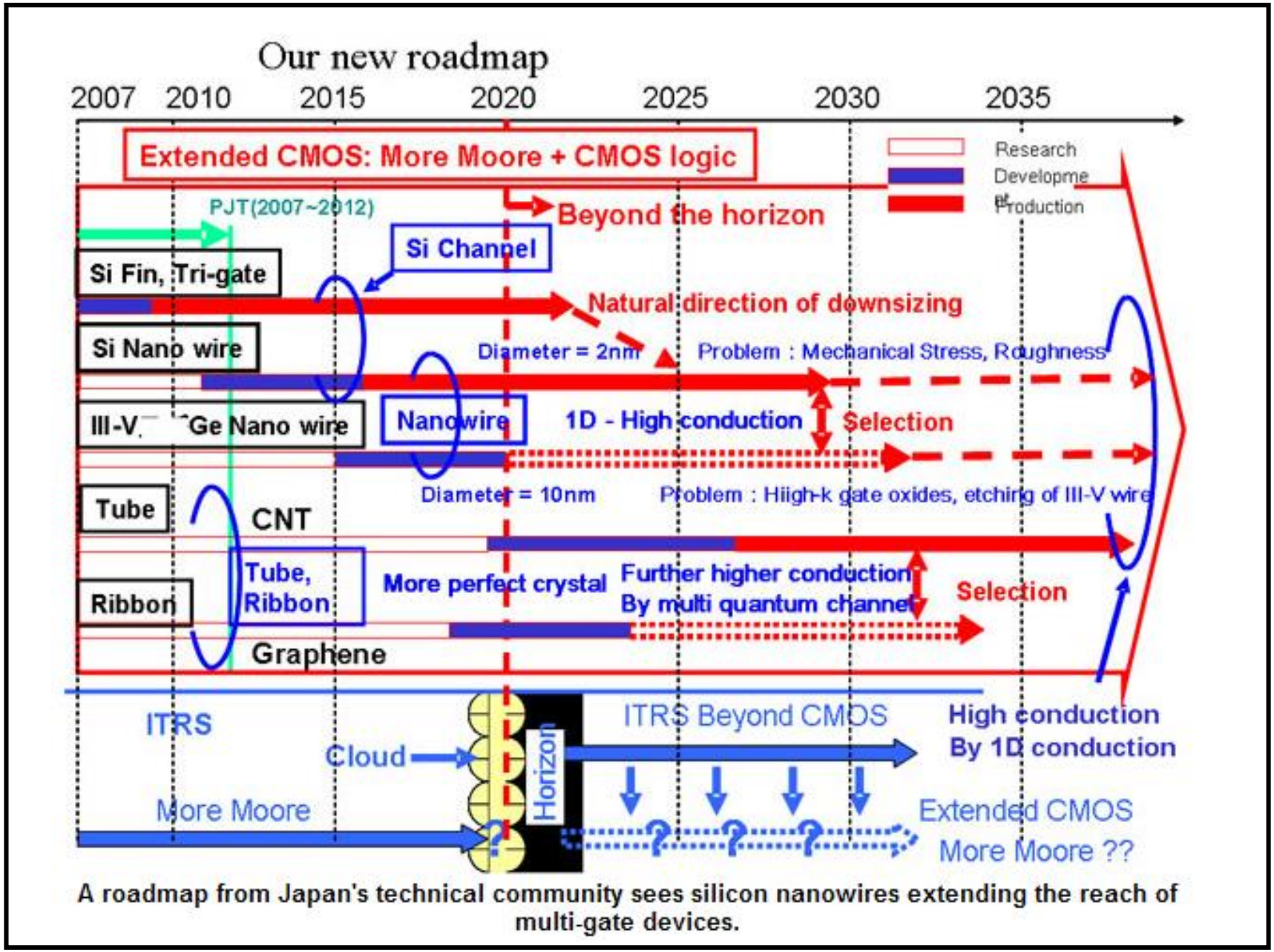
- **Advantageous transport** → **high transconduc. and I_{on}**
- **Wrap-gate geometry** → **low output conduc. and DIBL**
- **Band gap engineering** → **increased breakdown, reduced I_{off}**
- **Small nanowire footprint** → **reduced defect propagation probability**









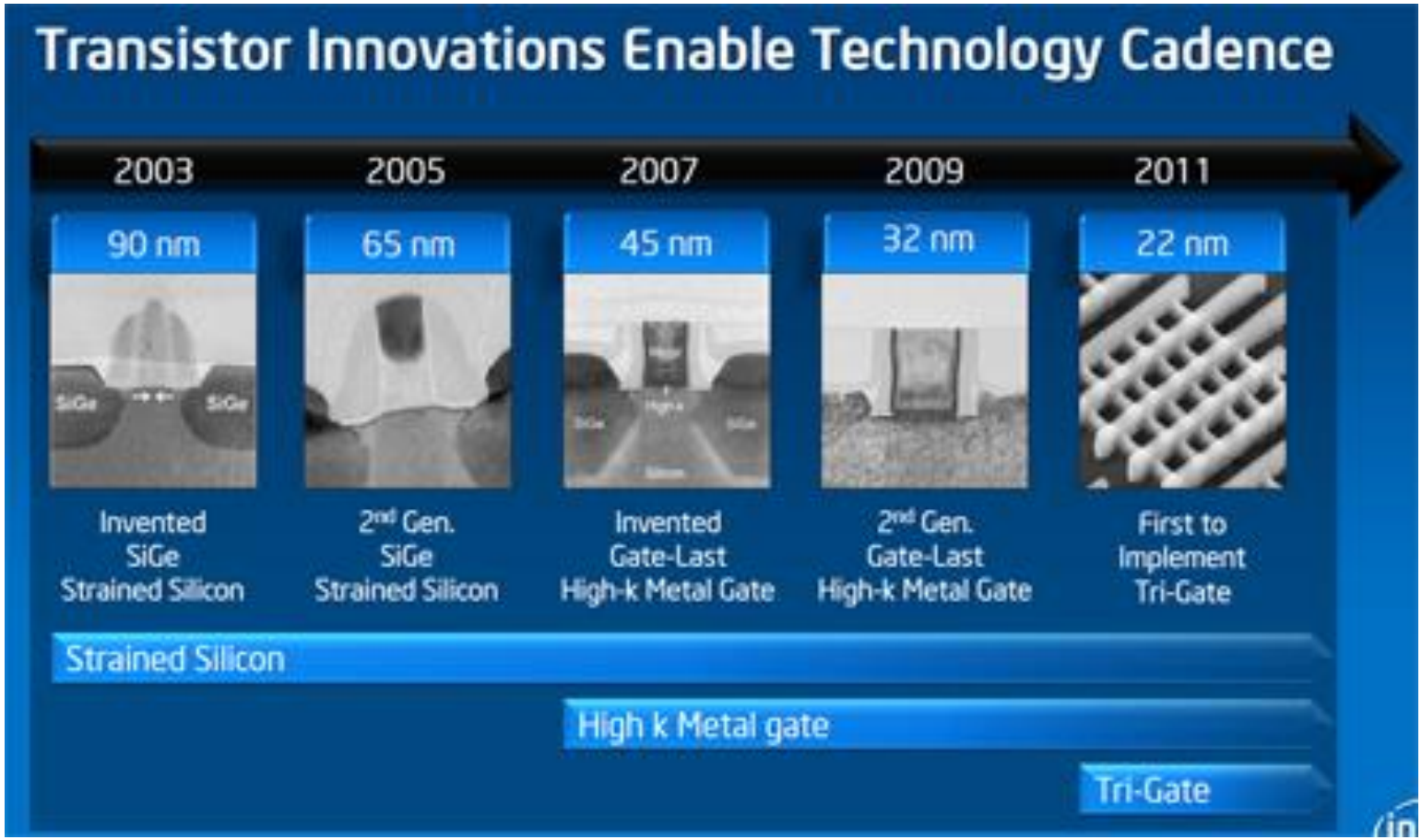


A roadmap from Japan's technical community sees silicon nanowires extending the reach of multi-gate devices.

EXPLORE

H. Iwai (Tokyo Institute of Technology), ISAGST, Sept. 25-28, 2007 Dallas, Texas, USA

Current Trends in Device Scaling



Current Trends in Device Scaling

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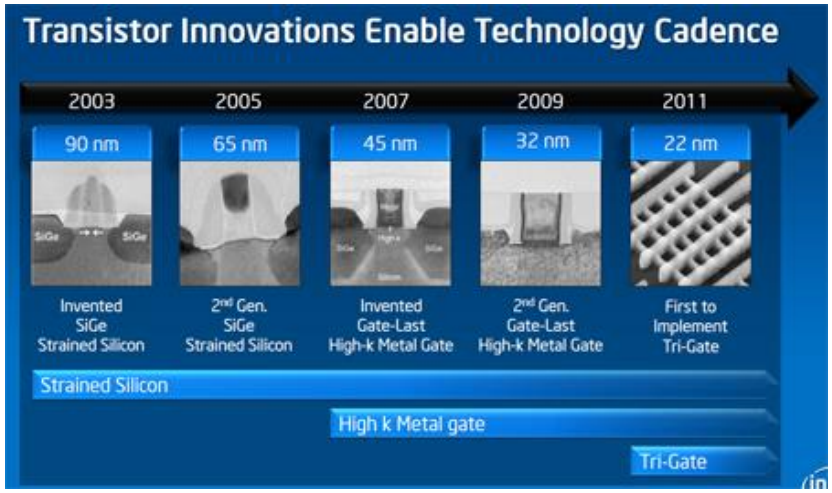
Transport Enhancement

Graphene

III-Vs

Strained Si



Electrostatics

Planar Technologies

FinFets Trigates

Nanowires

Current Trends in Device Scaling

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Transport Enhancement

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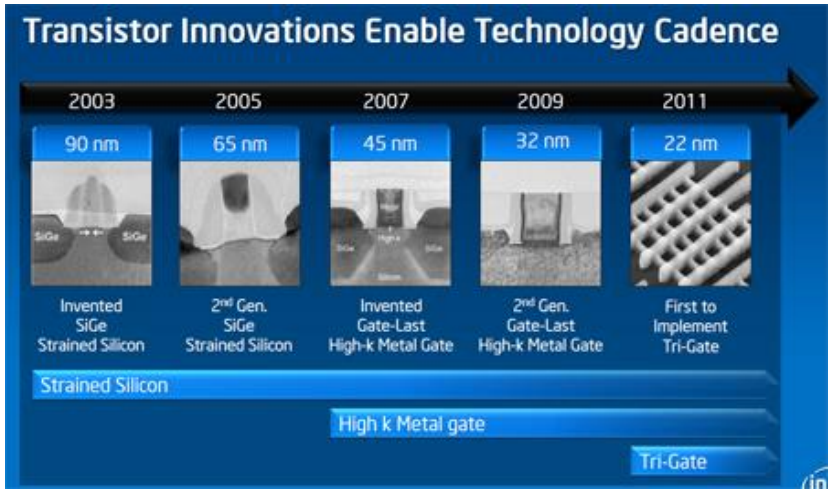
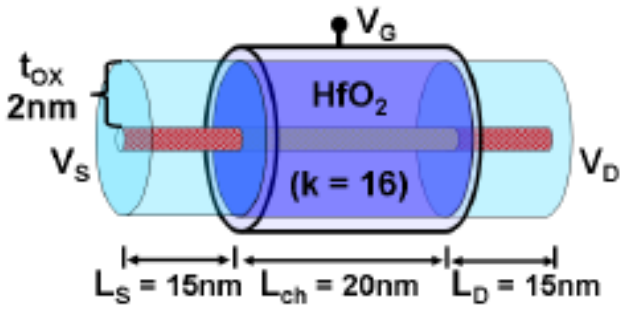
III-Vs

Strained Si





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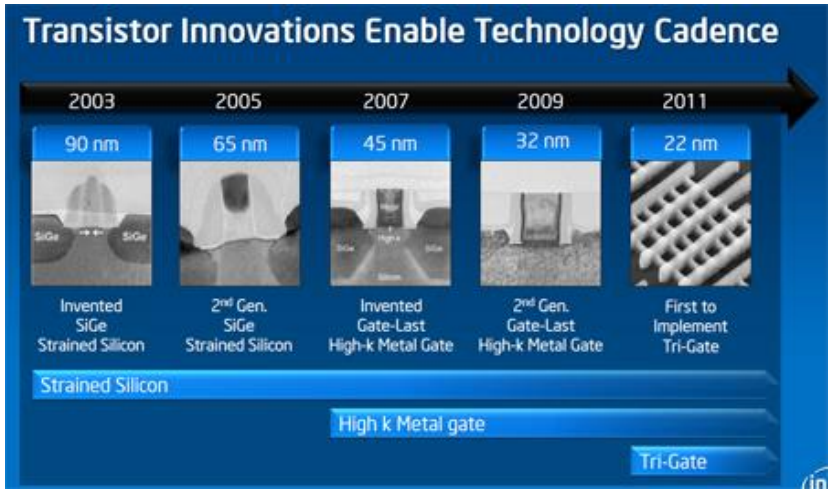

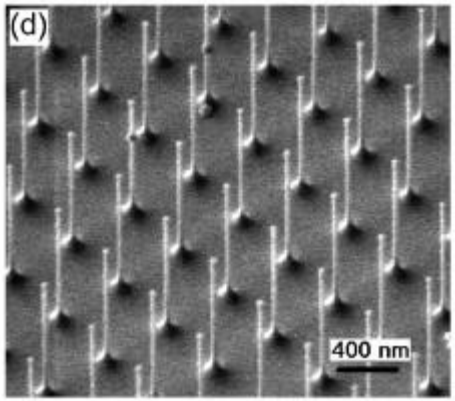

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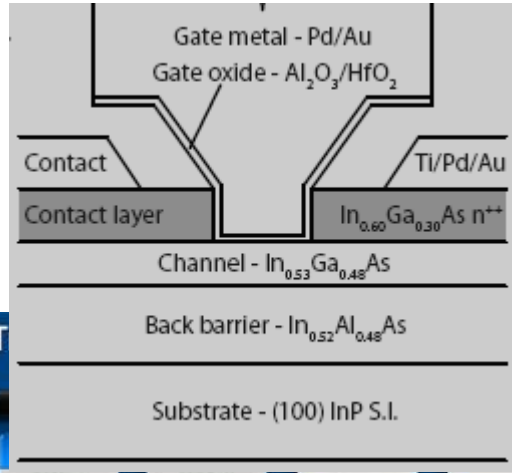
Transport Enhancement

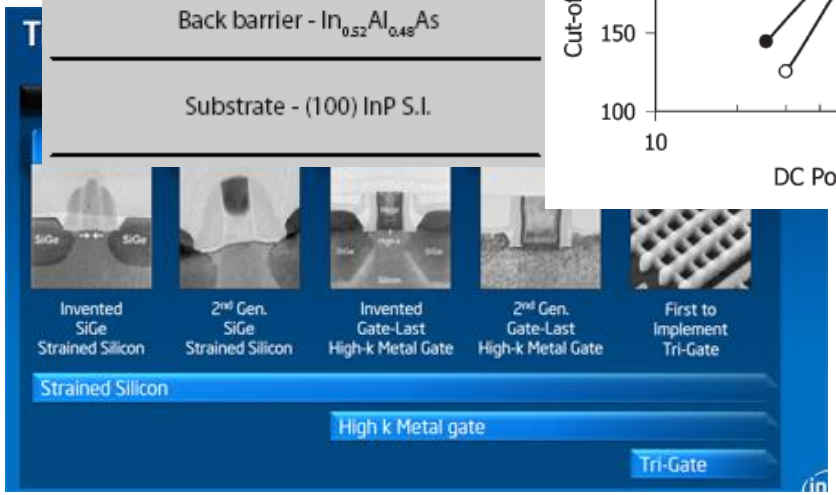
X2 performance increase

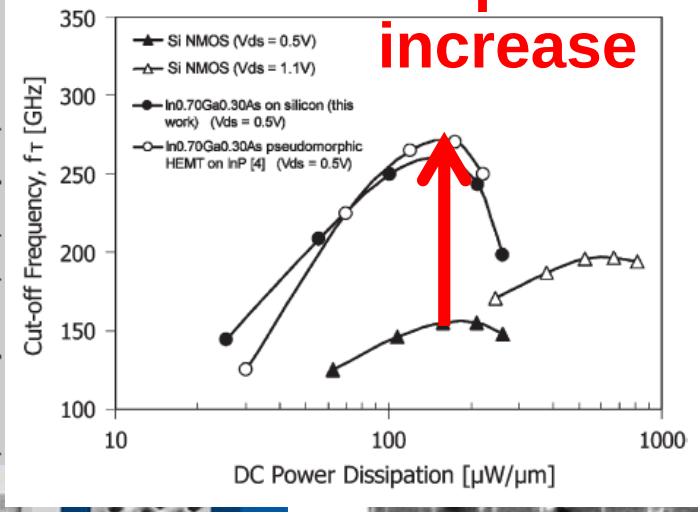
Graphene

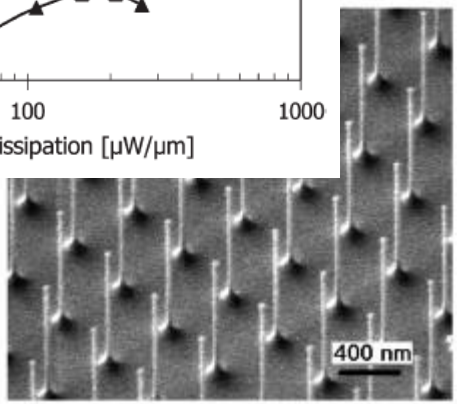
III-Vs

Strained Si









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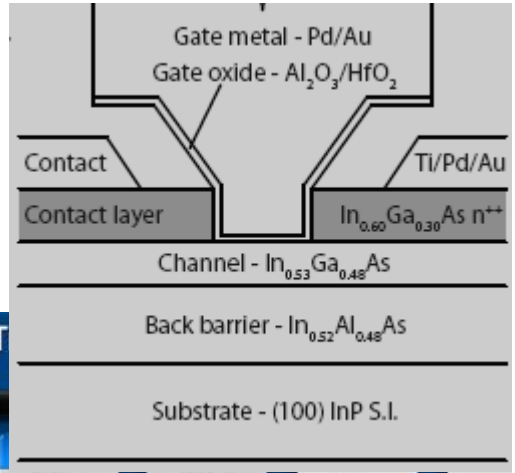
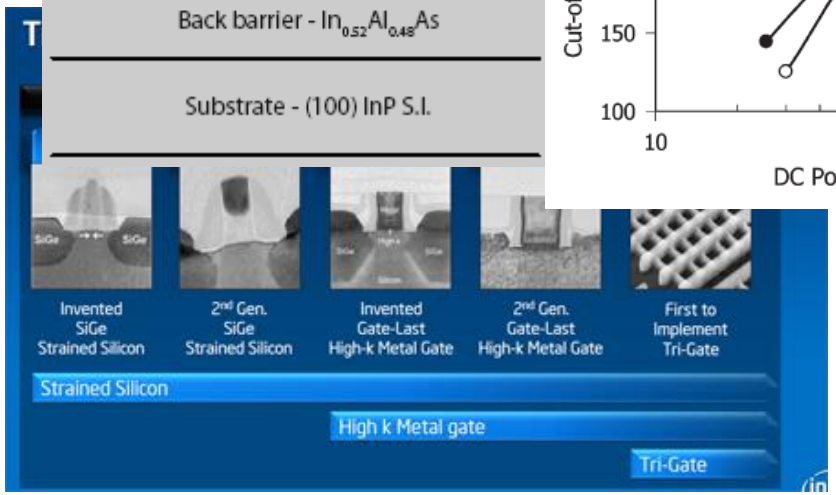
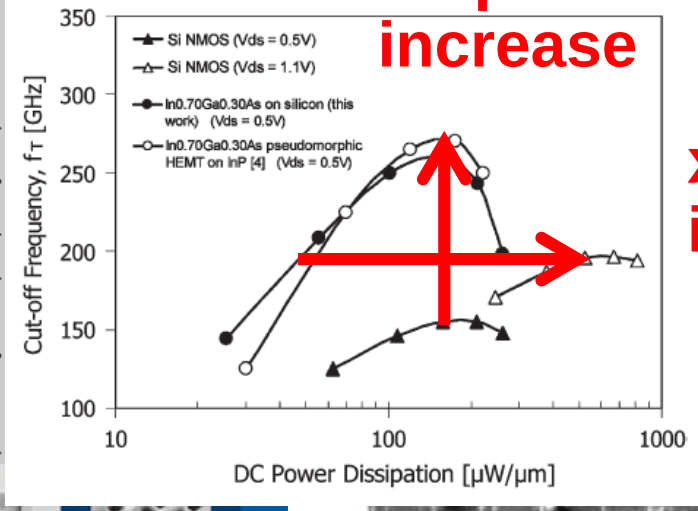
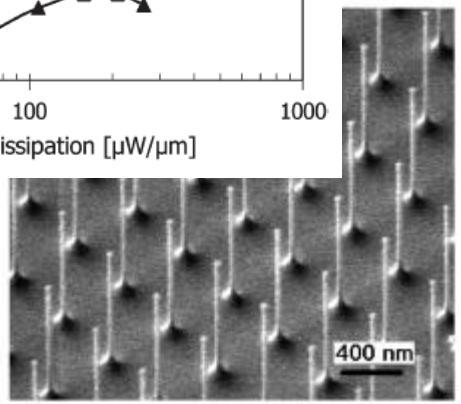




X2 performance increase



x10 power increase



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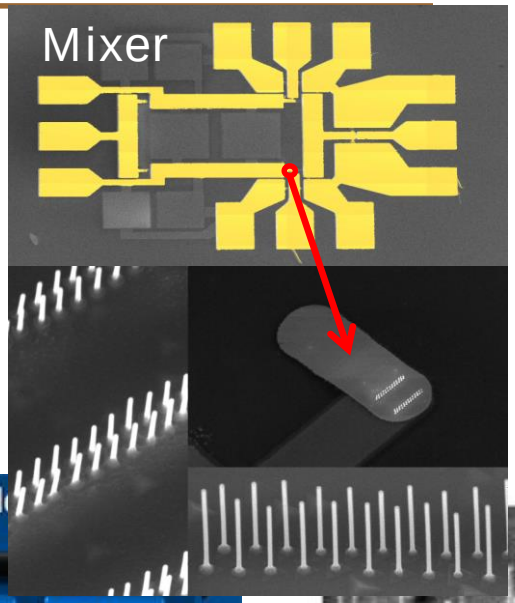

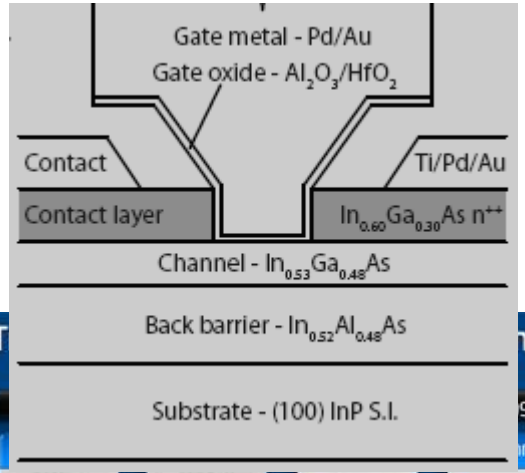

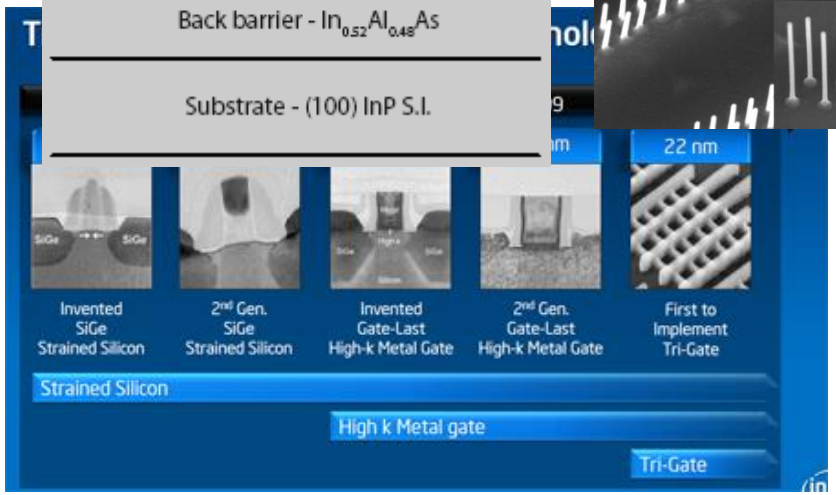

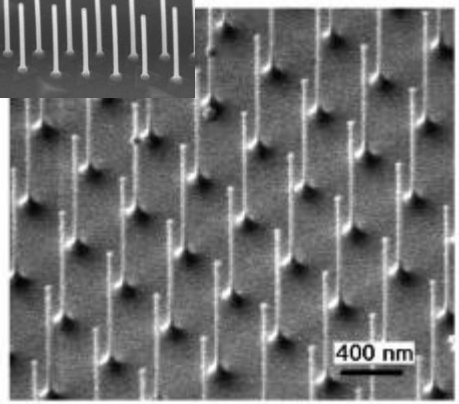

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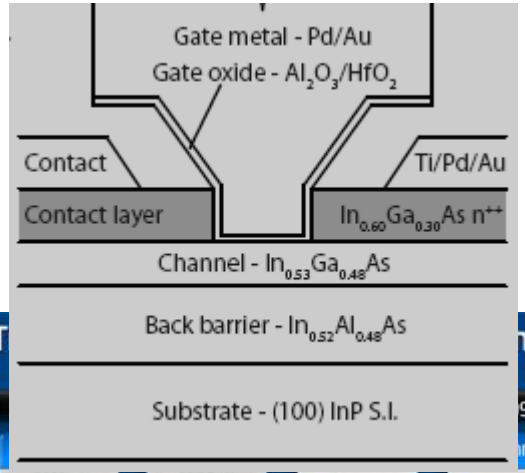
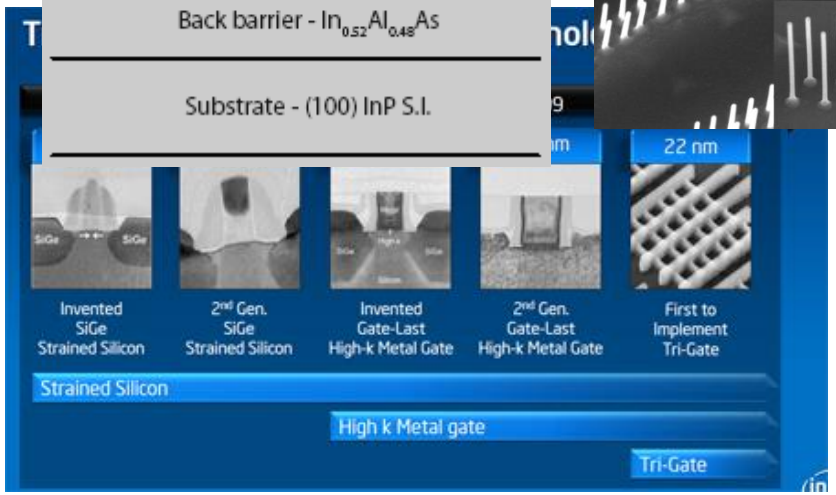
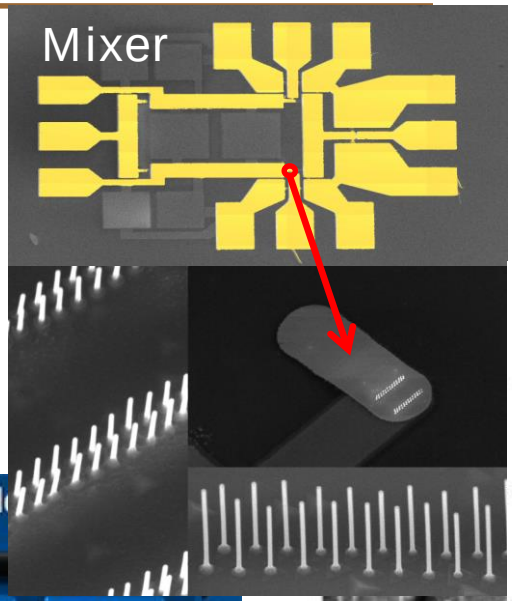
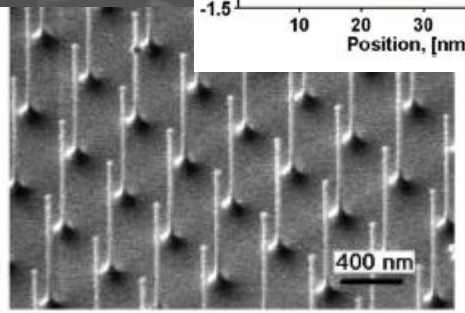
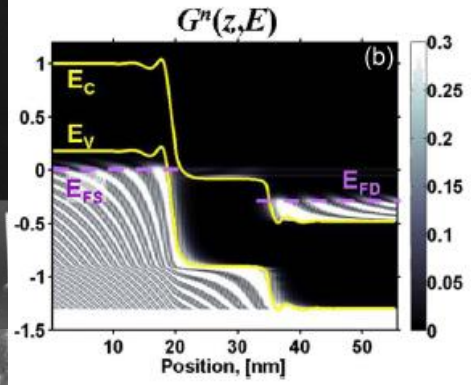








More than Moore
Beyond Moore



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Nanowires

What will you learn in this course?

How small transistors can we make?

How do we compare data for different transistors?

What are good numbers for a transistor?

What is the relation between the physics, the technology and the performance?

What are the ultimate limits in terms of power consumption?

What are the benefits of nanotechnology?

How can we implement high-speed circuits?