

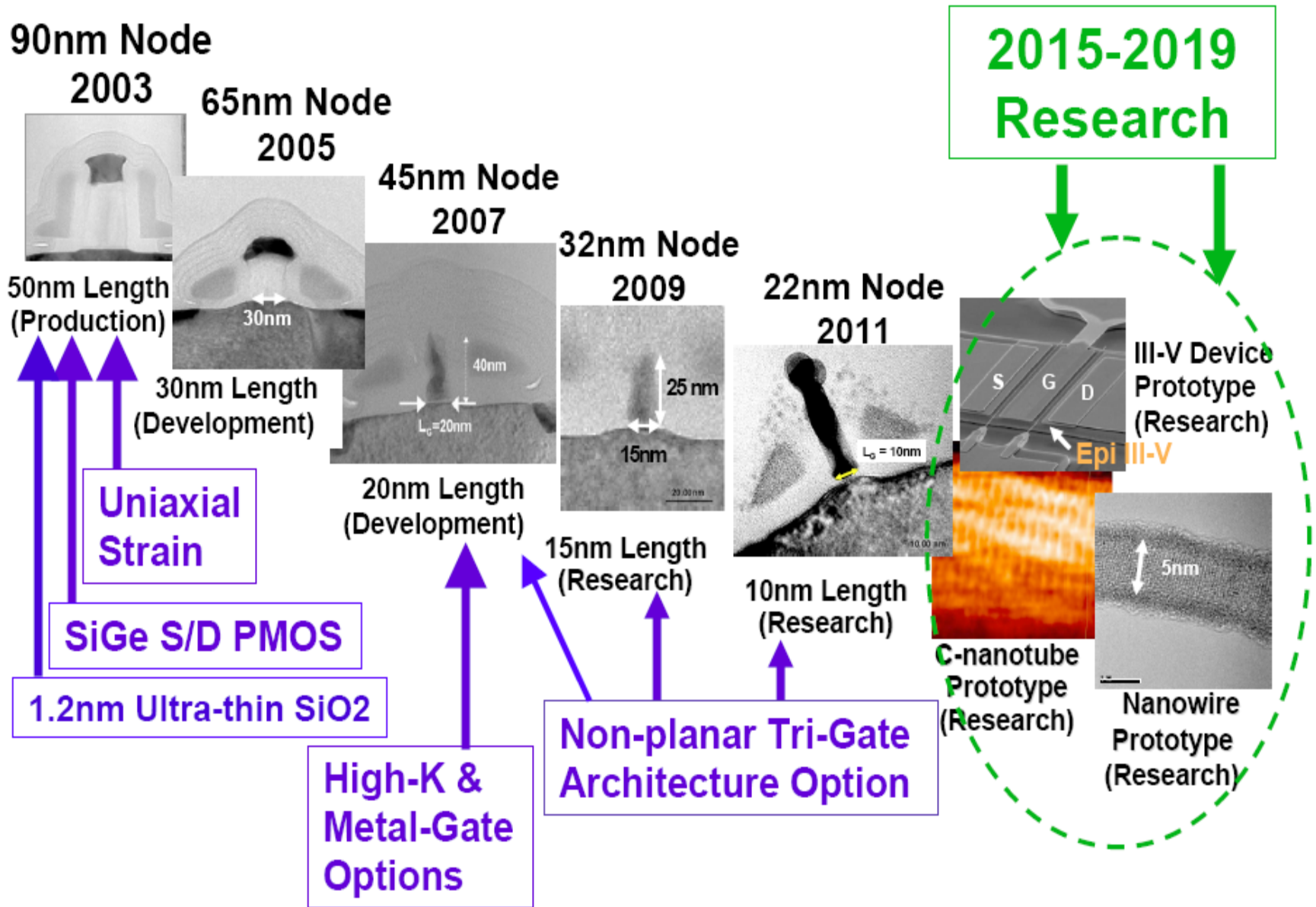
## Research-oriented course

**Learning by reading research articles**

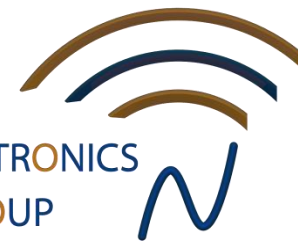
- **Identify key facts from articles**
- **Use commercial simulation tool to identify transistor benefits in circuit**
- **Writing short research article**



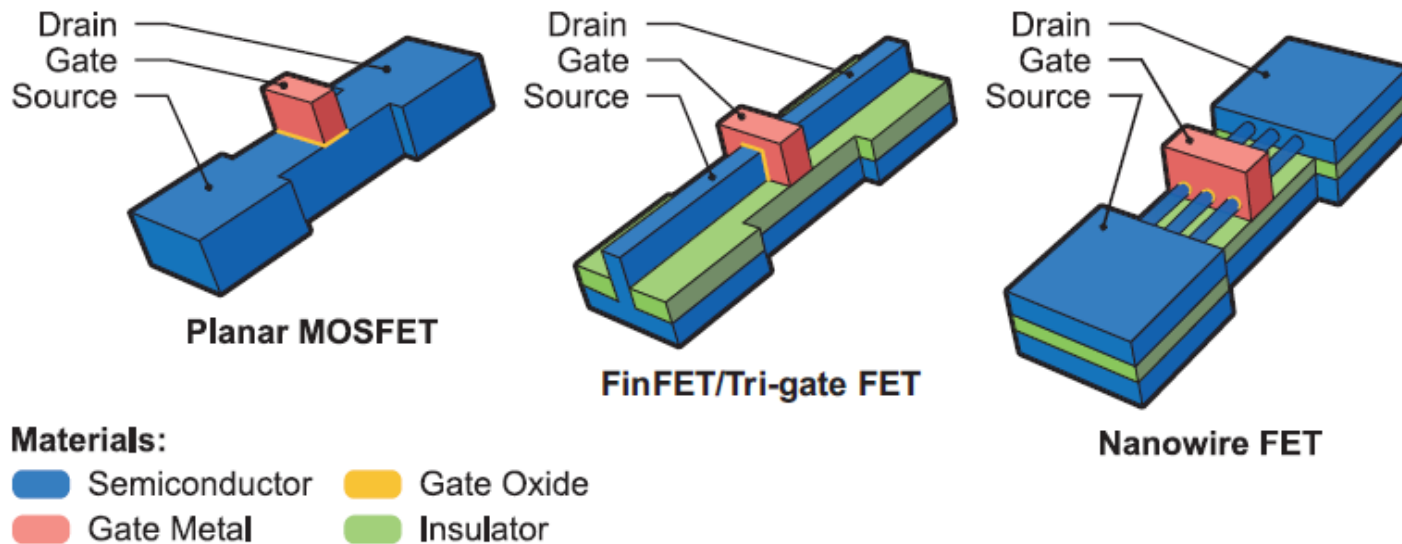
# Transistor Scaling and Research Roadmap



# Current Trends in Device Scaling



Nanowires are a natural extension of the transistor evolution



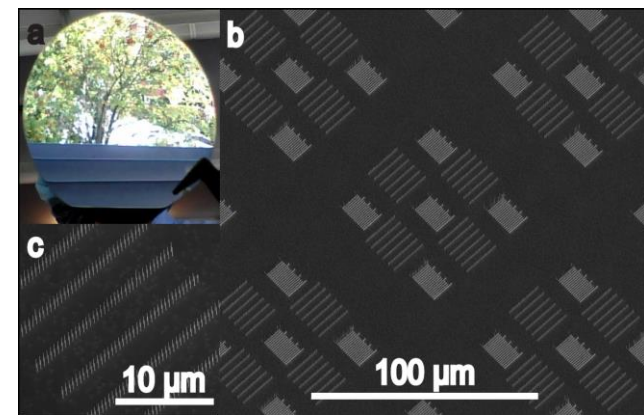
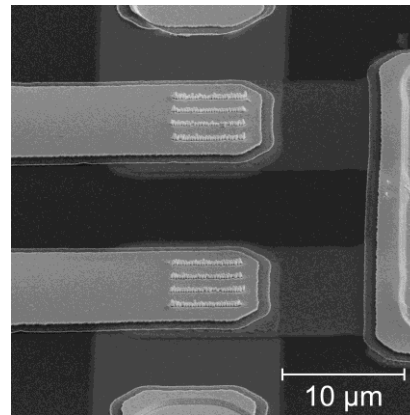
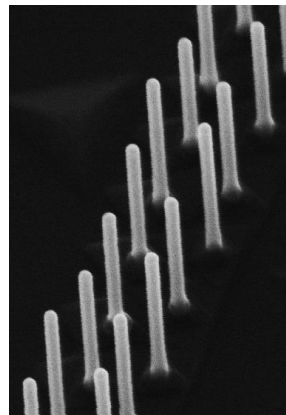
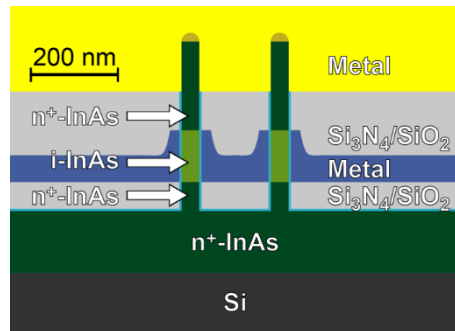
*Riel et al, MRS Bulletin 2014*



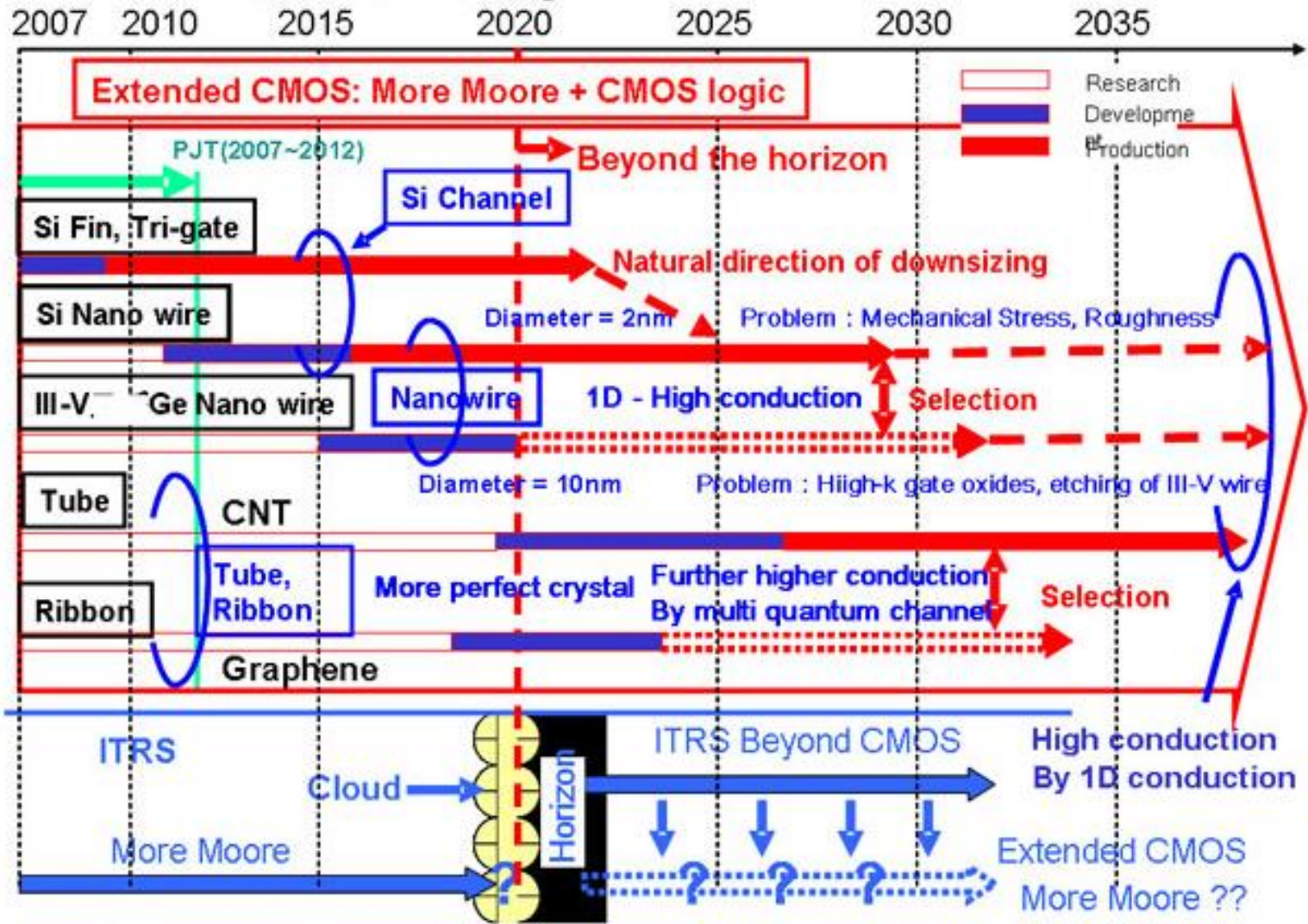
# Why III-V Nanowires

## Why III-V Nanowires?

- Advantageous transport → high transconduc. and  $I_{on}$
- Wrap-gate geometry → low output conduc. and DIBL
- Band gap engineering → increased breakdown, reduced  $I_{off}$
- Small nanowire footprint → reduced defect propagation probability



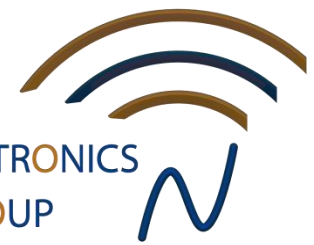
# Our new roadmap



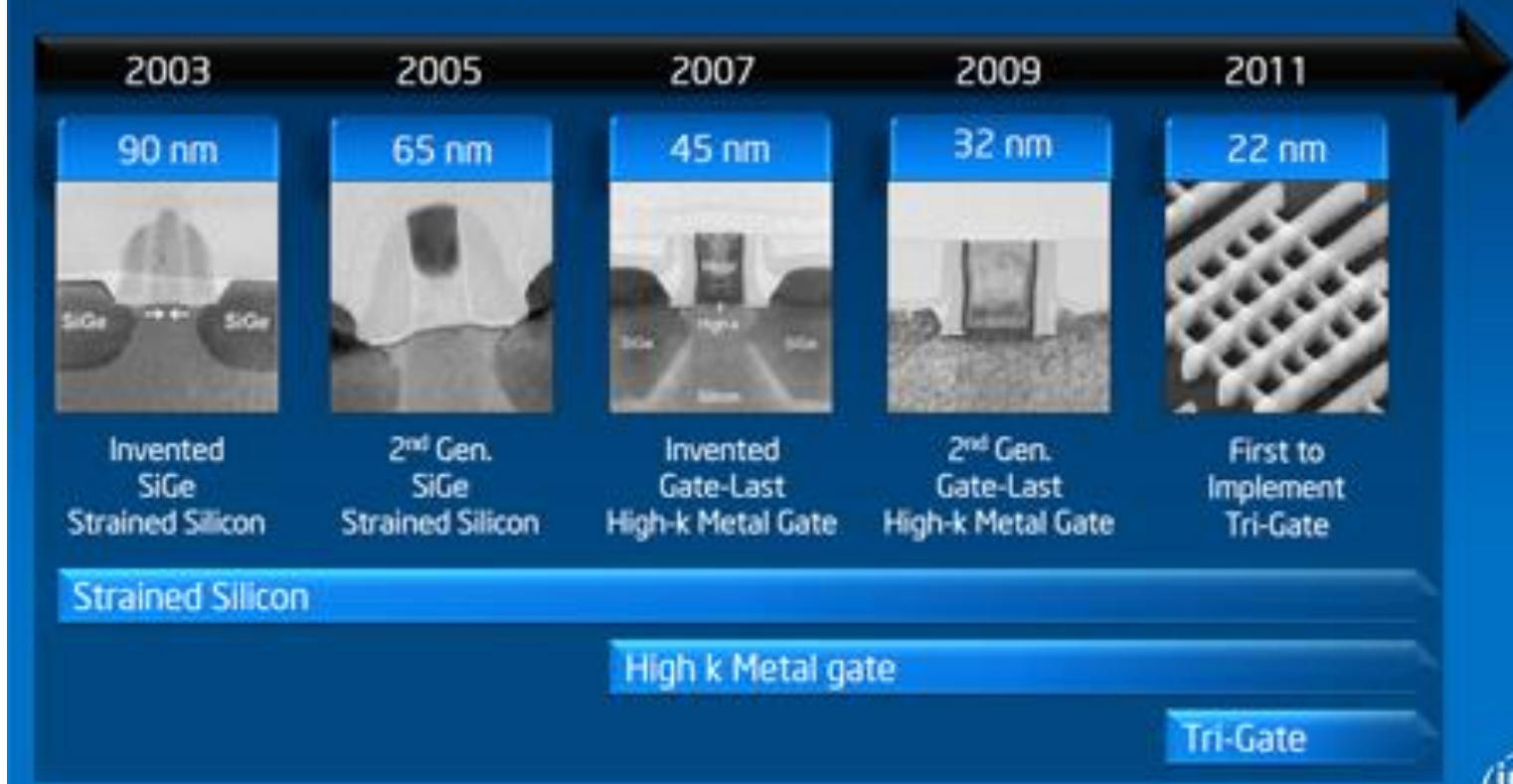
A roadmap from Japan's technical community sees silicon nanowires extending the reach of multi-gate devices.

EXPLORE

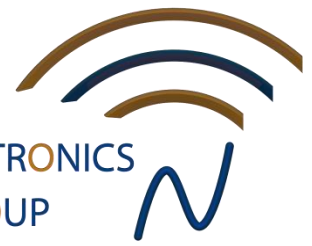
# Current Trends in Device Scaling



## Transistor Innovations Enable Technology Cadence



# Current Trends in Device Scaling

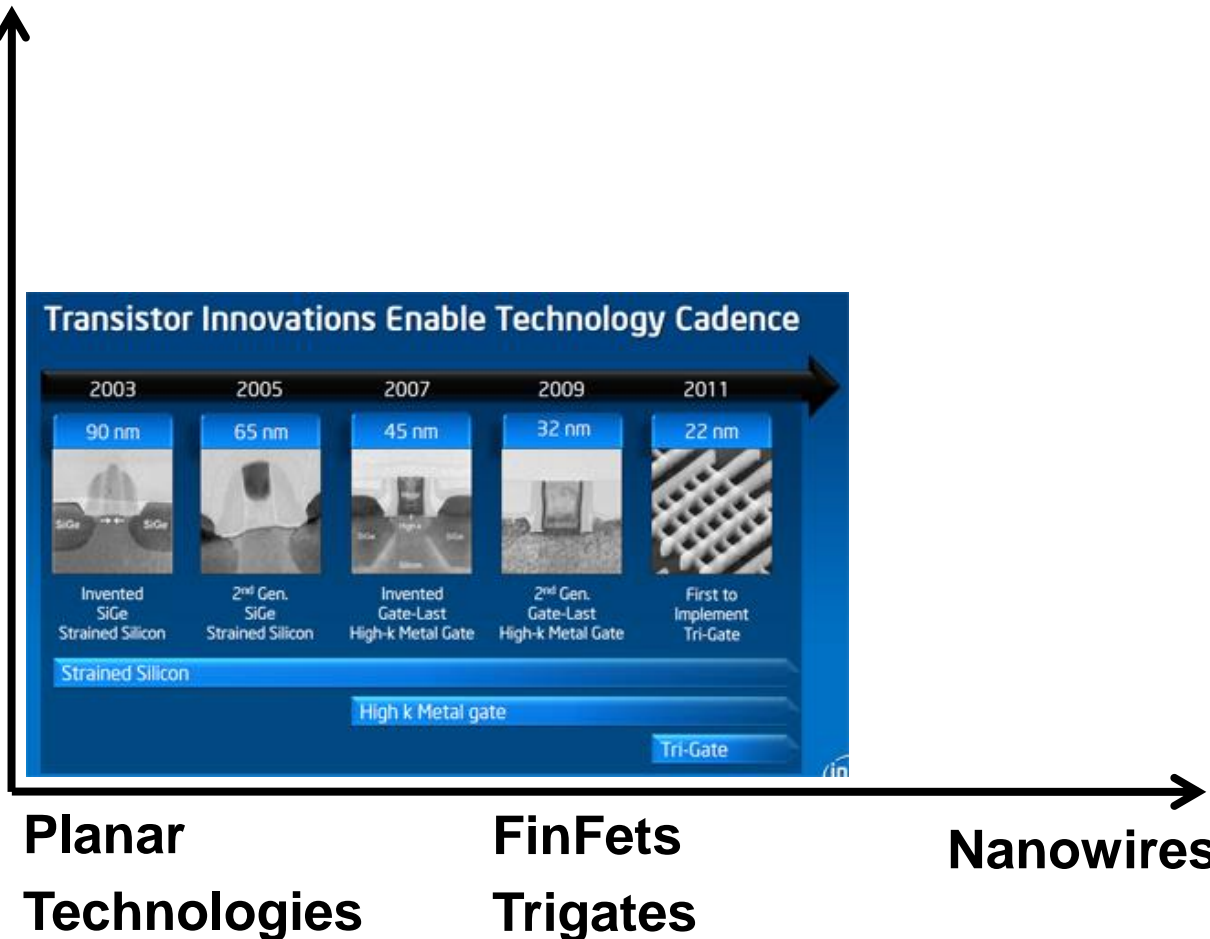


## Transport Enhancement

Graphene

III-Vs

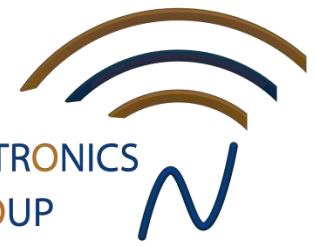
Strained  
Si



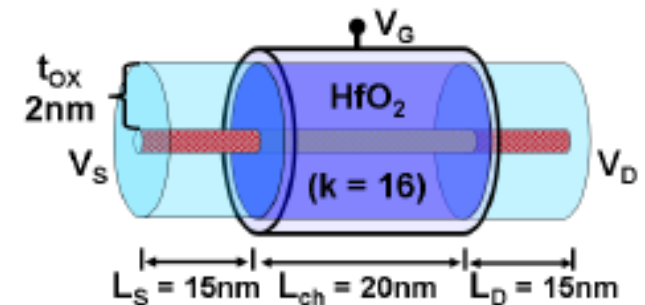
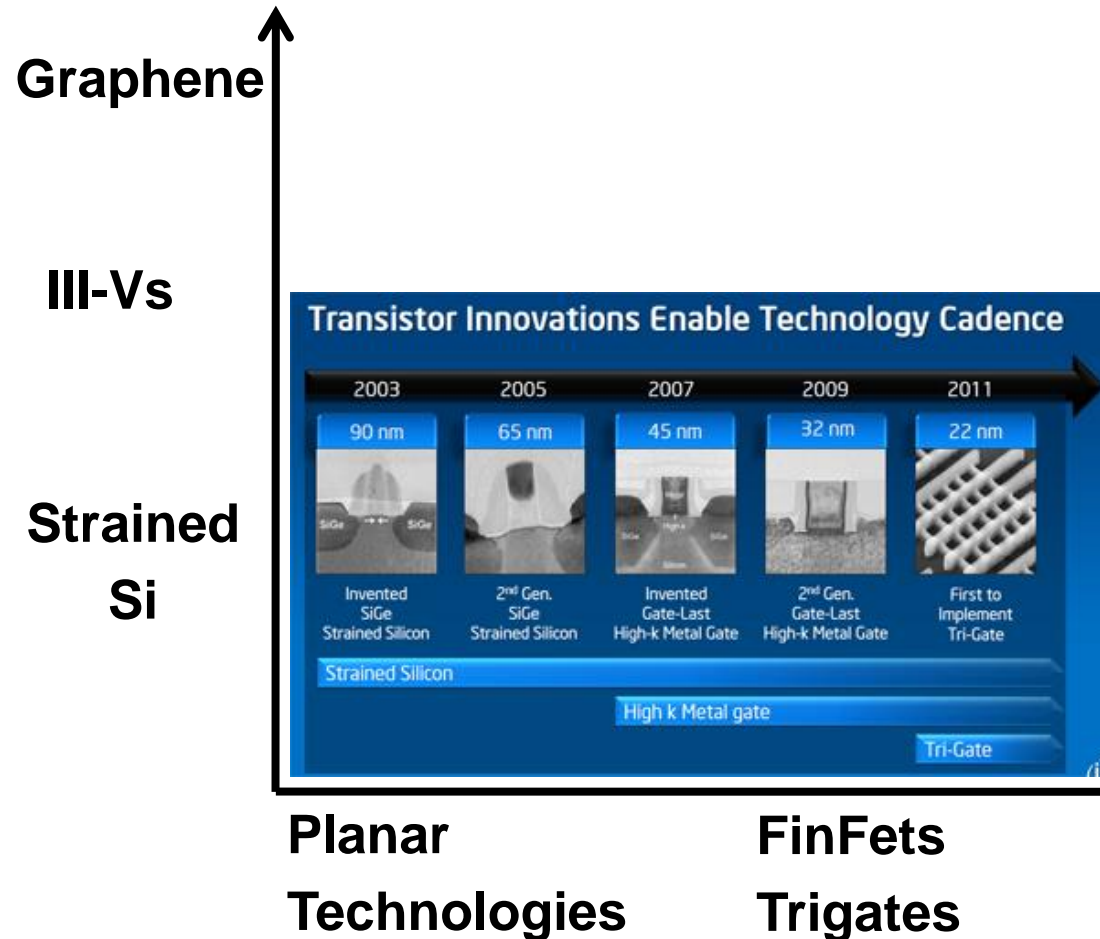
Electrostatics



# Current Trends in Device Scaling



## Transport Enhancement

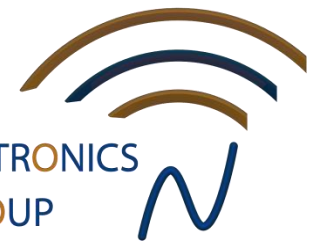


## Electrostatics



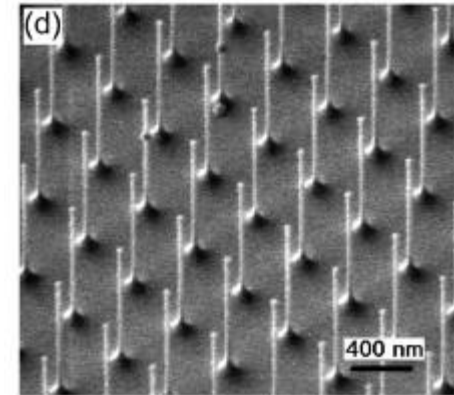
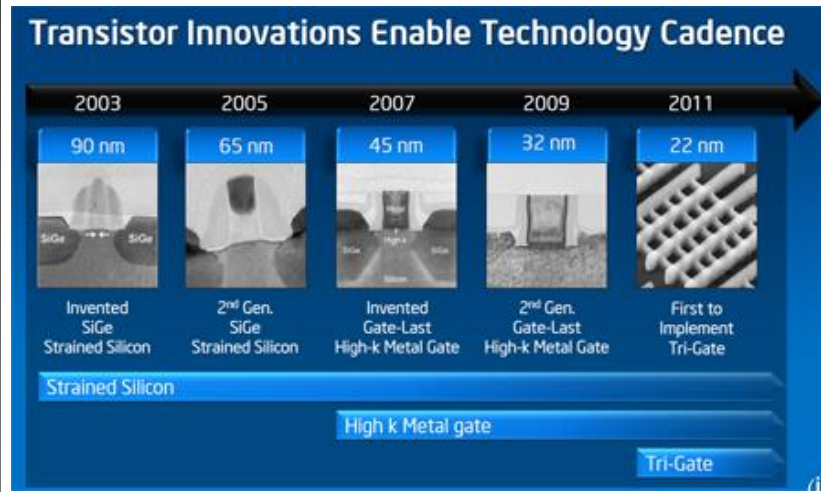


# Current Trends in Device Scaling



## Transport Enhancement

Graphene  
III-Vs  
Strained Si



Planar  
Technologies

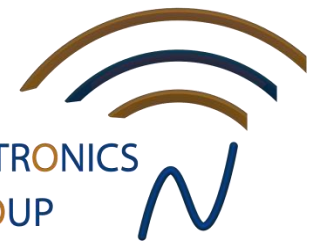
FinFets  
Trigates

Nanowires

Electrostatics



# Current Trends in Device Scaling

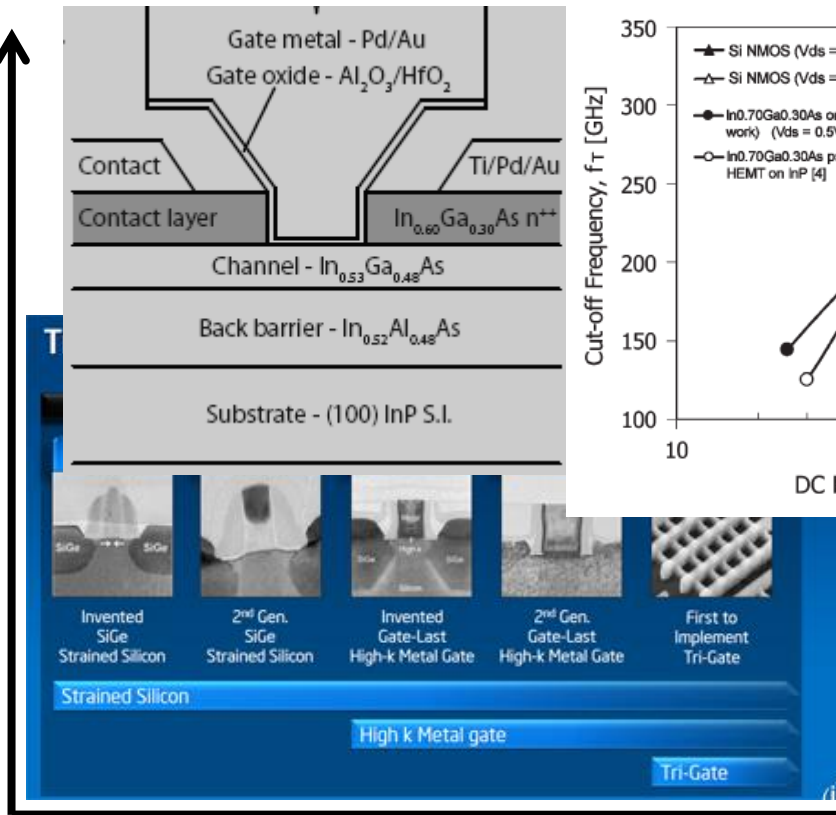


## Transport Enhancement

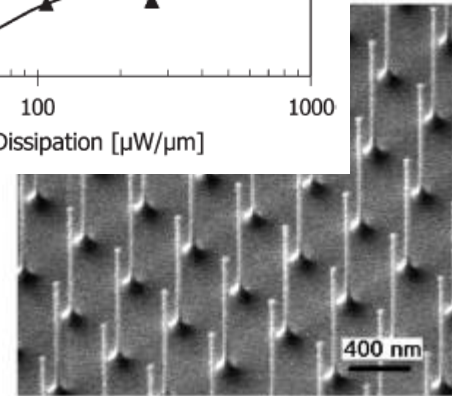
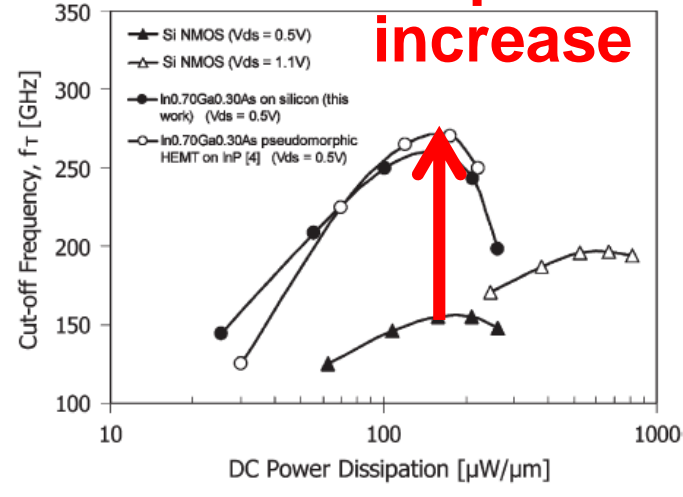
Graphene

III-Vs

Strained  
Si



**X2 performance increase**



**Electrostatics**

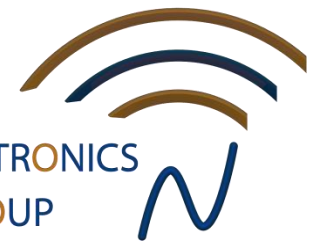
Planar  
Technologies

FinFets  
Trigates

Nanowires



# Current Trends in Device Scaling

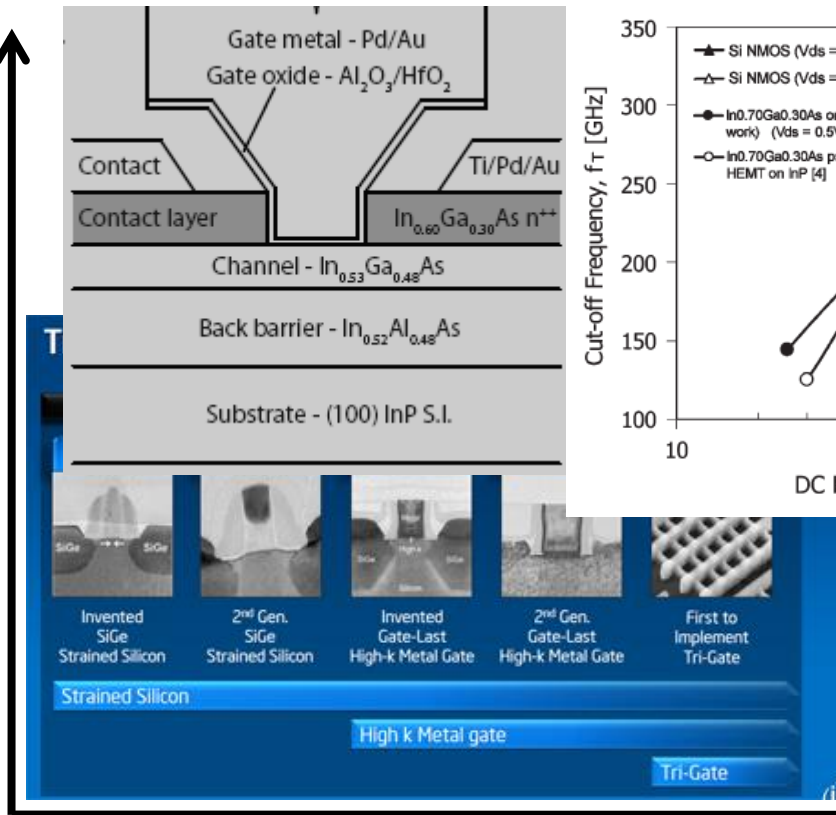


## Transport Enhancement

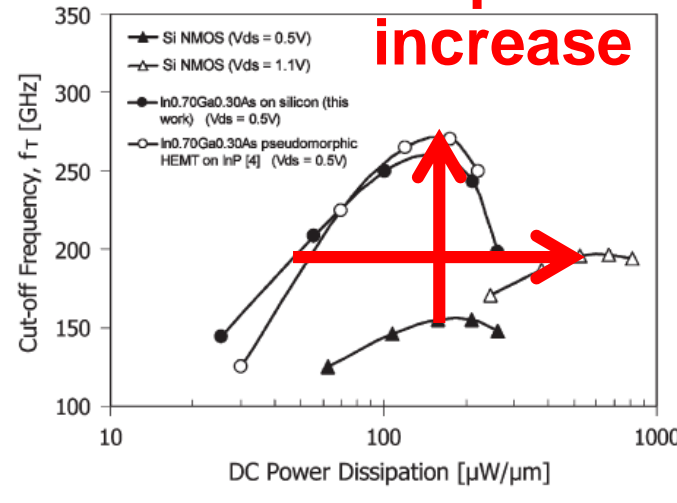
Graphene

III-Vs

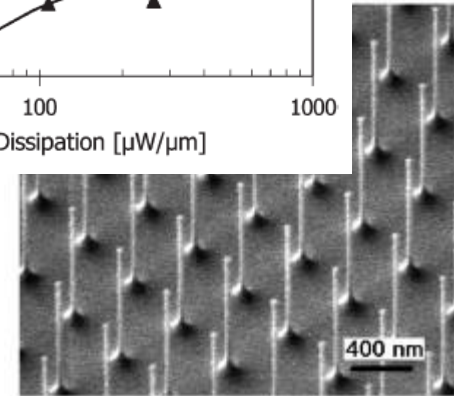
Strained  
Si



**X2 performance increase**



**x10 power increase**



**Electrostatics**

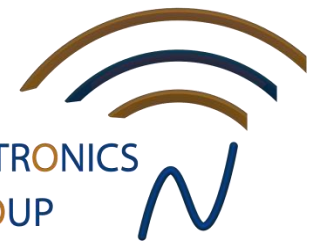
Planar  
Technologies

FinFets  
Trigates

Nanowires



# Current Trends in Device Scaling

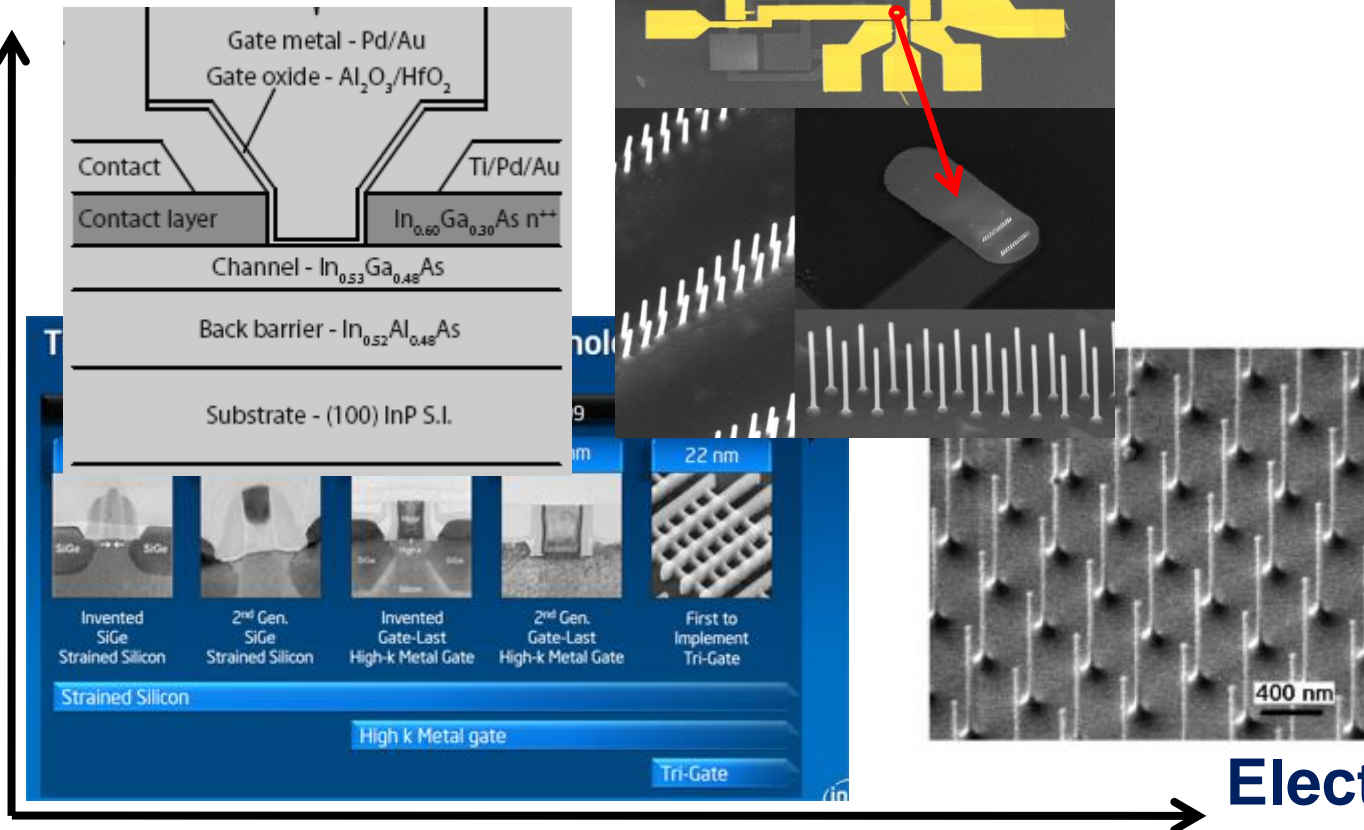


## Transport Enhancement

Graphene

III-Vs

Strained  
Si



Planar  
Technologies

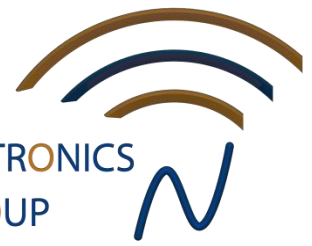
FinFets  
Trigates

Nanowires

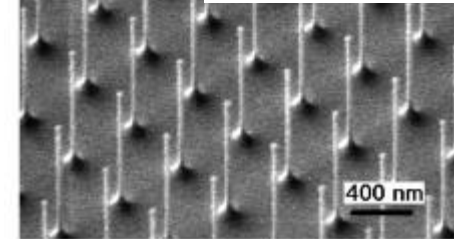
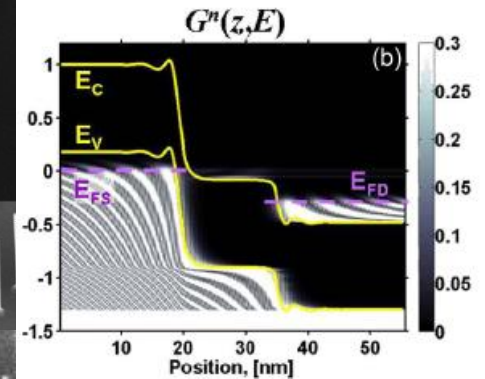
Electrostatics



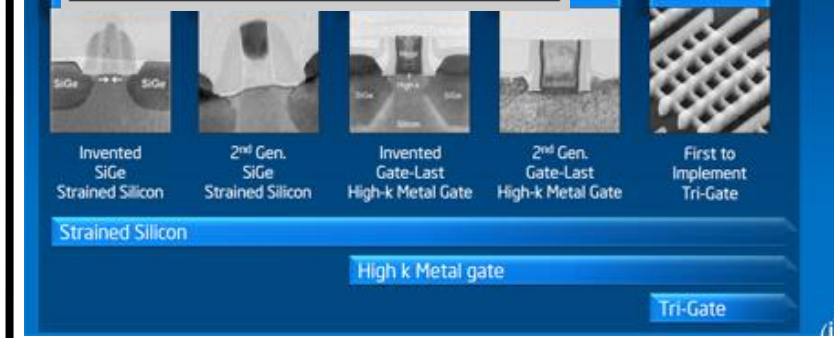
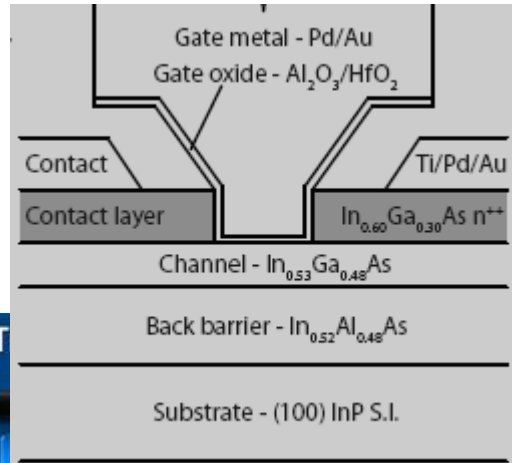
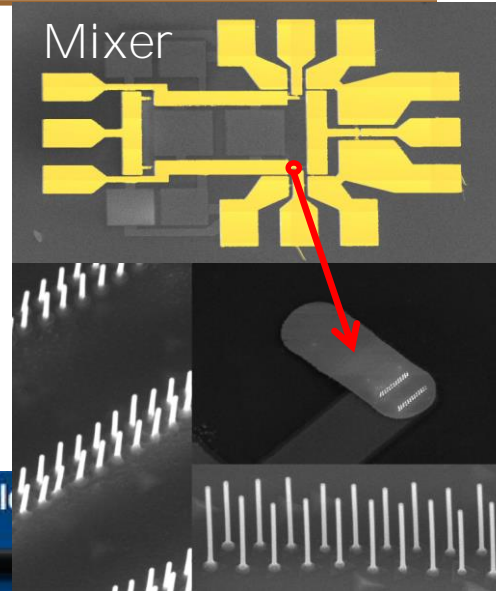
# Current Trends in Device Scaling



More than Moore  
Beyond Moore



Electrostatics



Planar  
Technologies

FinFets  
Trigates

Nanowires

Transport Enhancement

Graphene

III-Vs

Strained  
Si

# What will you learn in this course?

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**How small transistors can we make?**

**How do we compare data for different transistors?**

**What are good numbers for a transistor?**

**What is the relation between the physics, the technology and the performance?**

**What are the ultimate limits in terms of power consumption?**

**What are the benefits of nanotechnology?**

**How can we implement high-speed circuits?**