Lecture 3: III-V CMOS 1

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REVIEW

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Nanometre-scale electronics with III–V compound semiconductors

Jesús A. del Alamo[1]

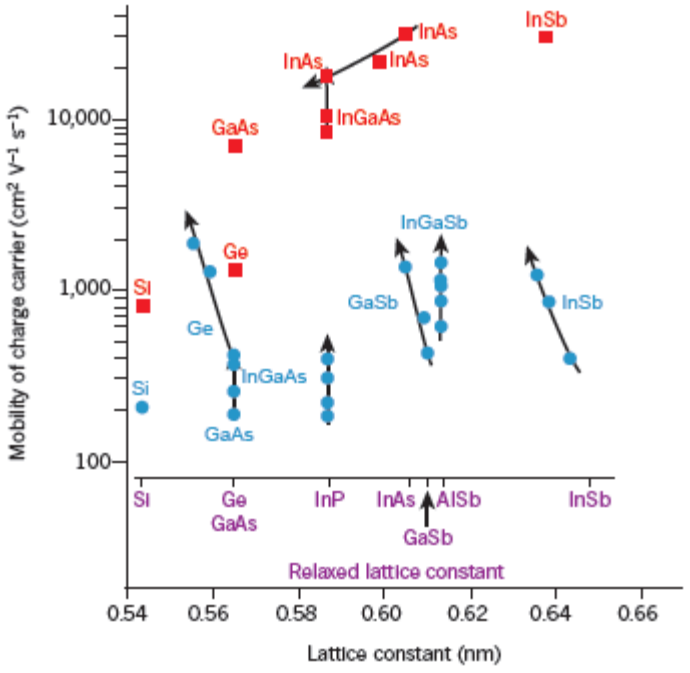
For 50 years the exponential rise in the power of electronics has been fuelled by an increase in the density of silicon complementary metal–oxide–semiconductor (CMOS) transistors and improvements to their logic performance. But silicon transistor scaling is now reaching its limits, threatening to end the microelectronics revolution. Attention is turning to a family of materials that is well placed to address this problem: group III–V compound semiconductors. The outstanding electron transport properties of these materials might be central to the development of the first nanometre-scale logic transistors.

Power-constrained scaling
Need for voltage reduction
With out loss of performance

III-V technology
Manufacturing technology established

Rationale for Using III-Vs

Mobility and Speed are Impressive But not Good numbers



We should look at the injection velocity

$$I_{On} = qn_s v_{inj}$$

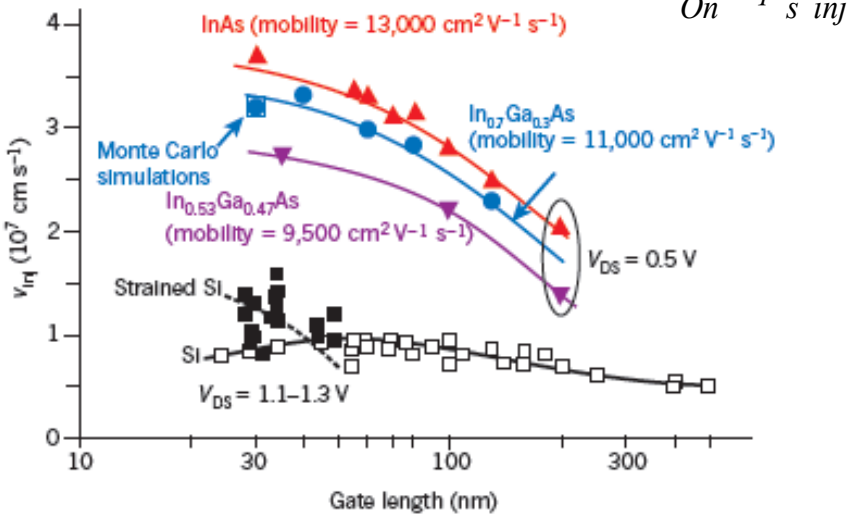


Figure 2 | Electron injection velocity in III–V HEMTs. Electron injection velocity, v_{inj}, is shown for InGaAs and InAs HEMTs with different channel compositions and for silicon MOSFETs as a function of gate length[13,14]. The III–V HEMTs are measured at a drain–source voltage (V_{DS}) of 0.5 V, the silicon MOSFETs at a V_{DS} of 1.1–1.3 V. Despite this discrepancy in voltage, the injection velocity of InGaAs channels is more than twice that of the silicon MOSFETs. The saturation tendency of the injection velocity of InGaAs channels suggests that ballistic (collision-free) transport is occurring; this is confirmed by ballistic Monte Carlo simulations that fall right on the experimental point[15].

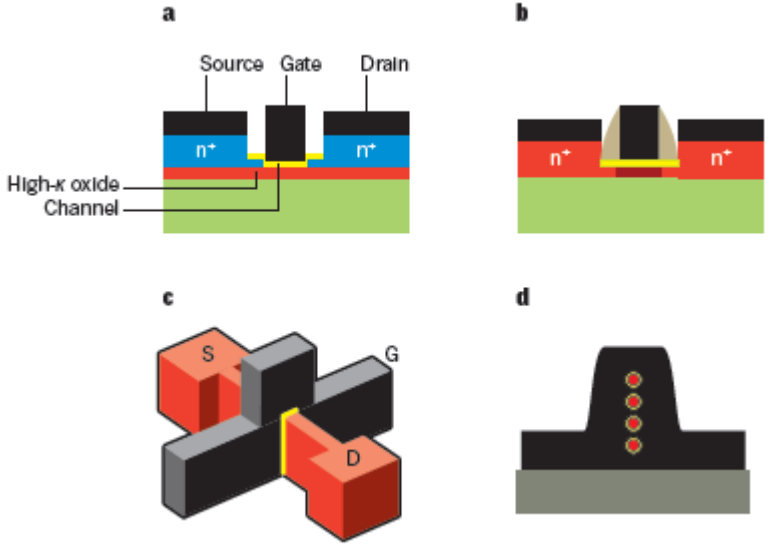
Issues

The gate stack: **Interface states, surface pinning, ALD**

Self-aligned transistor design: **Planar, TriGates, Nanowires**

The p-type MOSFET: **Technology boosters like strain**

Co-integration of NMOS and PMOS transistors on Si:
Epitaxial techniques with buffer layers, Wafer bonding, Hetero-integration



The Perspective

But we need low off-currents as well!!!

I_{off} fixed at 100 nA/μm

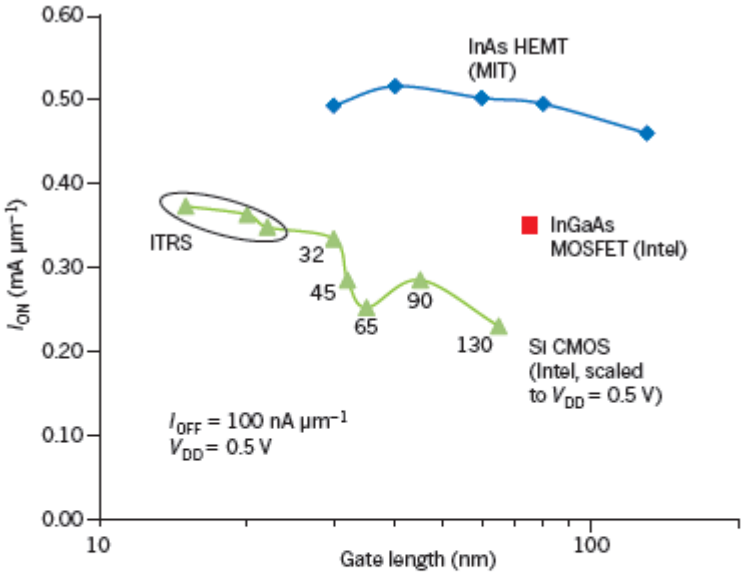
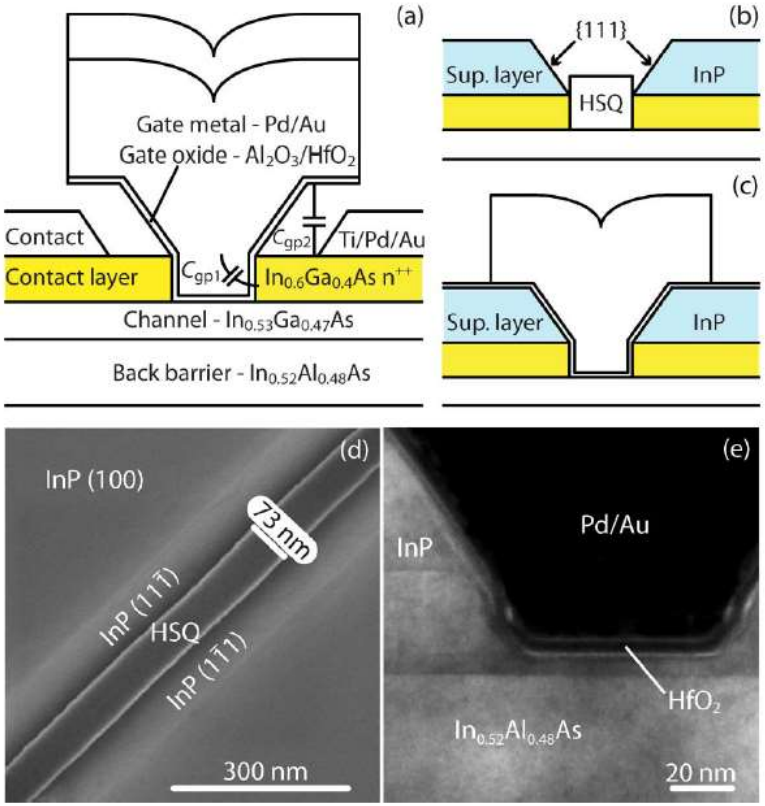


Figure 3 | High 'on' currents in III–V HEMTs. The graph shows how 'on' current, I_{ON}, varies with gate length for InAs HEMTs and silicon MOSFETs at 0.5 V for a fixed 'off' current of 100 nA μm^{-1}. The silicon data correspond to 0.5 V and are obtained from models of published experimental data at higher voltages[12]. The data points labelled ITRS represent projections for future scaling from the *International Technology Roadmap for Semiconductors*[7]. The red square corresponds to an InGaAs MOSFET[59]; the fact that it already exceeds the performance of silicon MOSFETs at 0.5 V is very encouraging. MIT, Massachusetts Institute of Technology. Image modified, with permission from ref. 13.

IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 3, MARCH 2012 369

High-Frequency Performance of Self-Aligned Gate-Last Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFET

Mikael Egard, Lars Ohlsson, Mats Ärlelid, Karl-Magnus Persson, B. Mattias Borg, Filip Lenrick, Reine Wallenberg, Erik Lind, and Lars-Erik Wernersson



First demonstration of:

III-V gate-last technology with replacement gate

Epitaxial regrowth of contacts

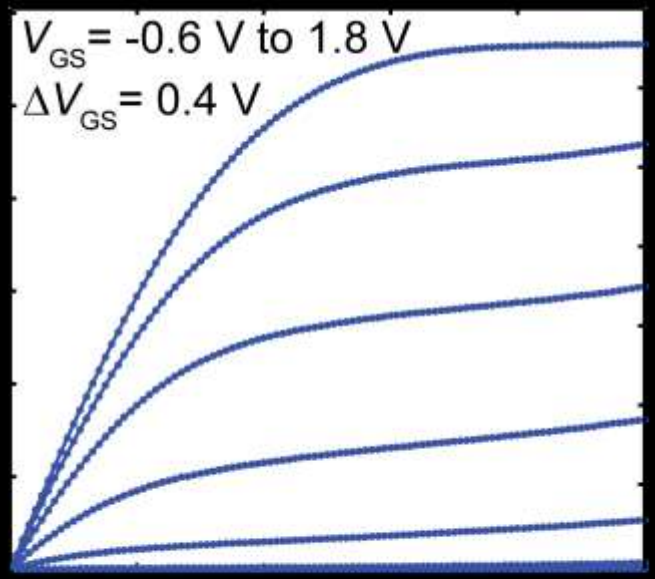
Self-aligned technology

Very good performance

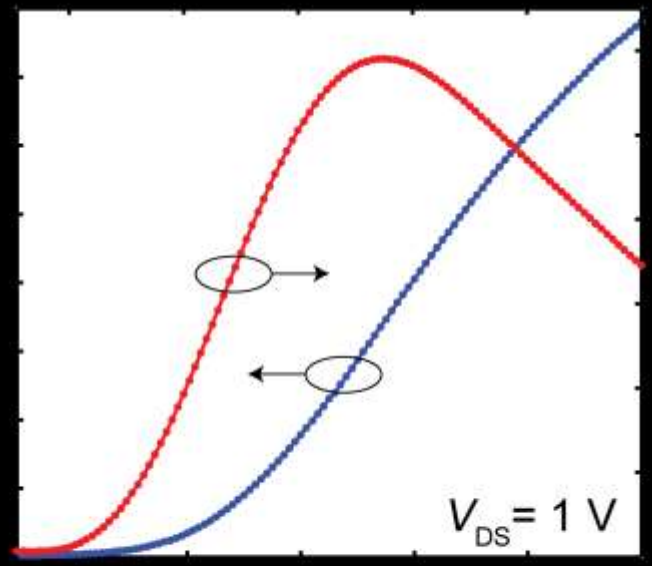
Process flow important

DC Characterization L_g=140 nm

Output characteristics



Transfer characteristics

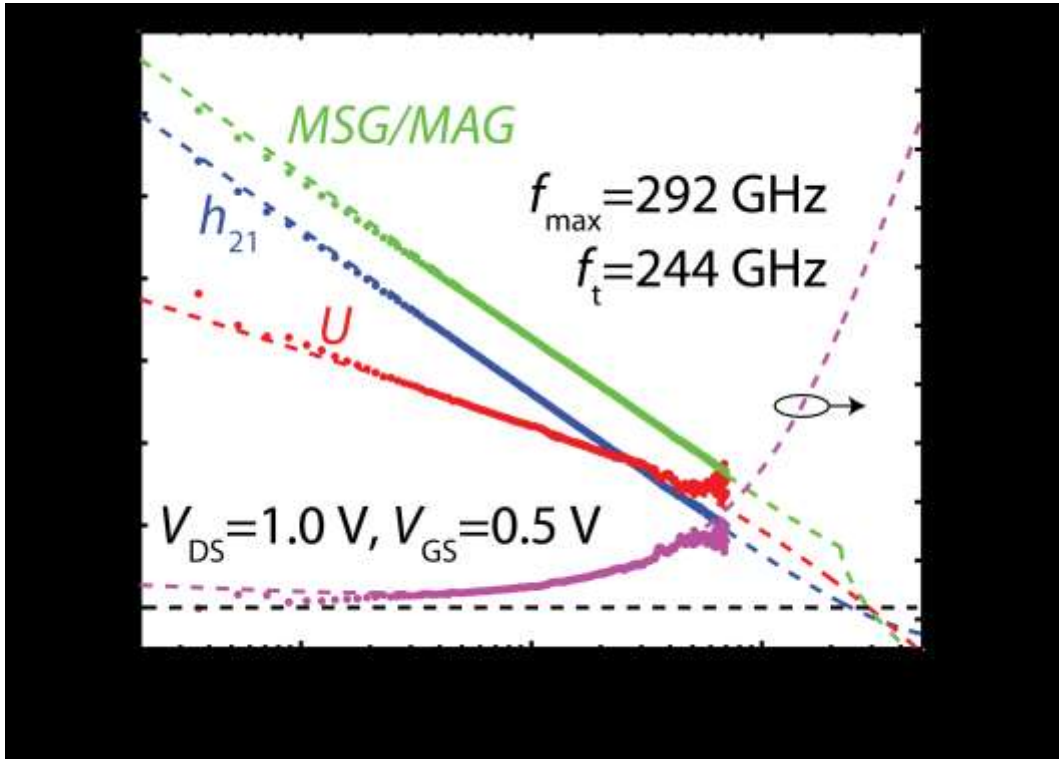


R_{on}=265 Ωμm, max I_d=1.3 mA/μm, max g_m=1.2 mS/μm

- Low access resistance enables high drive current
- Enhancement mode operation

S-parameter Characterization

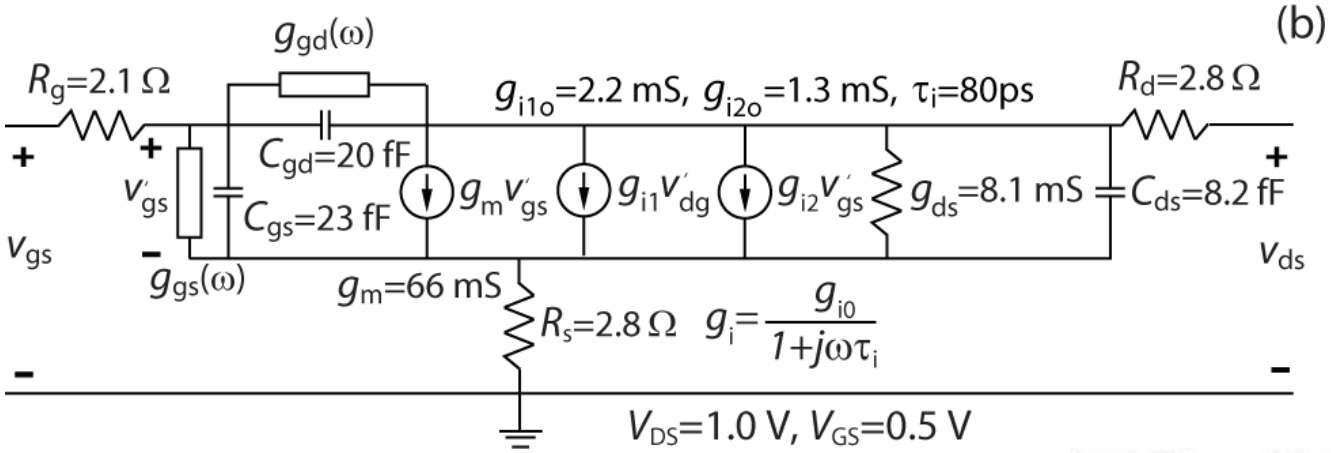
- L_g=55 nm, W_g=21.6 μm device characterized to 70 GHz
- Modeling accounts for impact ionization and border traps



Egard et al IEEE EDL 2012

S-parameter Characterization

Small-signal model includes effects related to impact ionization, band-to-band tunneling and conduction via border traps



C_{gd1}=7.2fF

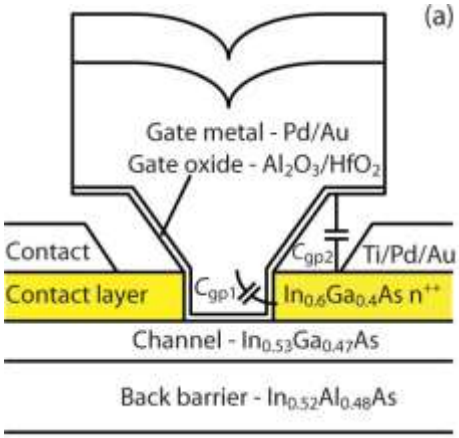
C_{gd2}=19 fF

g_{mint}=3.0 mS/μm

Frequency dependent g_m!

Border traps 9x10^{19} cm^{-3}

Johansson et al IEEE T-ED 2012



MOS-HEMT

High-Speed E-Mode InAs QW MOSFETs With Al_2O_3 Insulator for Future RF Applications

Dae-Hyun Kim, Tae-Woo Kim, Richard J. W. Hill, Chadwin D. Young, Chang Yong Kang, Chris Hobbs, Paul Kirsch, Jesus A. del Alamo, and Raj Jammy

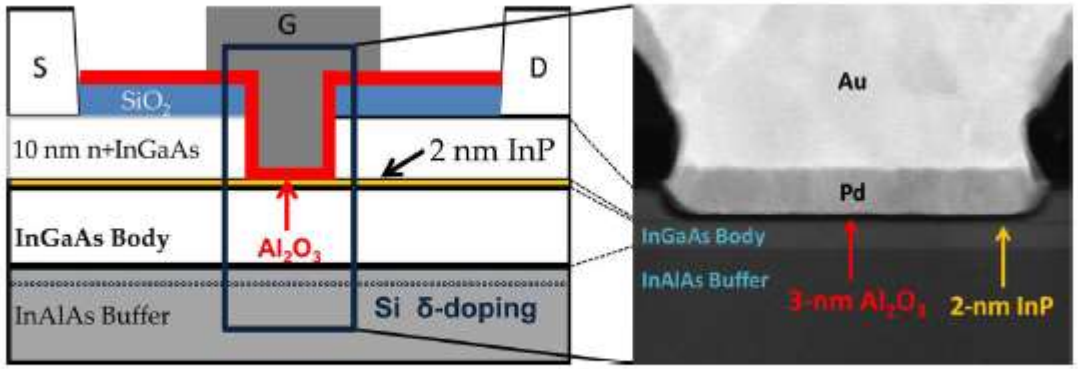


Fig. 1. (Left) Device schematic and (right) TEM image for the cross section of 100-nm InAs MOSFETs with $Al_2O_3 = 3$ nm.

Much like a HEMT, but with an oxide!

DC and RF characteristics

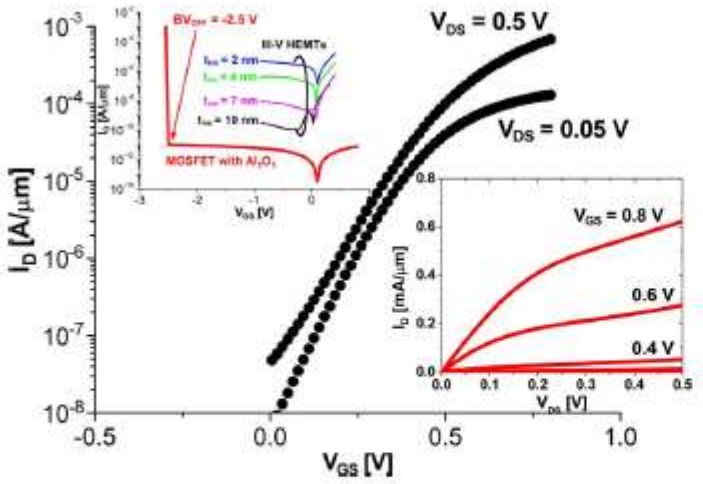


Fig. 2. DC subthreshold characteristics of $L_g = 100$ nm InAs MOSFETs. Inset on the right shows I_G against V_{GS} for InAs MOSFET with Al_2O_3 and III–V HEMTs with various values of t_{ins}. Inset on the left shows output characteristics.

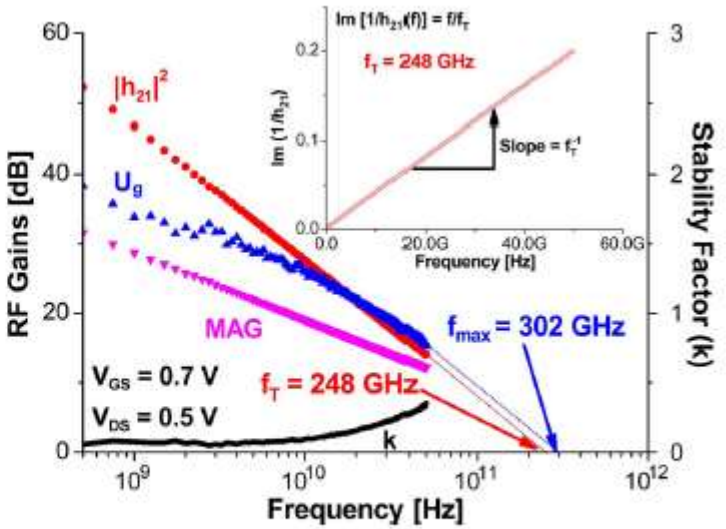


Fig. 3. $|h_{21}|^2$, Mason's unilateral gain U_g, and MAG, against frequency for $L_g = 100$ nm InAs MOSFETs at $V_{GS} = 0.7$ V and $V_{DS} = 0.5$ V. Inset shows f_T extraction by Gummel's approach [11].

Resistances

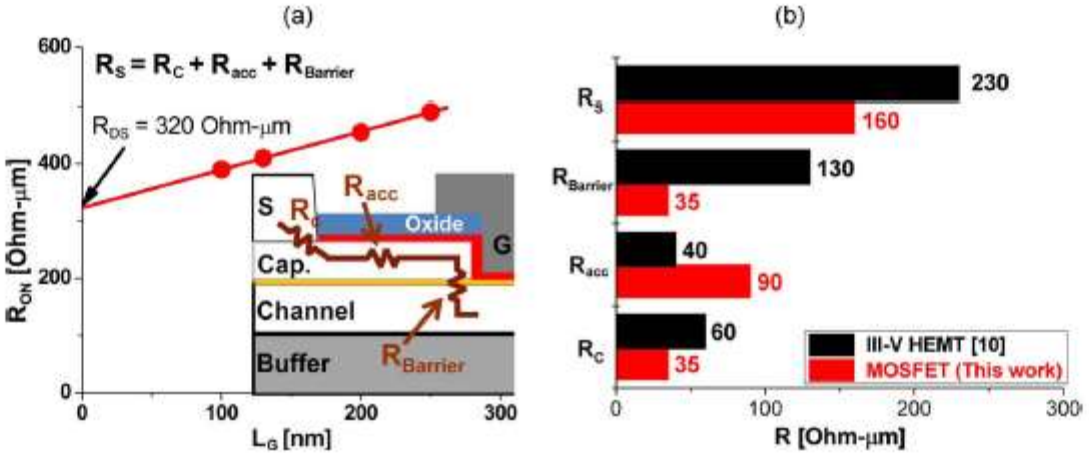


Fig. 4. (a) R_{ON} as a function of L_g for our InAs MOSFETs and (inset) simple model for R_s and (b) extracted components for R_s which arise from TLM and R_{ON} analysis.

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Is interfacial chemistry correlated to gap states for high-k/III–V interfaces?

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ALD critical for III-V MOS structures

Alternative cycles of metal and oxide

Has self cleaning effect

Reaction at interface detected by XPS

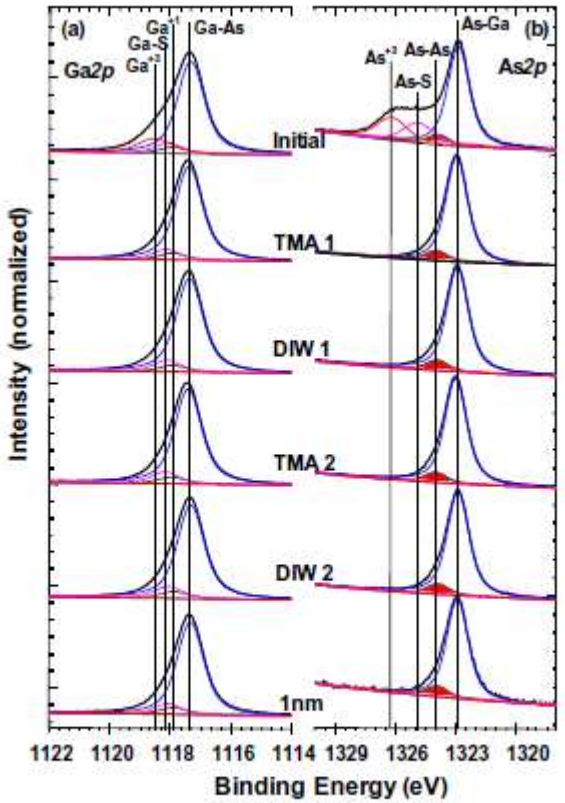

Fig. 4. *In situ* half-cycle ALD study of S-passivated GaAs showing (a) Ga 2p and (b) As 2p regions. The As-shaded feature corresponds to As–As bonding. Reprinted with permission from [28], © 2008, American institute of physics.

Correlation between XPS and CV

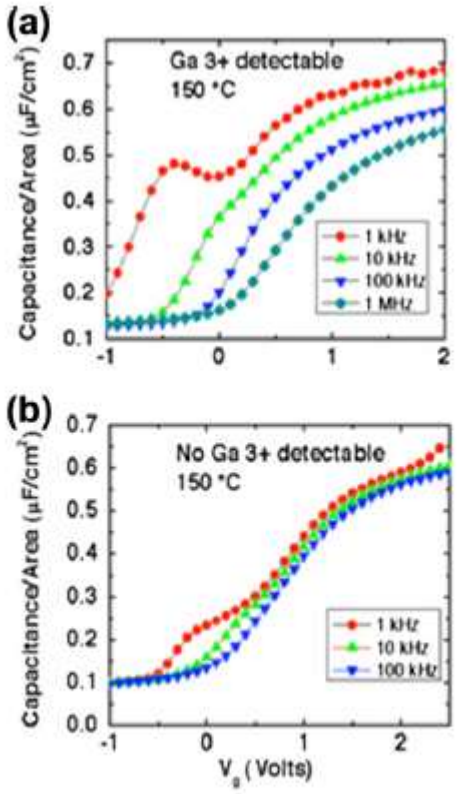

Fig. 1. *C–V* analysis at 150 °C for MOS capacitors consisting of (a) 10 nm Al_2O_3/GaAs(1 0 0) and (b) 10 nm Al_2O_3/Si/GaAs(1 0 0). Reprinted with permission from [28], © 2008, American Institute of physics..

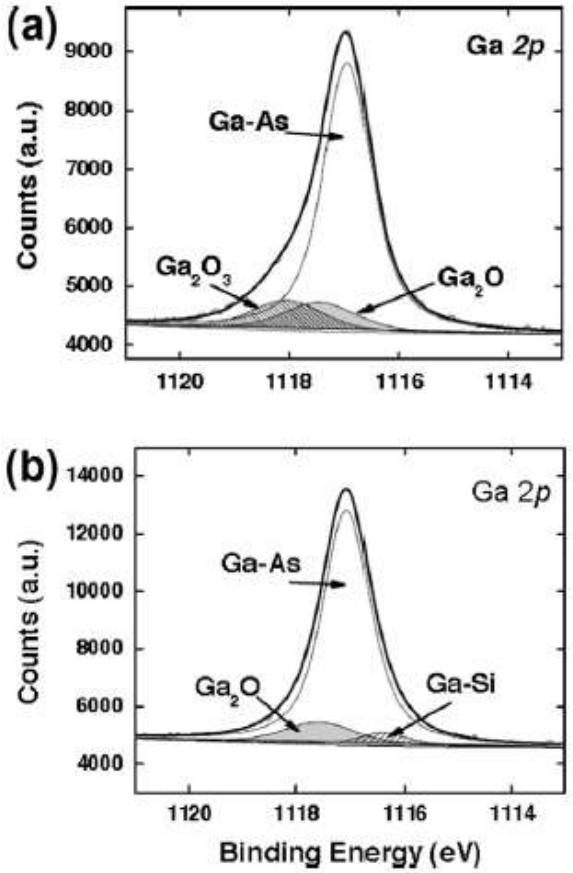

Fig. 2. Corresponding XPS spectra for Fig. 1 for ~1 nm Al_2O_3 (a) directly on HF-last GaAs(1 0 0) and (b) on Si interfacial layer on GaAs(1 0 0). Reprinted with permission from [28], © 2008, American Institute of physics..

The Bad Guys

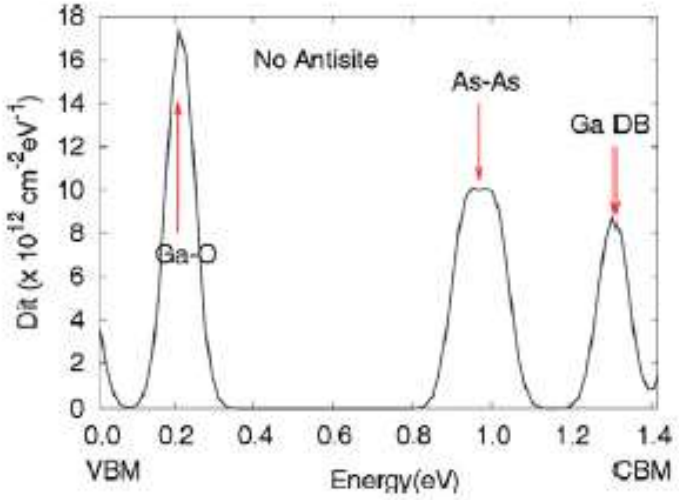

Fig. 6. Density of states calculated from the O-rich HfO_2/GaAs interface. The As–As dimer defect is seen to result in a significant density near the midgap, while Ga db and "Ga +3-like" states contribute near the band edges.

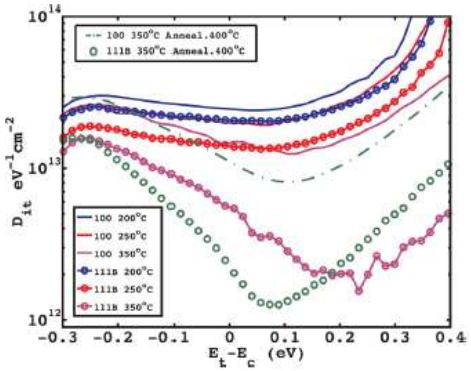

FIG. 2. D_{it} vs. E_t - E_c extracted using the low frequency fitting method (see Ref. 14) as a function of InAs orientation and oxide deposition temperature. The x-axis denotes the position of the trap level E_t in the band gap with respected to the conduction band edge E_c.

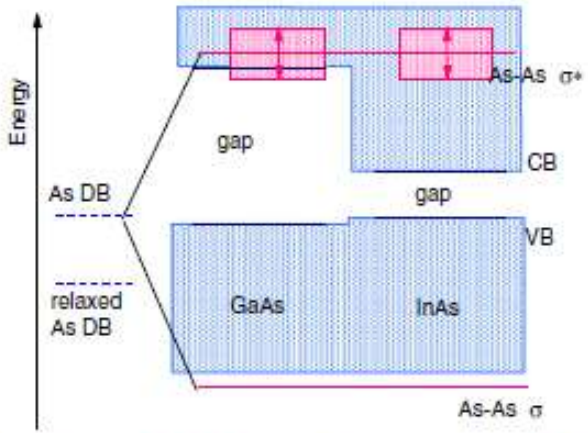

Fig. 4. Creation of bonding and antibonding states (σ and σ*) from As–As bonds, related to the band energies.

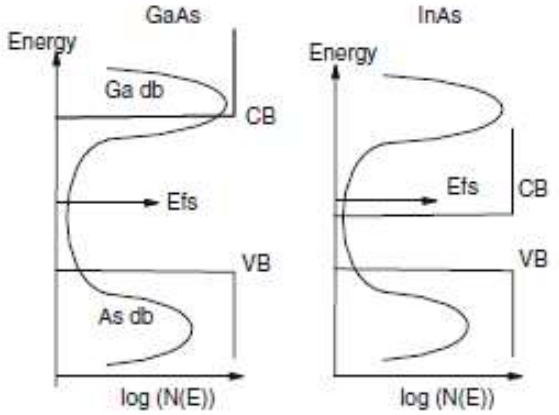

Fig. 5. Schematic of the density of interface states for GaAs and InAs, compared to the bulk band states, and their charge neutrality levels (CNL)/Fermi level stabilisation energies.

N S