Lecture 4: III-V CMOS II

Contents:

III-V CMOS I:
J Nah et al Nano Lett. 12 2012, p. 3592 ”III- V Complementary ...”

III-V CMOS II:
S Takagi et al IEEE IEDM Tech Digest. 2012, p. 505 ”MOS interface and channel ... ”

III-V CMOS III:
J. Svensson et al Nano Letters 15, 2015, p. 7898 ” III−V Nanowire Complimentary…”

III-V Nanowires CMOS:
A. Jönsson et al IEEE EDL, 39, 2018, p. 935” A Self-Aligned Gate-Last Process Applied ...”

III-V Nanowires:
K. Tomioka et al Nature ” 488, 2012, p. 2012 A III–V nanowire channel on silicon ...”

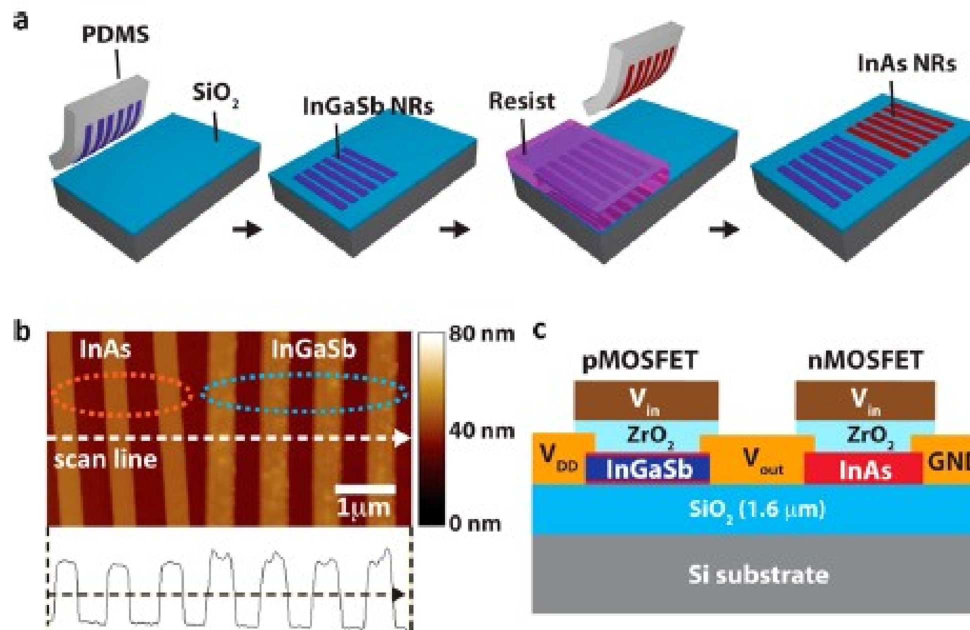
NANO LETTERS

Letter

pubs.acs.org/NanoLett

III–V Complementary Metal–Oxide–Semiconductor Electronics on Silicon Substrates

Junghyo Nah,[†,‡,§,∥,⊥] Hui Fang,[†,‡,§,⊥] Chuan Wang,[†,‡,§] Kuniharu Takei,[†,‡,§] Min Hyung Lee,[†,‡,§,#] E. Plis,[○] Sanjay Krishna,[○] and Ali Javey[†,‡,§,*]



InAs/InGaSb Heterostructure:

Surface passivation

Non-doped ohmic contact formation

Provide strain to enhance mobility

Figure 1. III–V XOI CMOS. (a) Process schematic for the heterogeneous integration of InAs and InAs/InGaSb/InSb XOI on a Si/SiO_2 substrate. (b) Atomic force micrograph of transferred InAs and InAs/InGaSb/InAs NRs, located adjacently. (c) Schematic representation of a top-gated CMOS inverter with InAs (n-type) and InGaSb (p-type) active layers, having 10 nm of ZrO_2 as the top-gate dielectric.

Electrical Characteristics

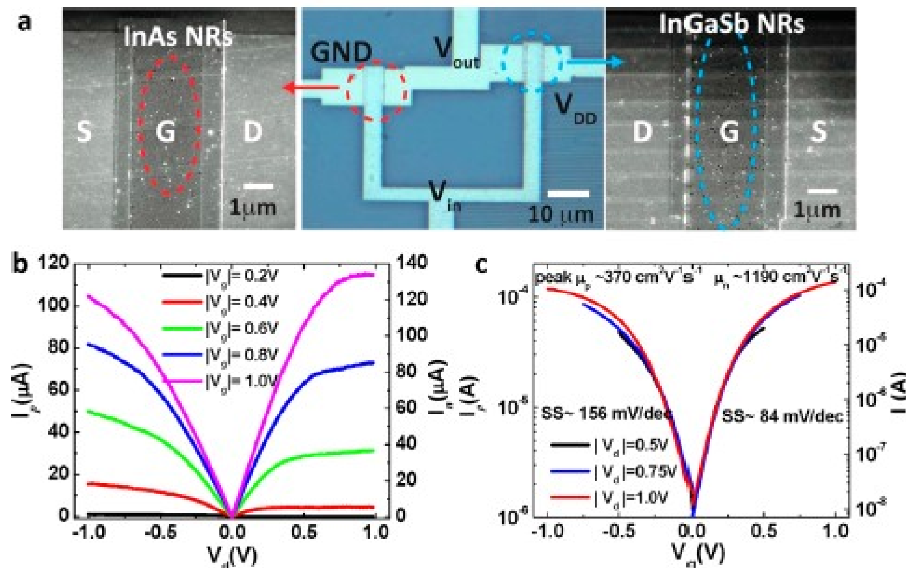


Figure 2. Performance of *p*- and *n*-type XOI MOSFETs. (a) Optical image (center) of a fabricated III−V CMOS inverter and the corresponding SEM images of each channel region (left: InAs; right: InAs/InGaSb/InAs). (b) Output and (c) transfer characteristics of *p*- (left axis) and *n*- (right axis) MOSFETs.

InAs: 3 nanoribbons
340 nm L_g
μ 1190 cm^2/Vs
SS 84 mV/dec

InGaSb: 9 nanoribbons
200 nm L_g
μ 370 cm^2/Vs
SS 156 mV/dec

Circuits

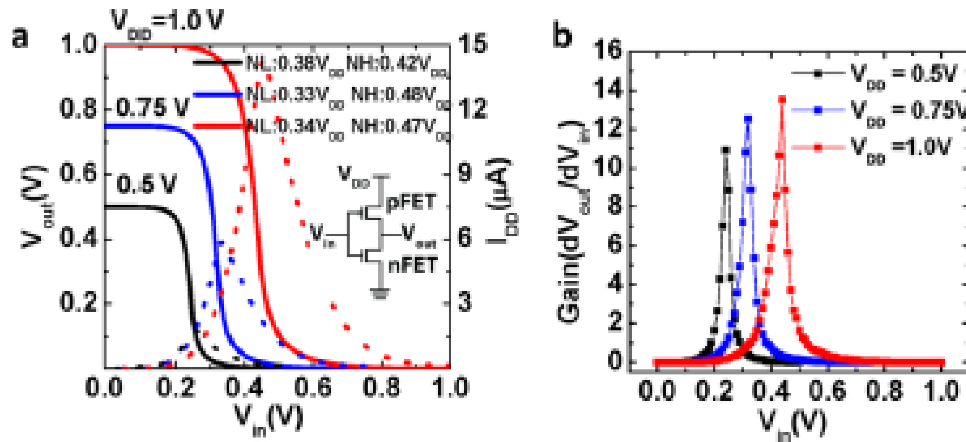


Figure 3. III–V CMOS inverter. (a) Transfer characteristics of a CMOS inverter, measured at different supply voltages (V_{DD}). Inset shows the circuit diagram for the fabricated inverter. (b) Inverter gain (dV_{out}/dV_{in}) dependence on the input voltage.

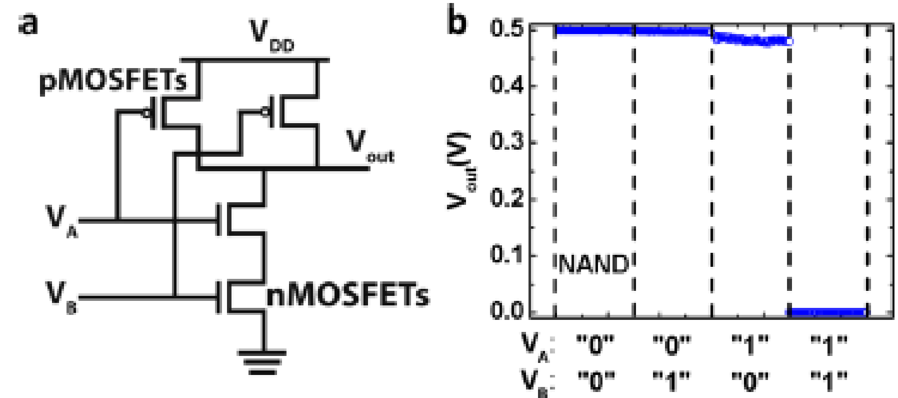


Figure 4. III–V CMOS NAND logic gate. (a) Circuit schematic of a CMOS NAND gate. The circuit is designed by connecting two p-MOSFETs in parallel and two n-MOSFETs in series. (b) Output voltage V_{out} for four different combinations of input states "0 0", "0 1", "1 0", and "1 1". The output is in the "low-state" only if the inputs are "1 1". Note: Input voltages of +0.5 and −0.5 V are treated as logic "1" and "0", respectively. The supply voltage (V_{DD}) for the circuit is 0.5 V.

MOS interface and channel engineering for high-mobility Ge/III-V CMOS

S. Takagi, R. Zhang, S.-H Kim, N. Taoka, M. Yokoyama, J.-K. Suh, R. Suzuki and M. Takenaka
The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-8656, Japan
Tel/Fax: +81-3-5841-0419, Email: takagi@ee.t.u-tokyo.ac.jp

IEDM12-505

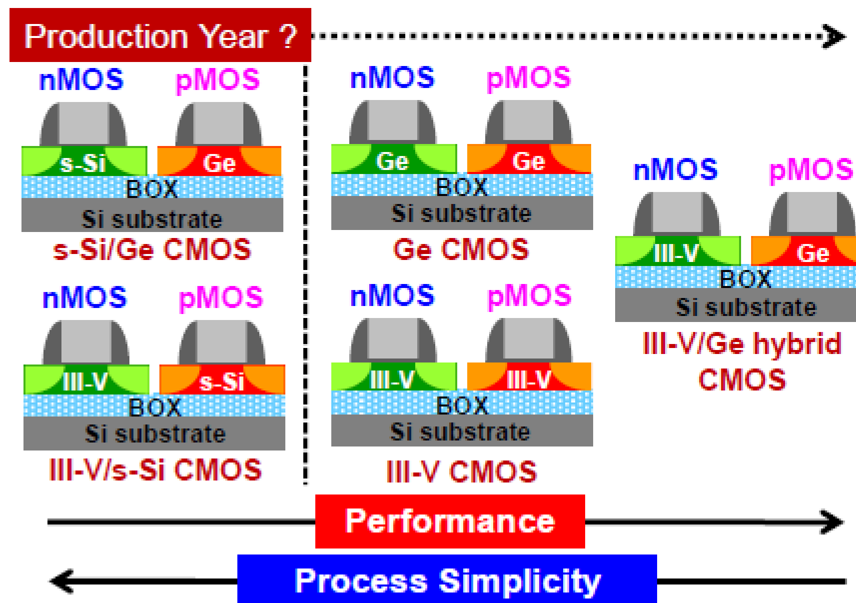


Fig.1: Several CMOS structures using Ge/III-V channels.

There are many challenges:

Scaling of Ge EOT

III-Vs on Si

n- and p-type Integration

Ge Technology

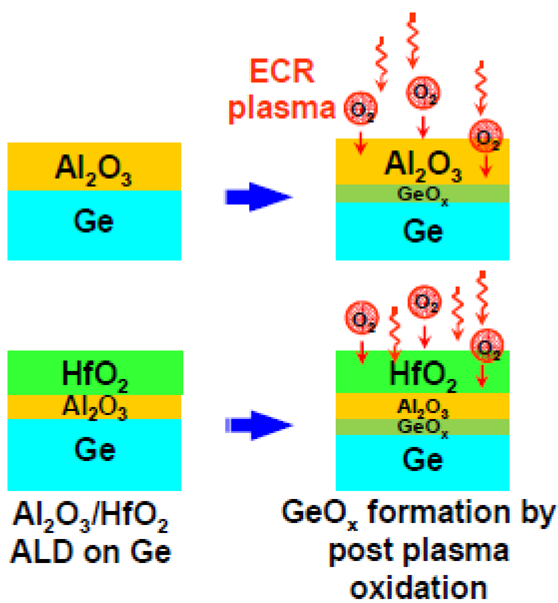


Fig. 2: Proposed GeO_x IL formation process by using ECR oxygen plasma oxidation through ALD Al_2O_3 and HfO_2/Al_2O_3.

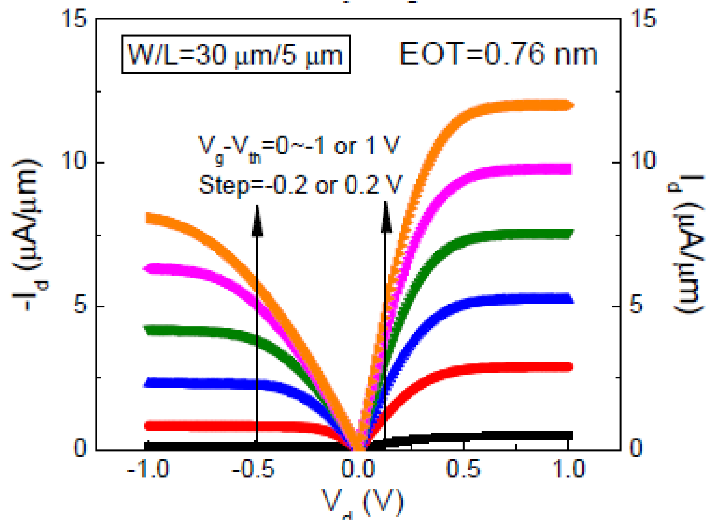


Fig. 7: I_d-V_d characteristics of Ge n- and pMOSFETs with $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks having EOT of 0. 76 nm.

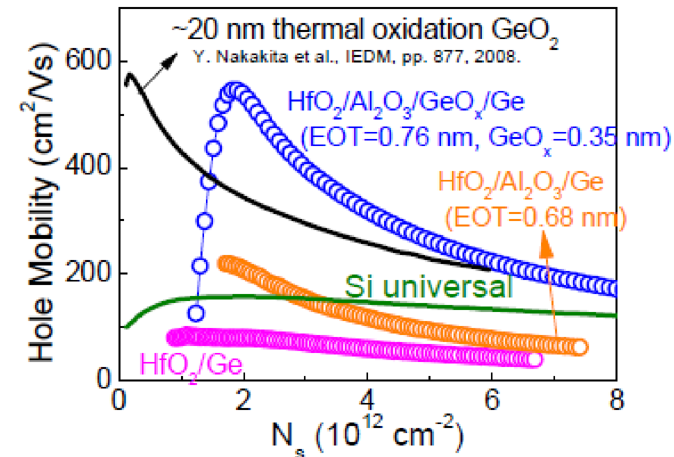
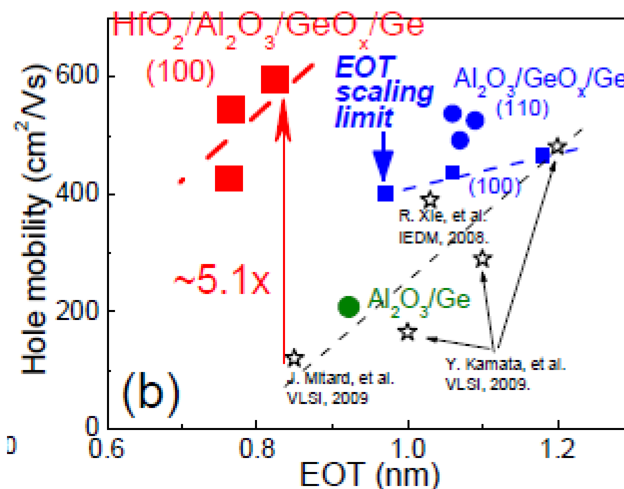


Fig. 9: Hole mobility of Ge pMOSFETs with a variety of MOS interfaces as a function of N_s



InGaAs on Si

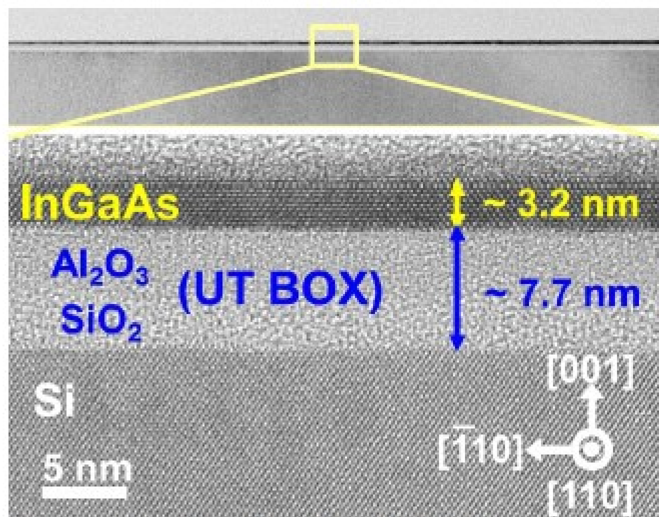


Fig. 13: TEM of a ultrathin body InGaAs substrate on Si with Al_2O_3/ SiO_2 BOX, fabricated by wafer bonding

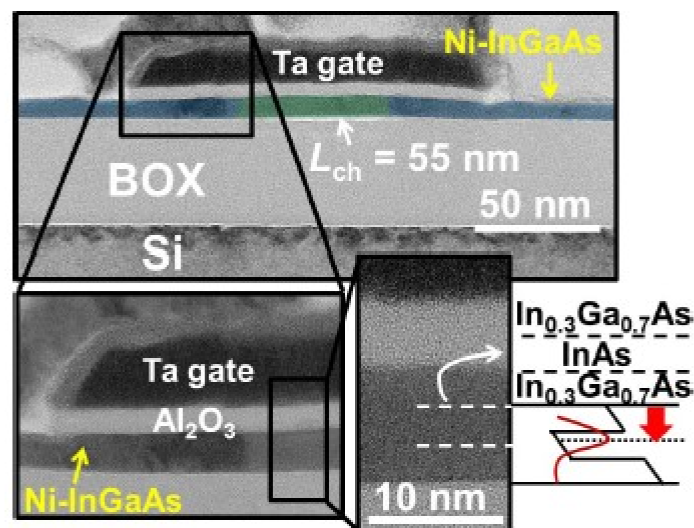


Fig. 16: TEM of 55-nm-L_g ultrathin body MOSFETs with $In_{0.3}Ga_{0.7}As$(3nm)/InAs (3nm)/$In_{0.3}Ga_{0.7}As$(3nm) and Ni-InGaAs metal S/D.

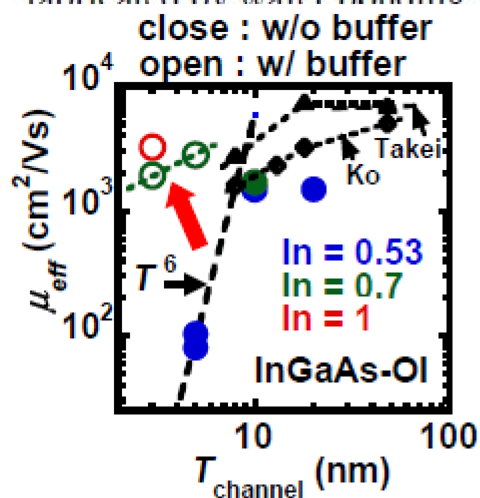


Fig. 14: Body thickness dependence of electron mobility in InGaAs/InAs-based MOSFETs.

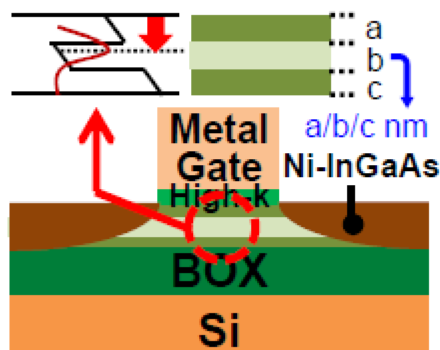


Fig. 15: MOS channel engineering for enhancing mobility in ultrathin body InGaAs-based MOSFETs.

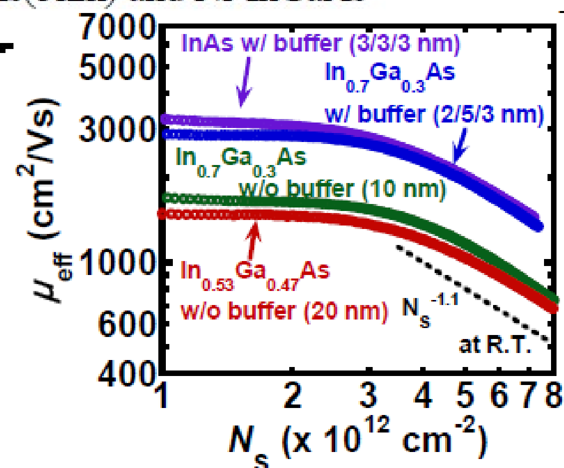


Fig. 19: N_s dependence of electron mobility at RT for InGaAs-based ultrathin body MOSFETs.

Ge and InGaAs Integration

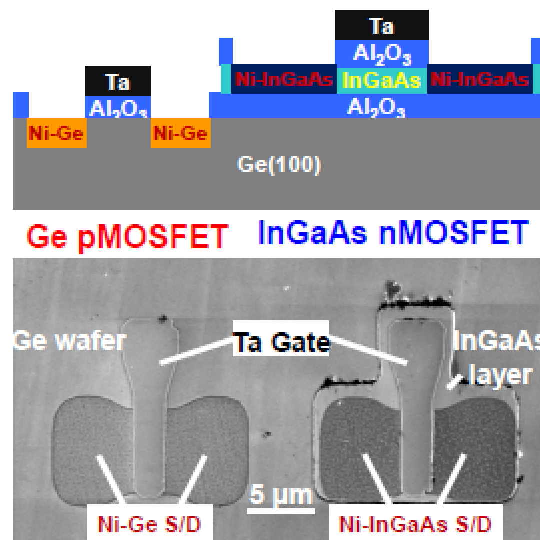


Fig. 27: Schematic view and a photograph of fabricated CMOS structure of InGaAs-OI nMOSFET and Ge pMOSFET by using common Al_2O_3-based gate stack and Ni-based S/D

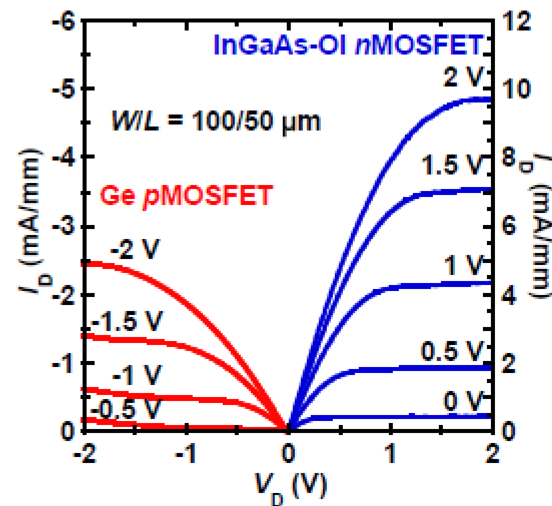
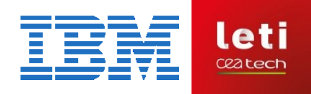
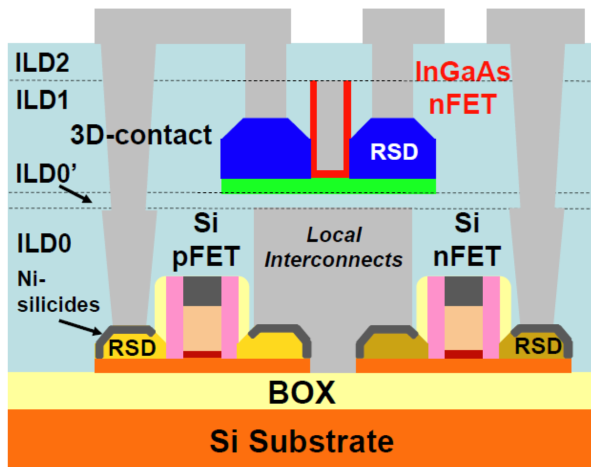


Fig. 28: I_d - V_d characteristics of a Ge pMOSFET and a 20-nm-thick InGaAs-OI nMOSFET, fabricated on a same wafer.

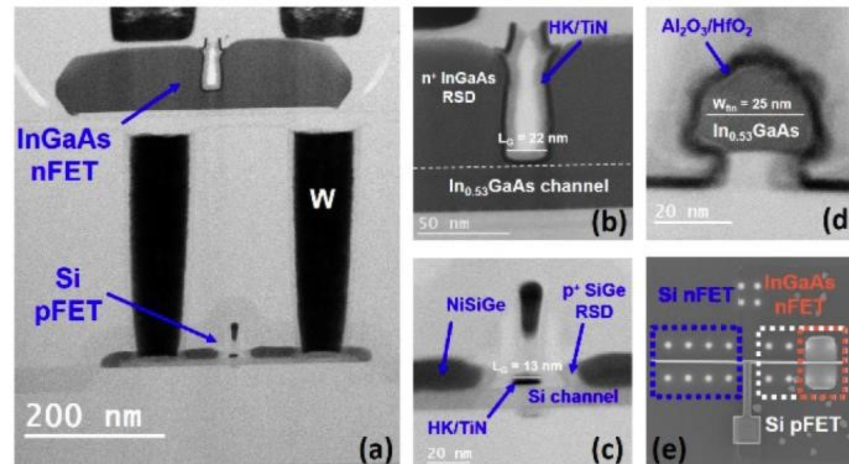
3D Monolithic Integration of InGaAs/Si CMOS Circuit



- Si FDSOI CMOS prepared by LETI until W-plugs
- 3D Monolithic integration of InGaAs FinFETs at IBM
- Proven no impact of InGaAs optimized process on Si FDSOI performance



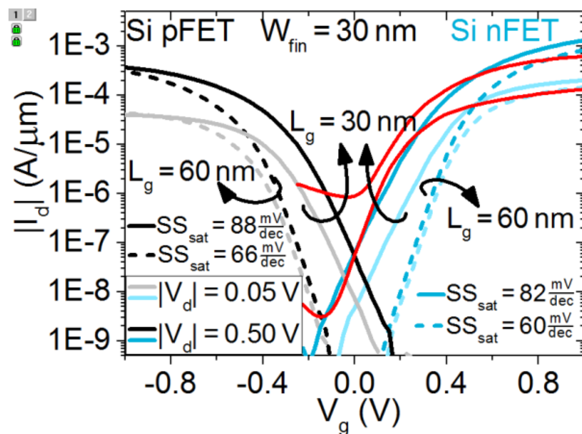
V. Deshpande, et al., VLSI Technology, (2017)

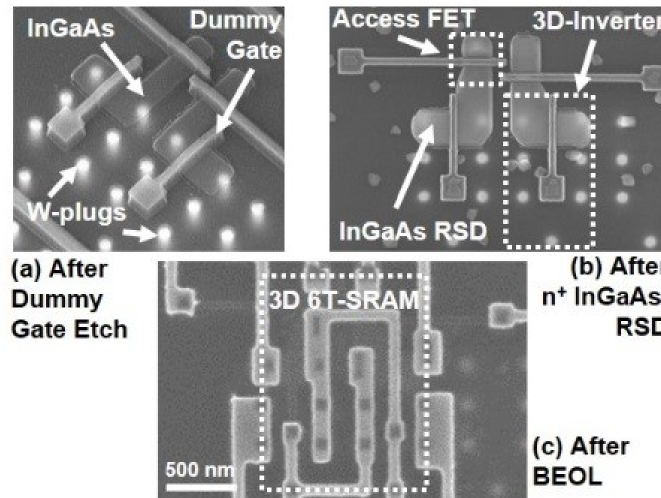


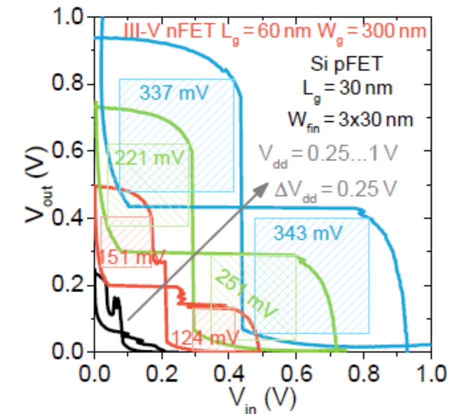
3D Integration scheme demonstrated

3D Monolithic Integration of InGaAs/Si CMOS Circuits

- Operational Si CMOS and InGaAs n-FETs demonstrated
- Design, fabrication and operation of 3D 6T-SRAM cells
- InGaAs RFFETs also fabricated on top layer → III-V RF + Si CMOS







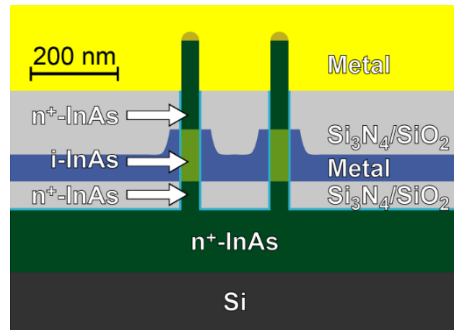
V. Deshpande, et al., VLSI Technology, (2017)

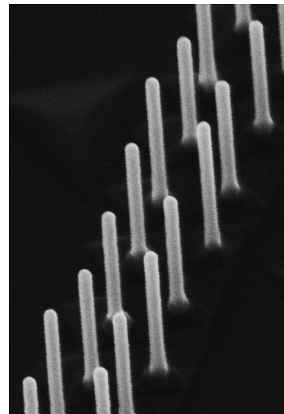
Why III-V Nanowires

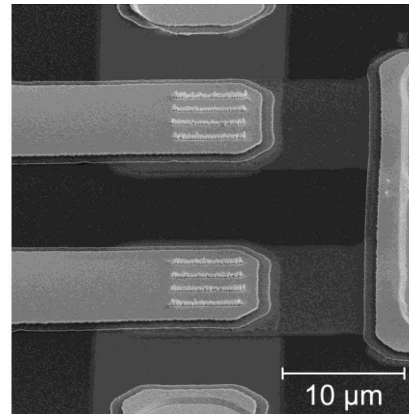
NANO ELECTRONICS GROUP

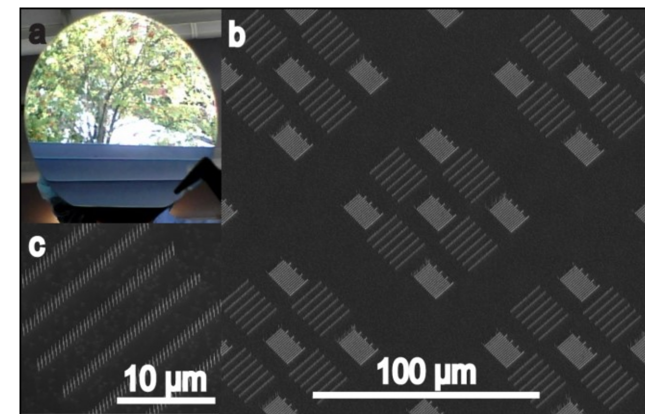
Why III-V Nanowires?

- **Advantageous transport** → **high transconduc. and I_{on}**
- **Wrap-gate geometry** → **low output conduc. and DIBL**
- **Band gap engineering** → **increased breakdown, reduced I_{off}**
- **Small nanowire footprint** → **reduced defect propagation probability**

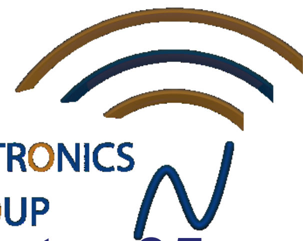






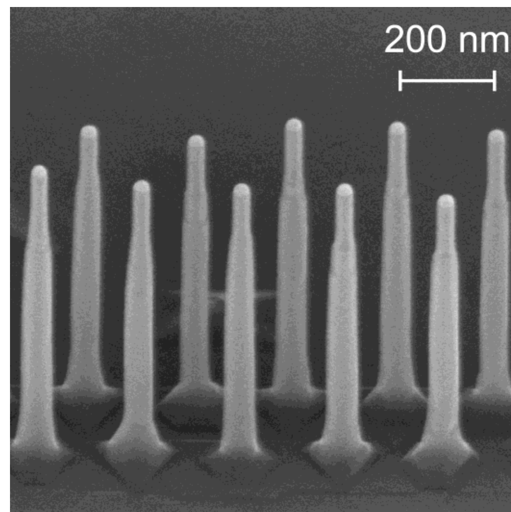


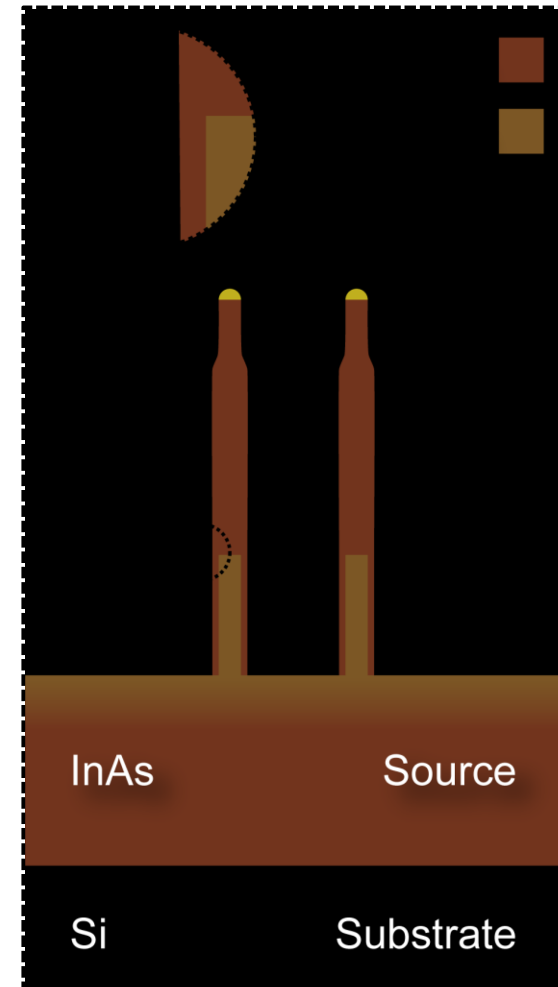
Gate-Last Process



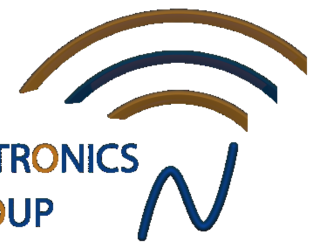
- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion

Core Diameter 35 nm
10 nm overgrowth

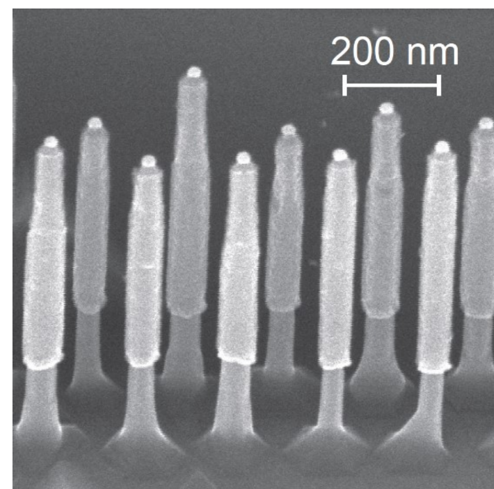


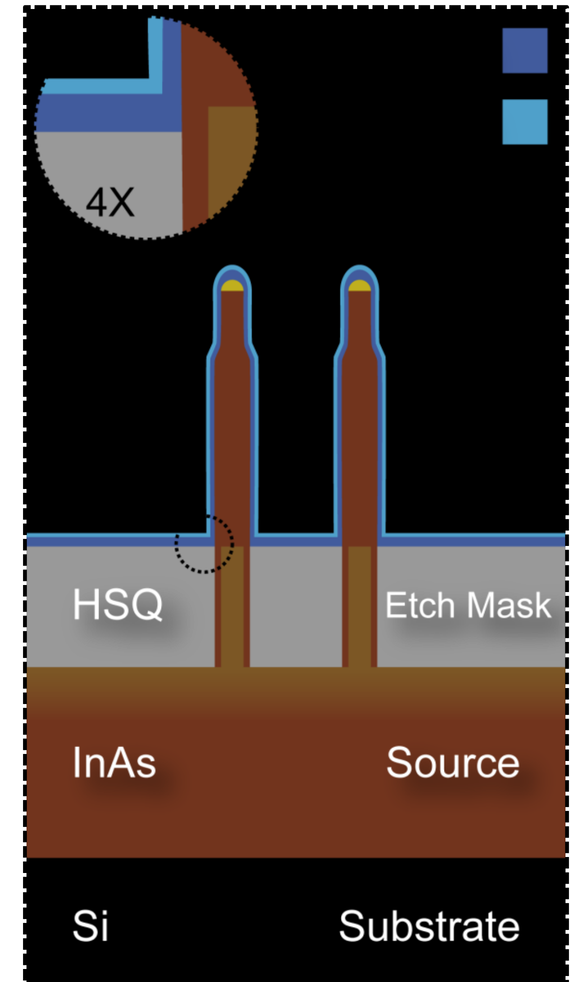


Gate-Last Process

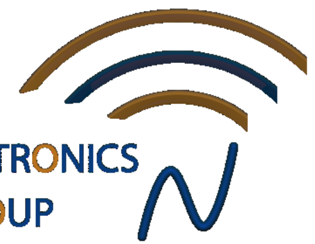


- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion

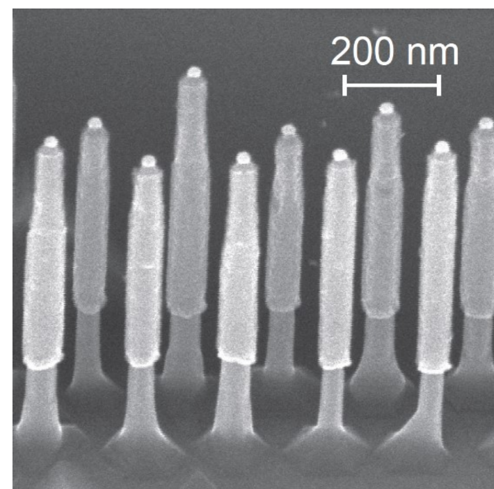


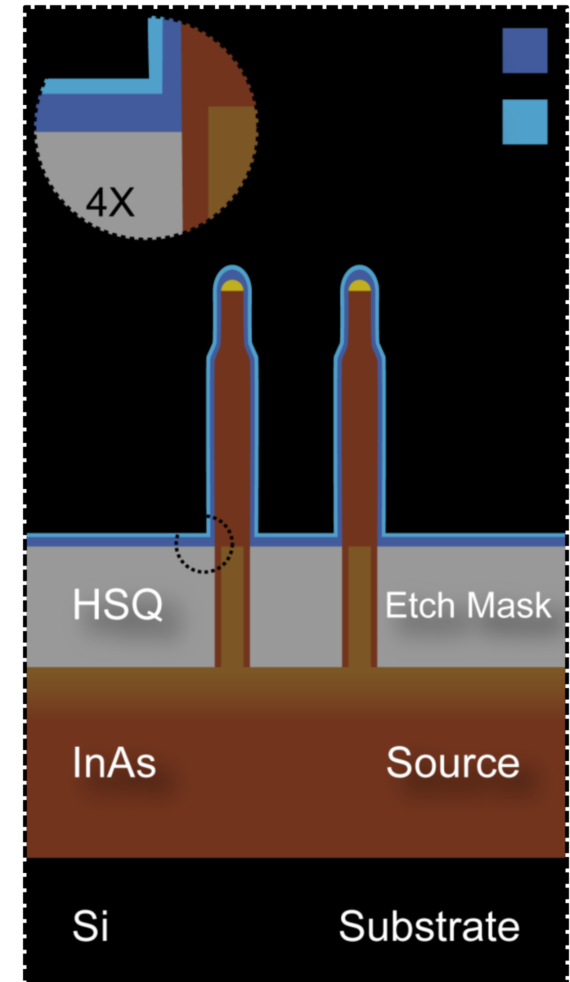


Gate-Last Process

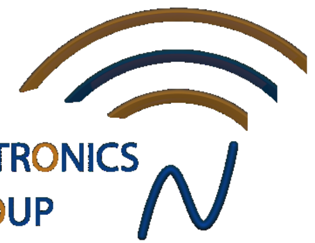


- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion



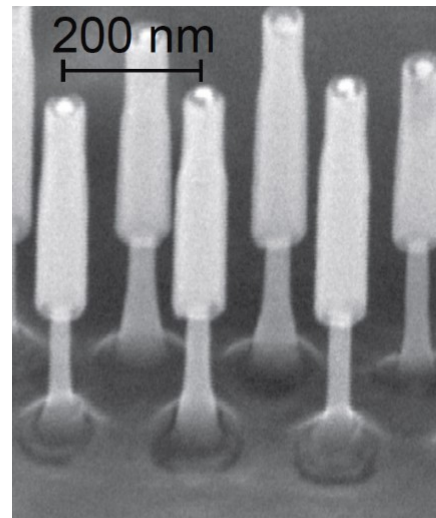


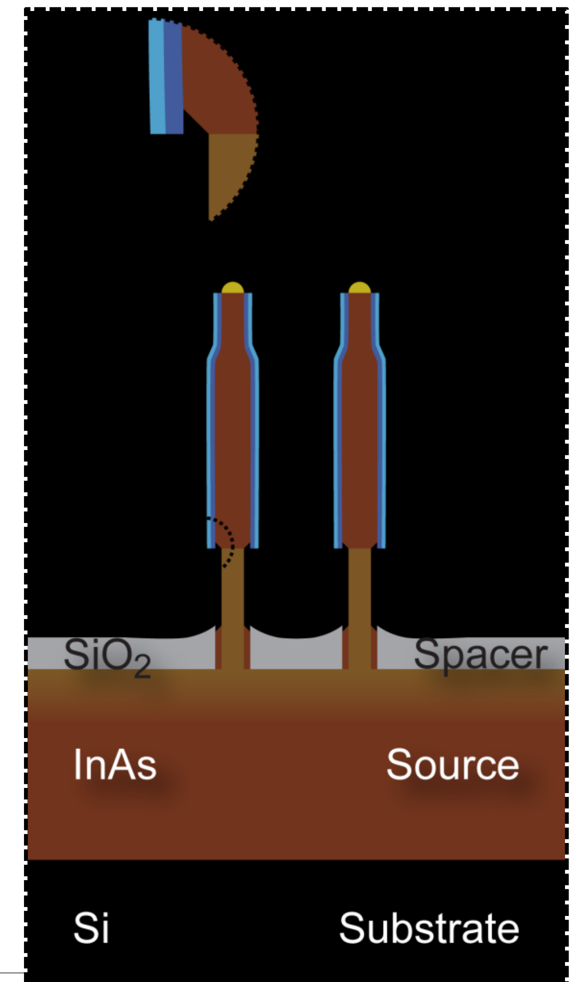
Gate-Last Process



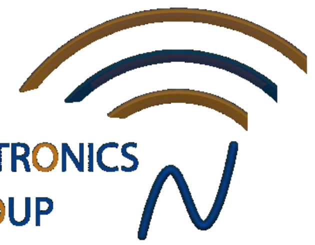
- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion

Diameter 28 nm

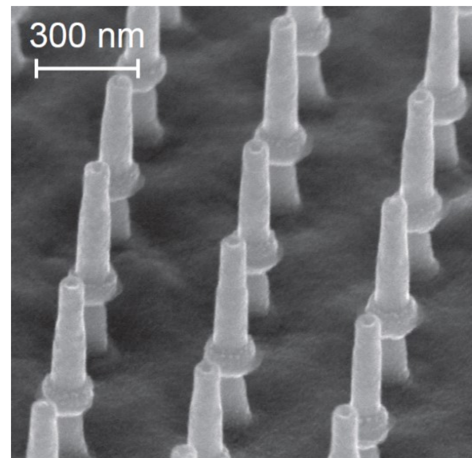


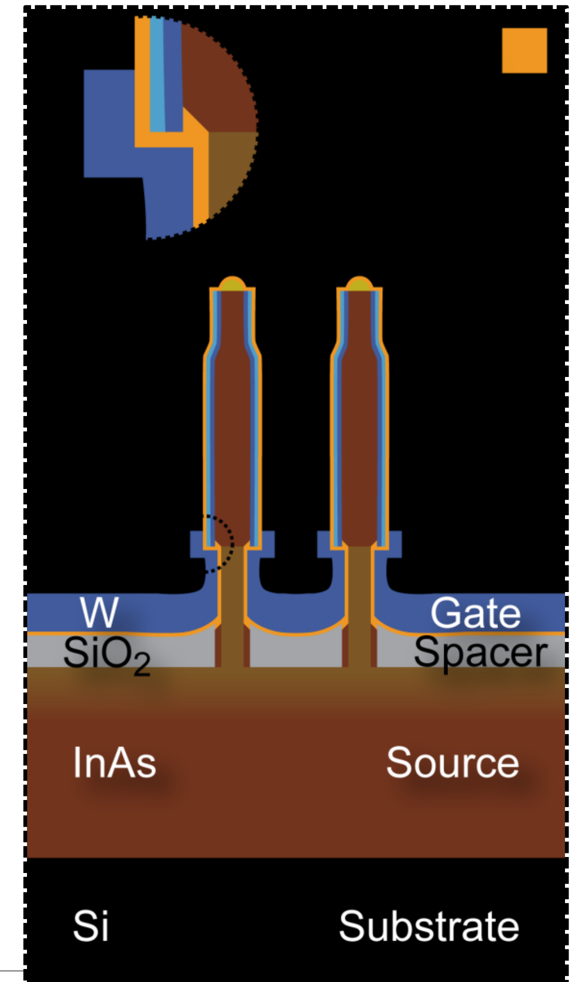


Gate-Last Process



- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion

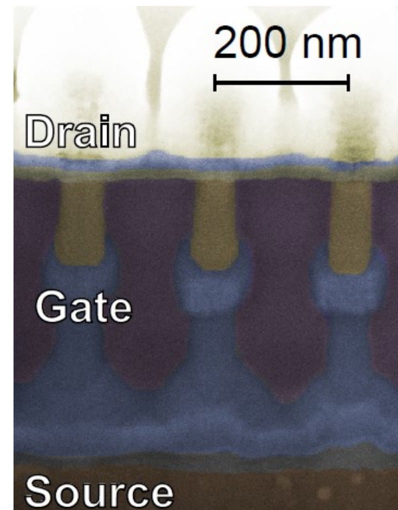


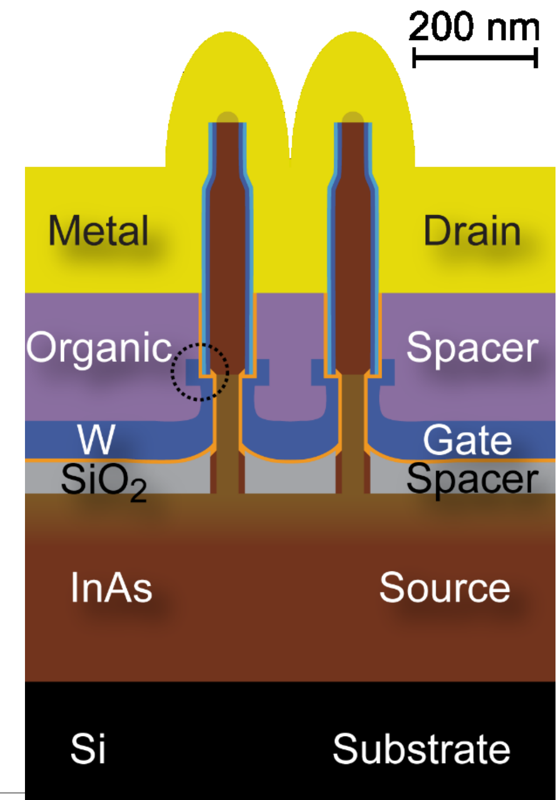


Gate-Last Process

NANO ELECTRONICS GROUP

- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion



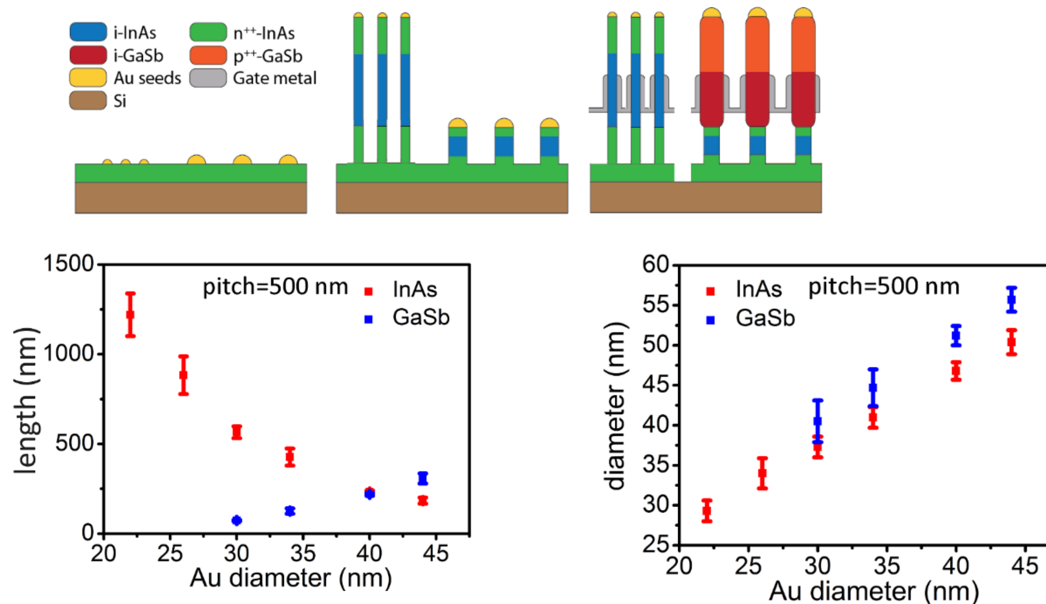


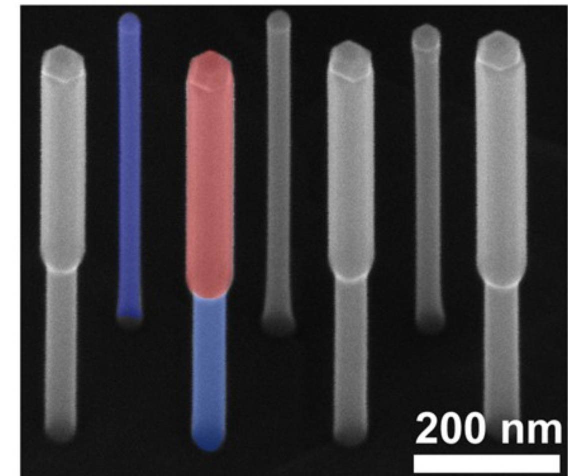
M. Berg et al., IEDM 2015

InAs-GaSb Nanowire Growth

NANO ELECTRONICS GROUP

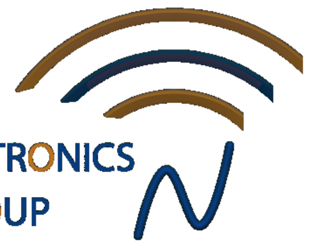
- **Growth technology establisehd for co-integration of InAs and GaSb in one growth run**
- **Diameter of GaSb larger than InAs since Sb enhances group III solubility in Au**
- **Distance between two types of wires down to 200 nm**





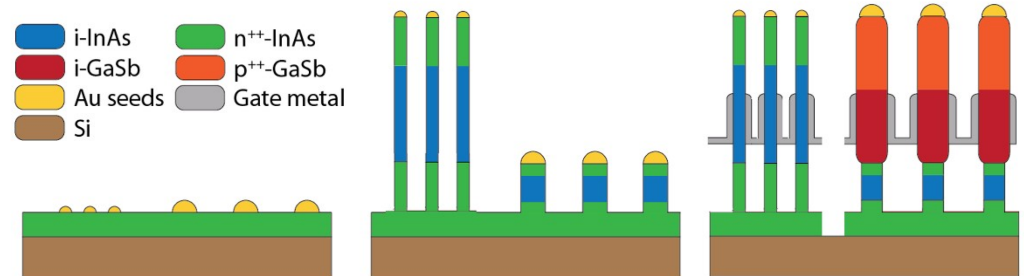
J. Svensson et al., Nano Letters 2015

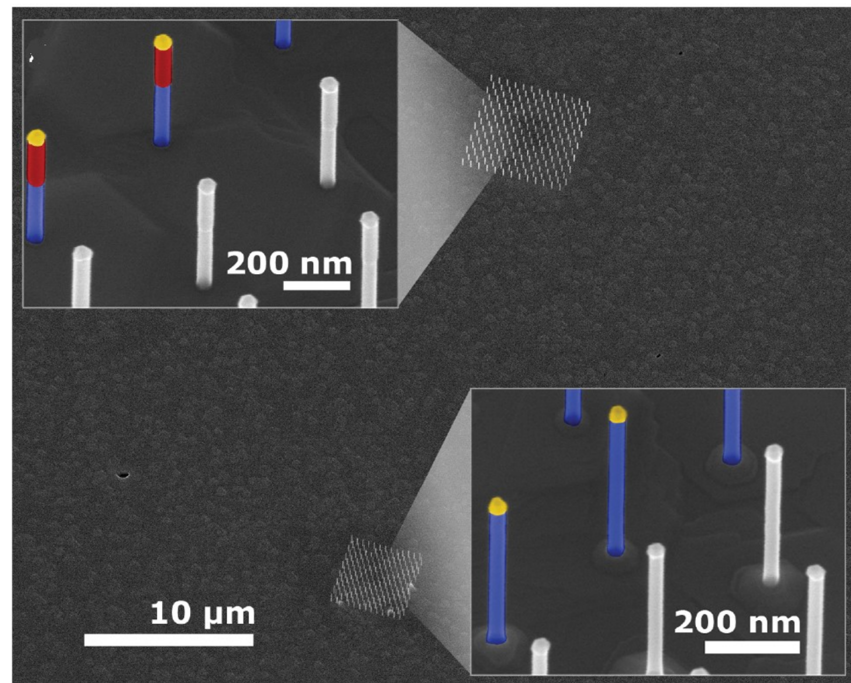
p- and n-MOSFET Layout



- Tuning d_{Au} and pitch enables equal length of InAs and InAs/GaSb NWs.

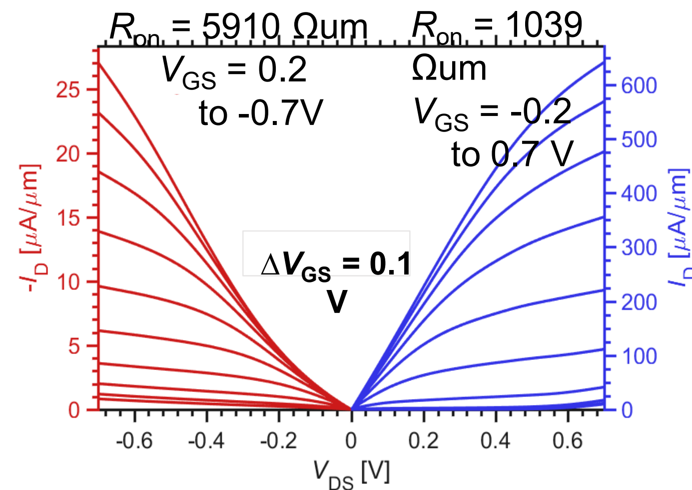
- Doping profiles enable n.i.d. channel and good contacts.

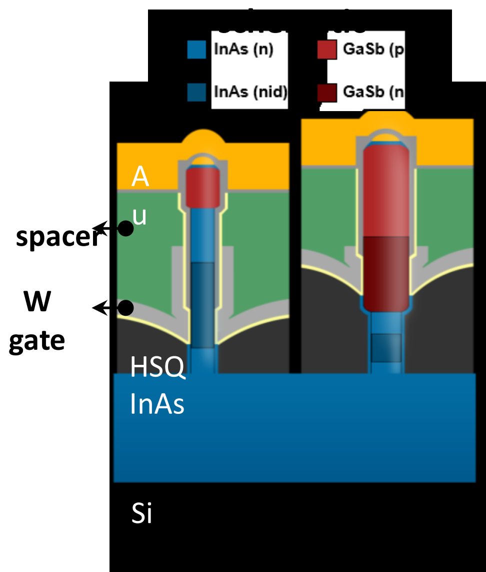


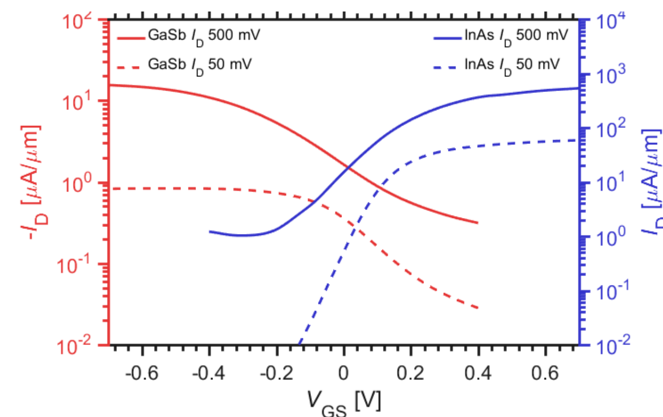


InAs-GaSb Co-Integration

- **Process optimized for InAs nMOSFET performance**
- **Common gate-stack with Al_2O_3 and sputtered W**
- **InAs: $g_{m,peak}$ = 1.2 mS/µm, SS_{lin} = 76 mV/dec**
- **GaSb: $g_{m,peak}$ = 74 µS/µm, SS_{lin} = 273 mV/dec**



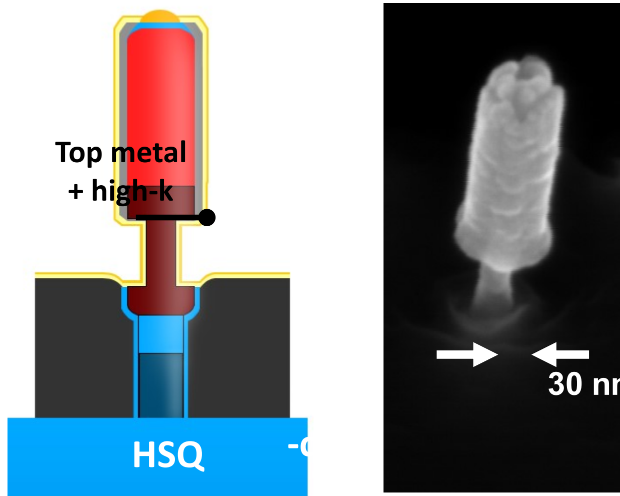


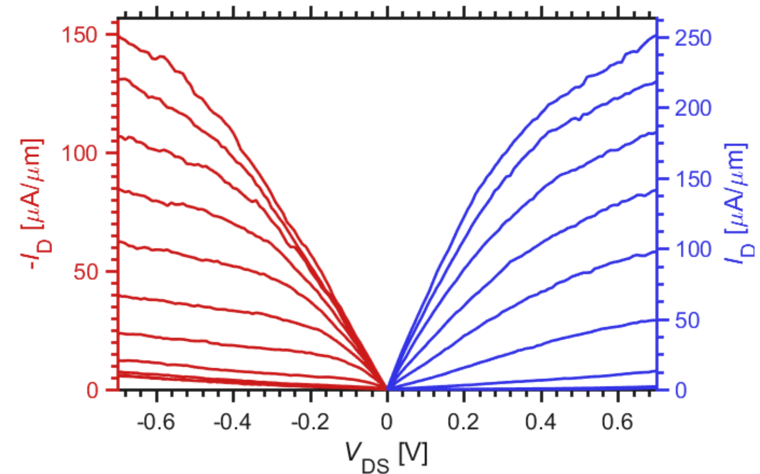


A. Jönsson et al., EDL 2018

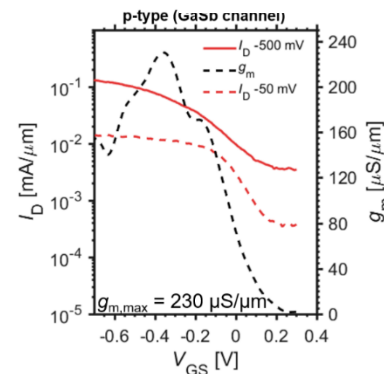
Best GaSb Transistor – so far

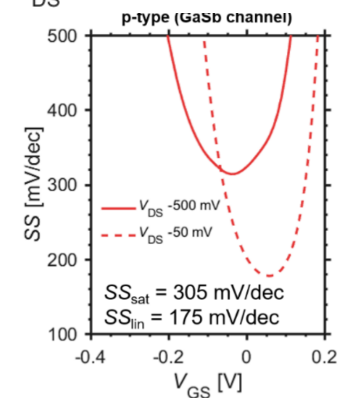
- **P-type:** Lg = 80 nm, 20 - 29 nm diameter
- **N-type:** Lg = 150 nm, 5-10 nm diameter





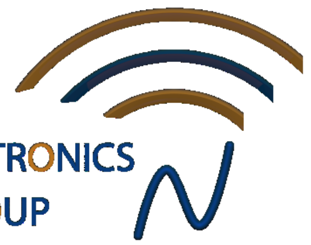
A. Jönsson et al., IEDM 2018



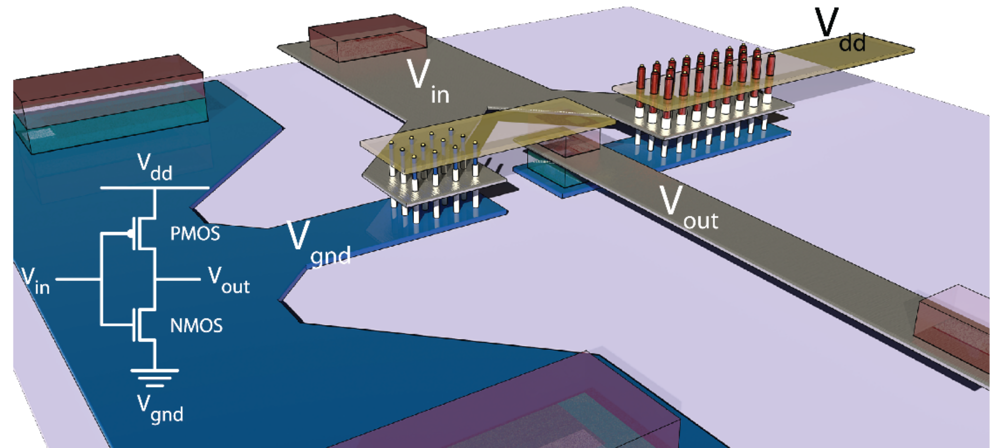


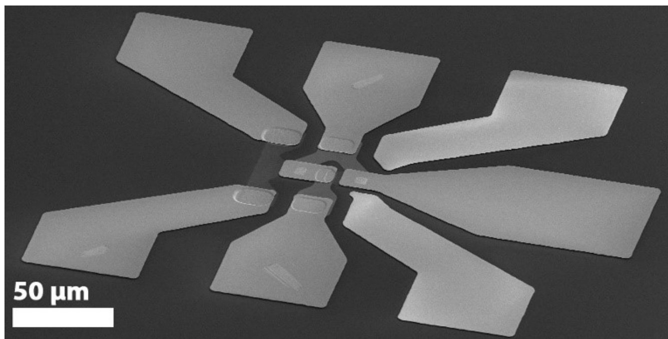
- P-type GaSb MOSFET
- D_{GaSb} = 22 nm *and* L_g = 60 nm

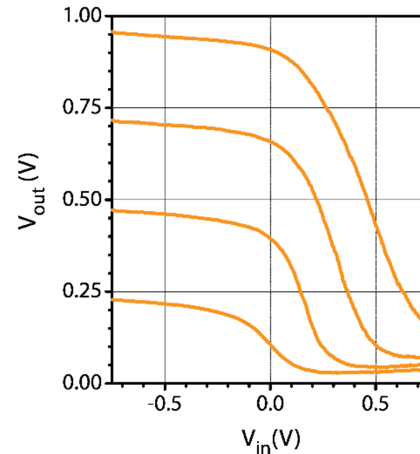
Inverter

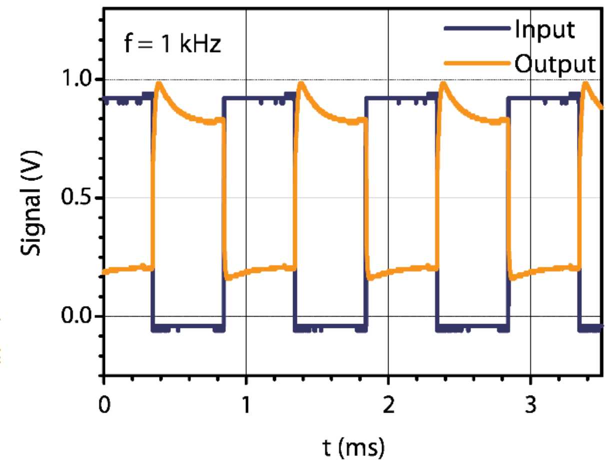


- Gain = 2 V/V (at V_{dd} = 0.5 V).
- Frequency response limited to 1 kHz due to parasitics.
- Can be improved by EBL patterned gate/drain electrodes and a self-aligned gate process.

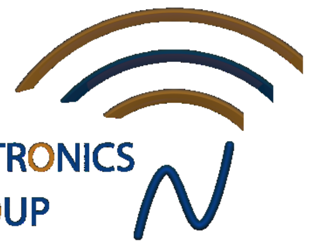




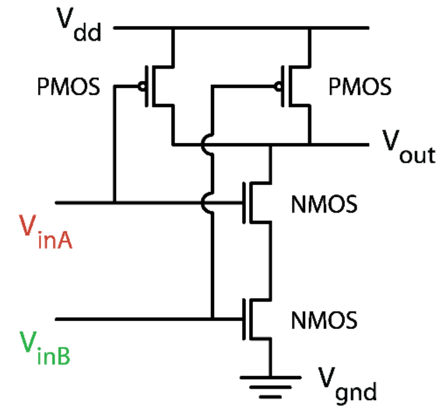


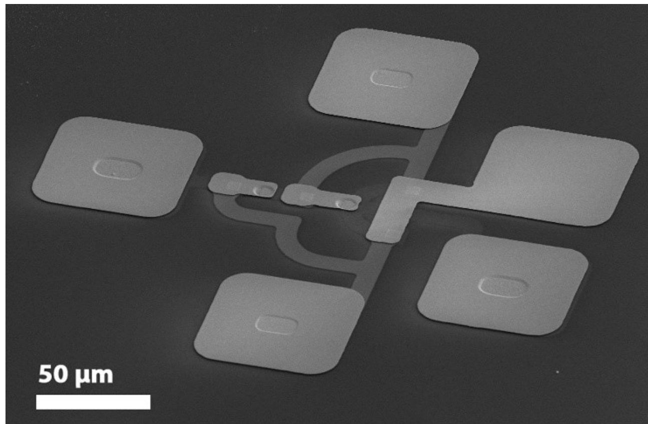


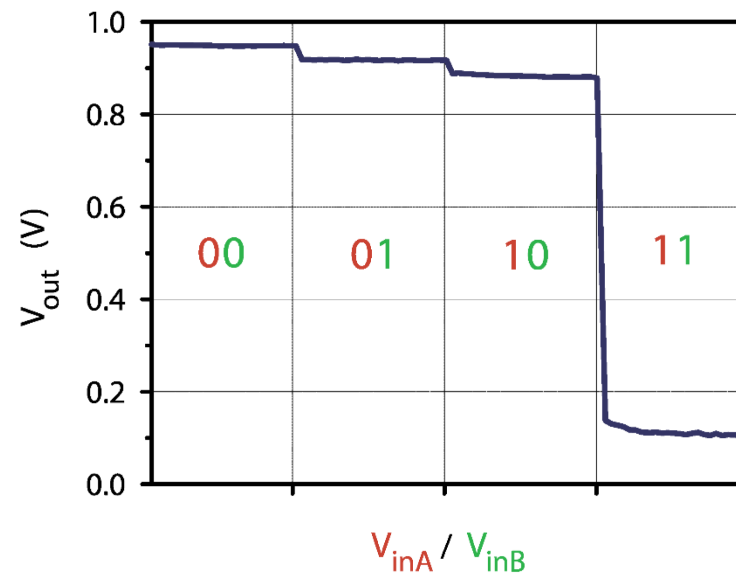
NAND gate



-Two p-MOSFETs in parallell + two n-MOSFETs in series.







LETTER

doi:10.1038/nature11293

A III–V nanowire channel on silicon for high-performance vertical transistors

Katsuhiro Tomioka[1,2], Masatoshi Yoshimura[1] & Takashi Fukui[1]

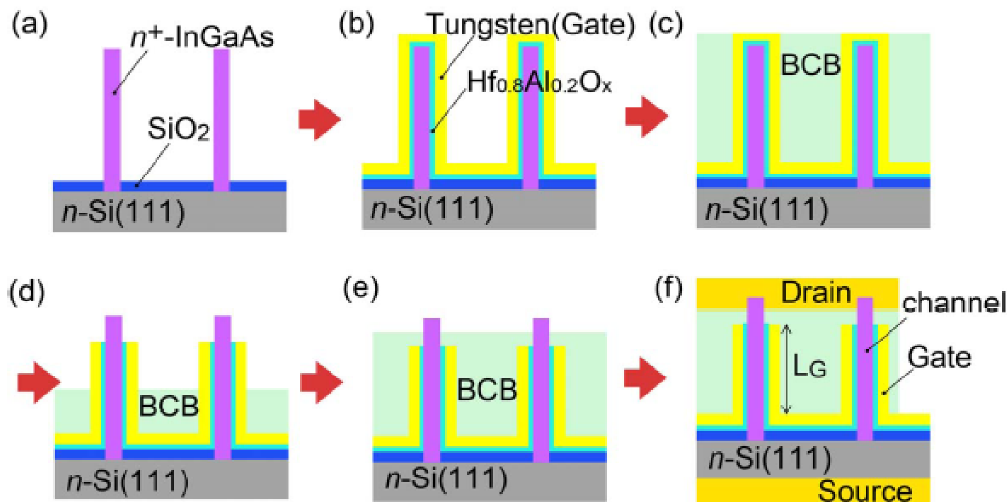
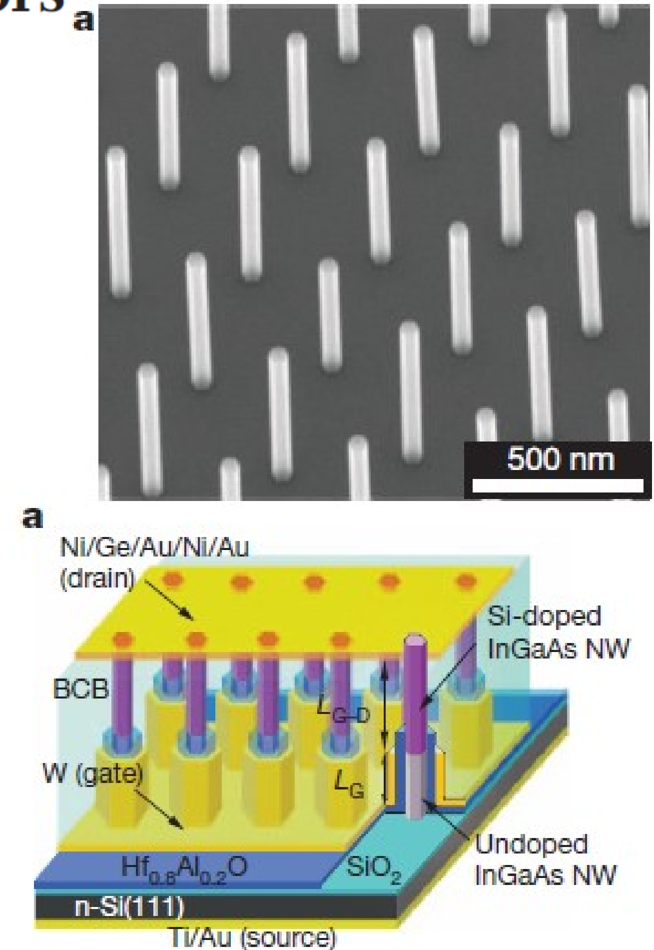
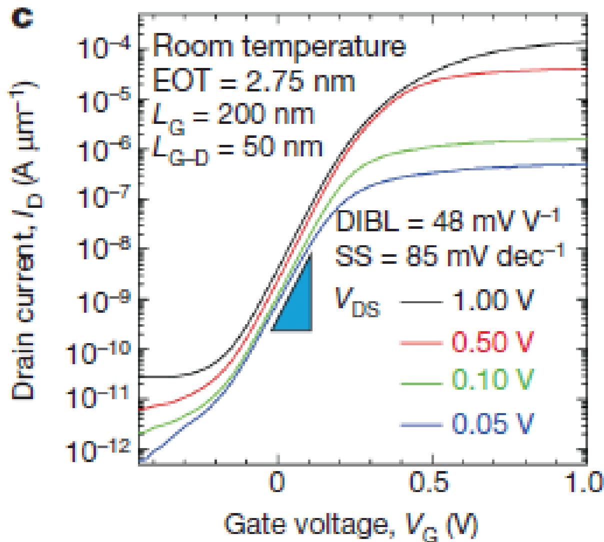


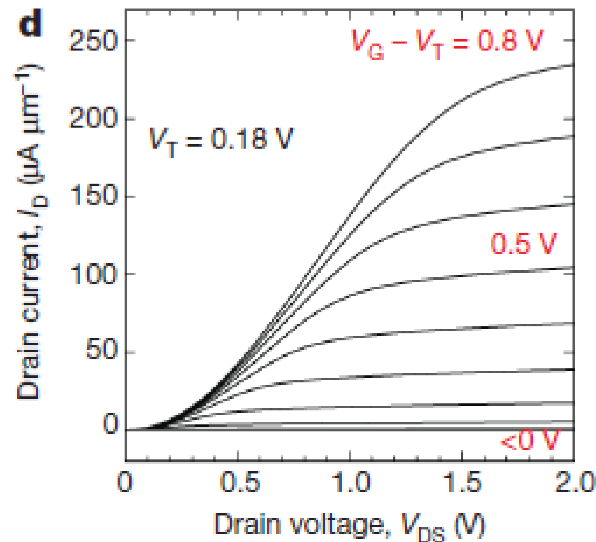
Figure 3: Device fabrication processes: (a) InGaAs NW growth. (b) Atomic layer deposition of $Hf_{0.8}Al_{0.2}O_x$ and sputtering of W-gate metal. (c) Spin-coating of BCB polymer. (d) RIE of BCB, gate oxide and W metal. (e) Spin-coating of BCB and RIE etch back for electrical separation layer formation. (f) Drain and source metal evaporation.

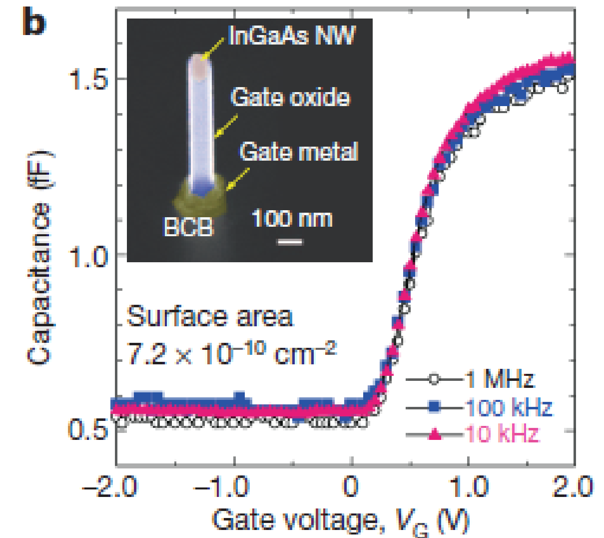


Nanoelectronics: III-V Nanowires

Device Performance







Gate length 200 nm

Nanowire diameter 60 nm

10 nanowires in the array

Transconductance of 280 μS/μm at Vd=1V

SS 98 mV/dec.

Device Performance

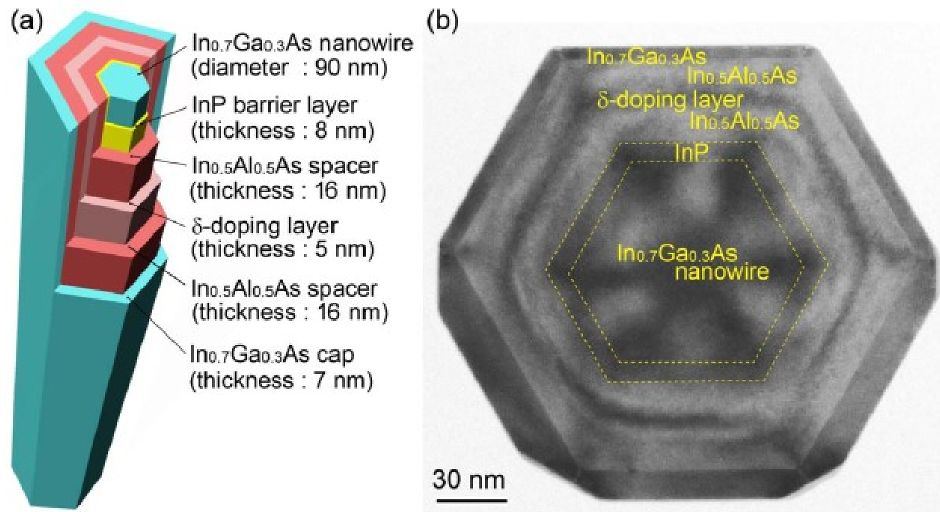
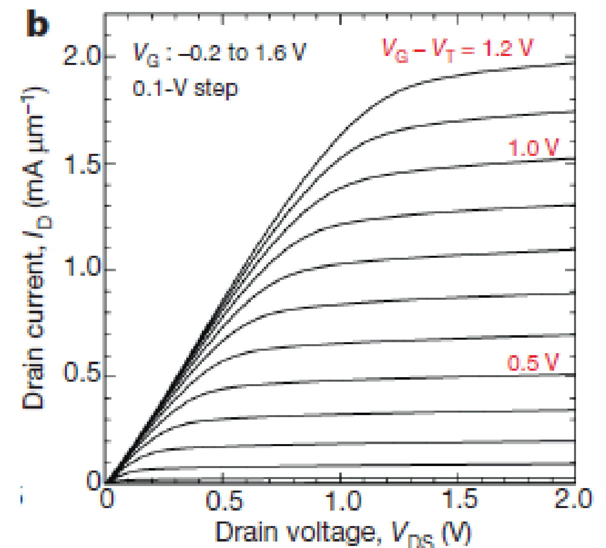
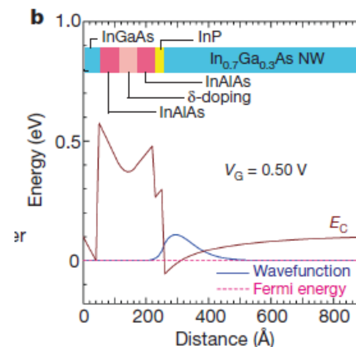
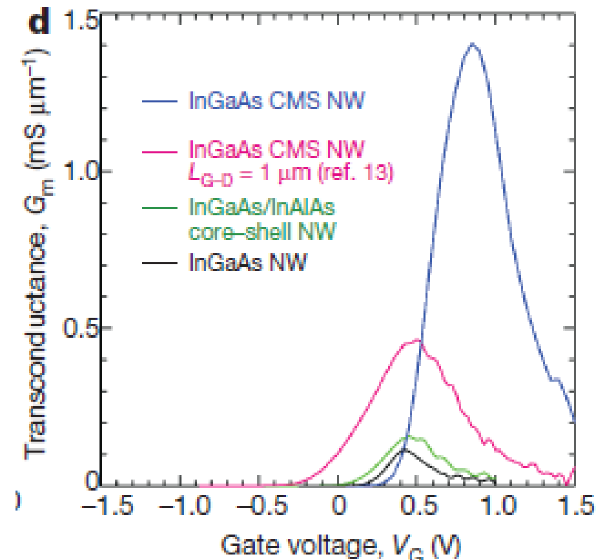


Figure 9: (a) Illustration of InGaAs/InP/InAlAs/δ-dope InAlAs/InAlAs/InGaAs core-multishell NW. (b) Cross-section TEM image of the growth results of Fig. 9(a). The InGaAs NW is 90 nm in diameter.







Gate length 200 nm

Nanowire diameter 90 nm

10 nanowires in the array

g_m=1.42 mS/μm at V_d=0.5 V

SS 75 mV/dec.