Lecture 4: III-V CMOS II

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III–V Complementary Metal–Oxide–Semiconductor Electronics on Silicon Substrates

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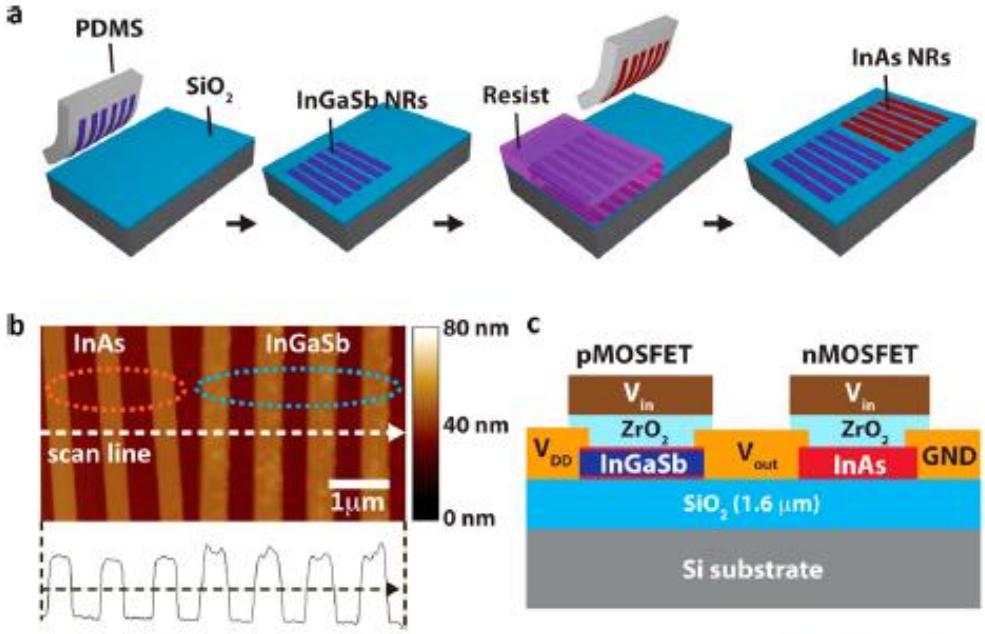


InAs/InGaSb Heterostructure:

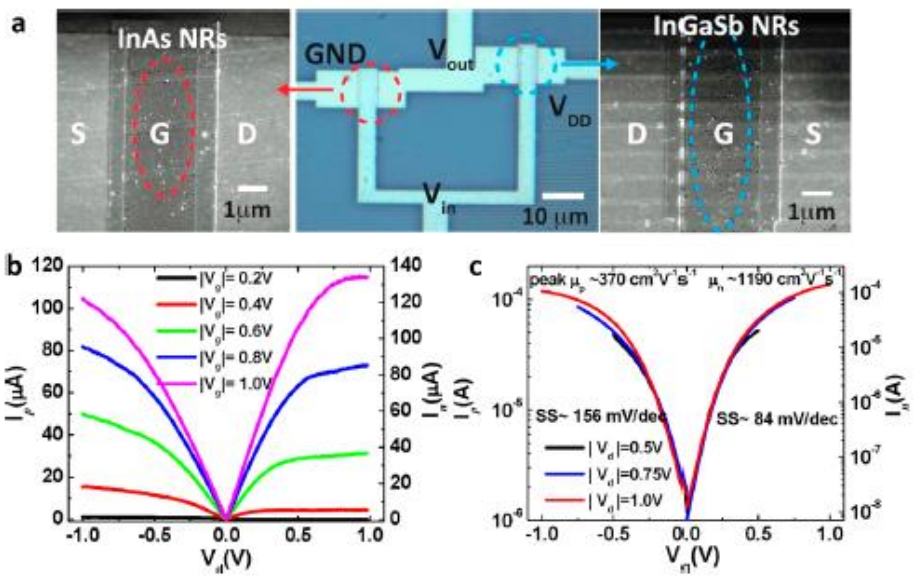
Surface passivation

Non-doped ohmic contact formation

Provide strain to enhance mobility

Figure 1. III–V XOI CMOS. (a) Process schematic for the heterogeneous integration of InAs and InAs/InGaSb/InSb XOI on a Si/SiO_2 substrate. (b) Atomic force micrograph of transferred InAs and InAs/InGaSb/InAs NRs, located adjacently. (c) Schematic representation of a top-gated CMOS inverter with InAs (n-type) and InGaSb (p-type) active layers, having 10 nm of ZrO_2 as the top-gate dielectric.

Electrical Characteristics



InAs: 3 nanoribbons
340 nm L_g
μ 1190 cm^2/Vs
SS 84 mV/dec

InGaSb: 9 nanoribbons
200 nm L_g
μ 370 cm^2/Vs
SS 156 mV/dec

Figure 2. Performance of *p*- and *n*-type XOI MOSFETs. (a) Optical image (center) of a fabricated III–V CMOS inverter and the corresponding SEM images of each channel region (left: InAs; right: InAs/InGaSb/InAs). (b) Output and (c) transfer characteristics of *p*- (left axis) and *n*- (right axis) MOSFETs.

Circuits

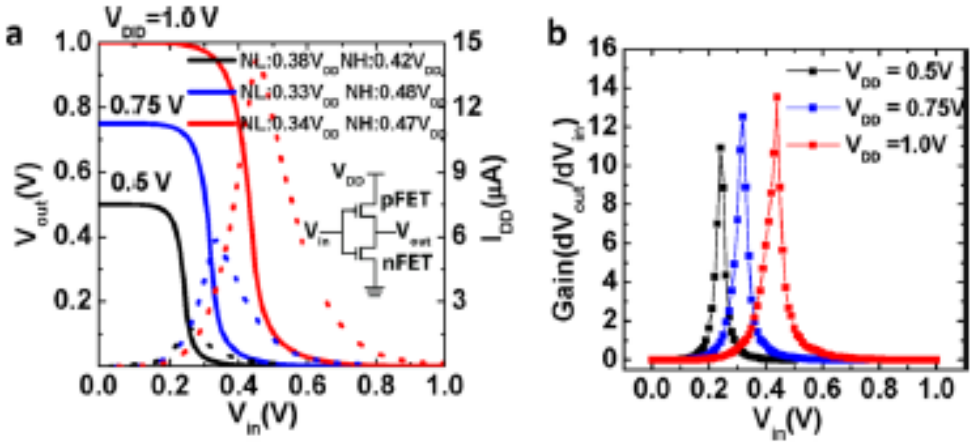


Figure 3. III–V CMOS inverter. (a) Transfer characteristics of a CMOS inverter, measured at different supply voltages (V_{DD}). Inset shows the circuit diagram for the fabricated inverter. (b) Inverter gain (dV_{out}/dV_{in}) dependence on the input voltage.

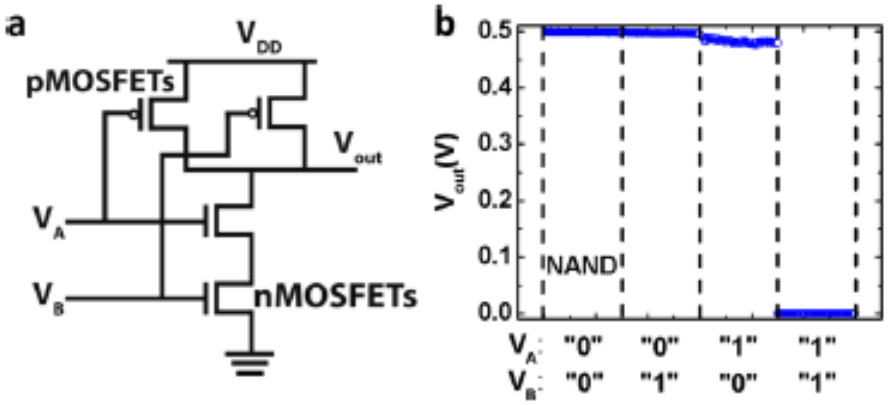


Figure 4. III–V CMOS NAND logic gate. (a) Circuit schematic of a CMOS NAND gate. The circuit is designed by connecting two p-MOSFETs in parallel and two n-MOSFETs in series. (b) Output voltage V_{out} for four different combinations of input states "0 0", "0 1", "1 0", and "1 1". The output is in the "low-state" only if the inputs are "1 1". Note: Input voltages of +0.5 and −0.5 V are treated as logic "1" and "0", respectively. The supply voltage (V_{DD}) for the circuit is 0.5 V.

GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al_2O_3 as Gate Dielectric

Min Xu, Runsheng Wang, *Student Member, IEEE*, and Peide D. Ye, *Senior Member, IEEE*

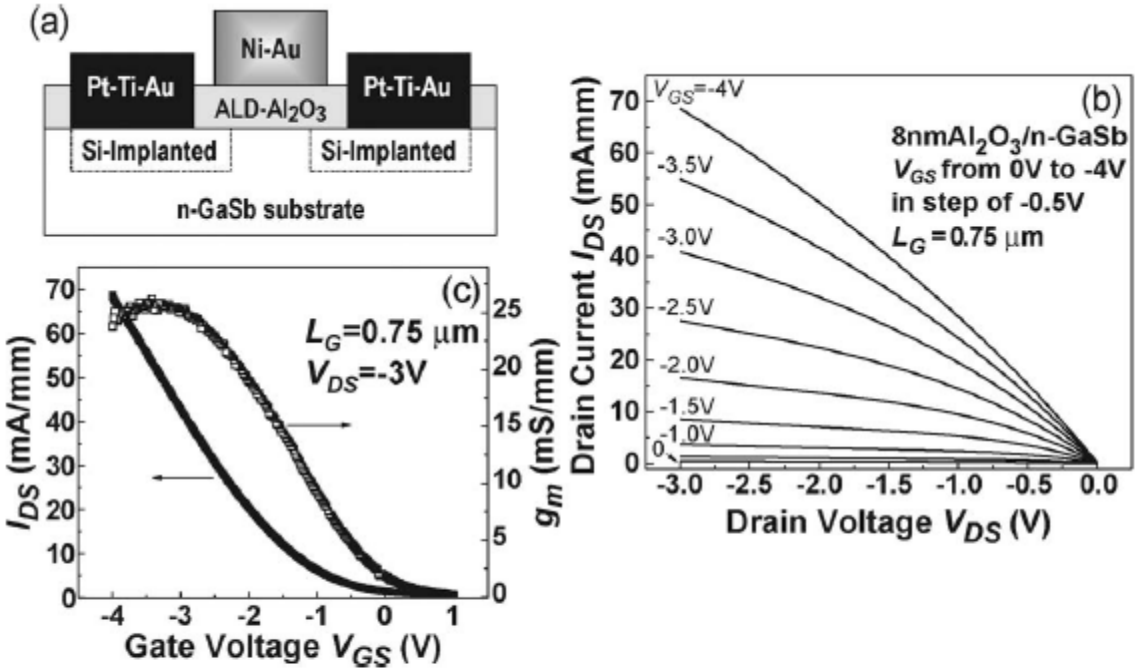


Fig. 1. (a) Schematic cross section of an inversion-mode GaSb PMOSFET with ALD Al_2O_3 as gate dielectric. (b) DC output characteristic of a 0.75-μm-gate-length device fabricated by Process I at $V_{DS} = -3$ V and $V_{GS} = -4$ V, showing the drain current potential at the current interface quality and dielectric strength. (c) DC transfer characteristics of the same device at $V_{DS} = -3$ V.

GaSb:

Large hole mobility

Large density of states in valence band

Low density of defects close to valence band

Electrical Characteristics

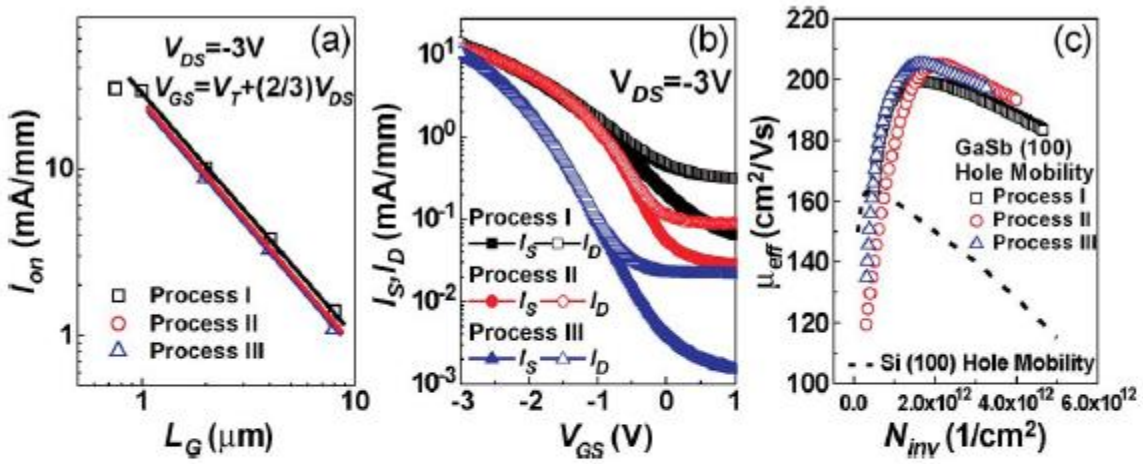


Fig. 2. (a) Comparison of scaling behavior of drain currents versus gate length L_G on three different processed samples at $V_{\mathrm{DS}} = -3$ V and $V_{\mathrm{GS}} = V_T + (2/3) \cdot V_{\mathrm{DS}}$. (b) (Empty signs) Drain currents and (solid signs) source currents versus gate bias V_{GS} on three different processed samples at $V_{\mathrm{DS}} = -3$ V. (c) Effective mobility (μ_{eff}) versus inversion hole charge density (N_{inv}). μ_{eff} is extracted from split C–V method with all three processes. The Si(100) universal hole mobility is also included for comparison.

Scaling of gate length Important due to larger effective mass

Process dependence (ohmic contacts)

Mobilities above 200 cm²/Vs

Interface quality

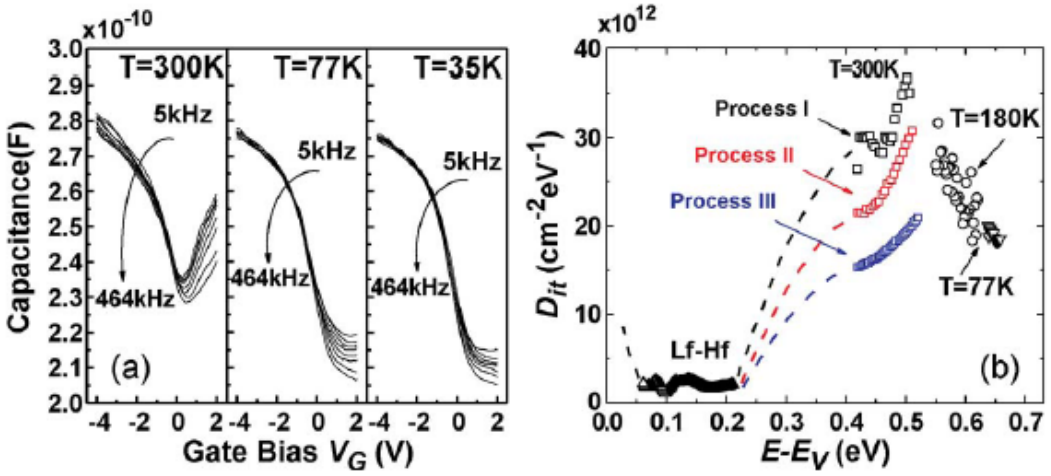


Fig. 3. (a) C–V plots of Au/ Ni/8-nm-Al_2O_3/p-GaSb at 300 K, 77 K, and 35 K. The excellent frequency-dispersion behavior at accumulation capacitance at all temperatures indicates true hole accumulation and a good interface near the valence band. The capacitor area is 3.14×10^4 μm^2 with a dielectric constant of ~8 for Al_2O_3. (b) Interface trap distribution near the conduction band is obtained from temperature-dependent conductance method on n-MOSCAPs at 300 K, 180 K, and 77 K, and that near the valence band is obtained from low-f–high-f C–V measurement on p-MOSCAPs at 35 K. The D_{it} distribution is similar to that on Ge without good surface passivation. The hole capture cross section in GaSb from 10^{-18} to $10^{-14}/cm^2$, depending on the energy level [20], is chosen to determine the D_{it} distribution. The dashed lines are guides to the eye. The square signs are obtained from conductance method performed at 300 K with the black signs for Process I, the red signs for Process II, and the blue signs for Process III. The black circle signs and down triangle signs are obtained from Process-I samples performed at 180 K and 77 K, respectively. Process I with a higher activation temperature of 650 °C results in a larger D_{it} since GaSb has a melting point of 712 °C and is easier to lose Sb at a higher processing temperature [10].

Comparably low density of defect levels close to valence band

High density of defect levels close to conduction band

Process dependence

MOS interface and channel engineering for high-mobility Ge/III-V CMOS

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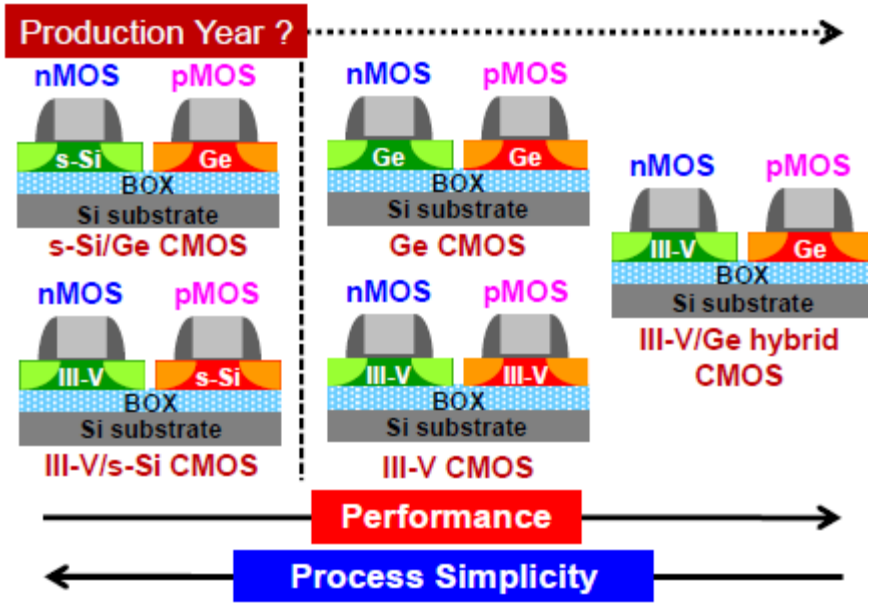


Fig.1: Several CMOS structures using Ge/III-V channels.

There are many challenges:

Scaling of Ge EOT

III-Vs on Si

n- and p-type Integration

Ge Technology

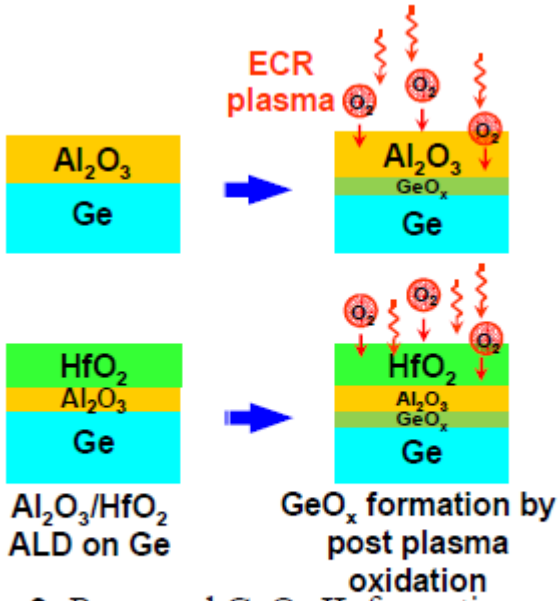


Fig. 2: Proposed GeO_x IL formation process by using ECR oxygen plasma oxidation through ALD Al_2O_3 and HfO_2/Al_2O_3.

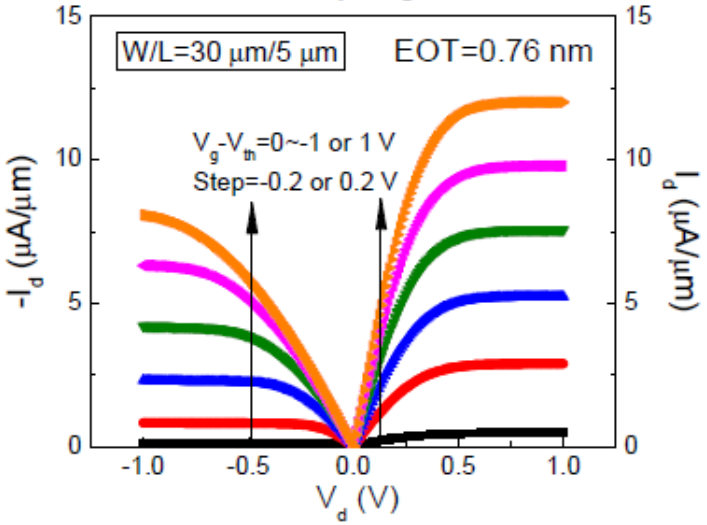


Fig. 7: I_d-V_d characteristics of Ge n- and pMOSFETs with $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks having EOT of 0. 76 nm.

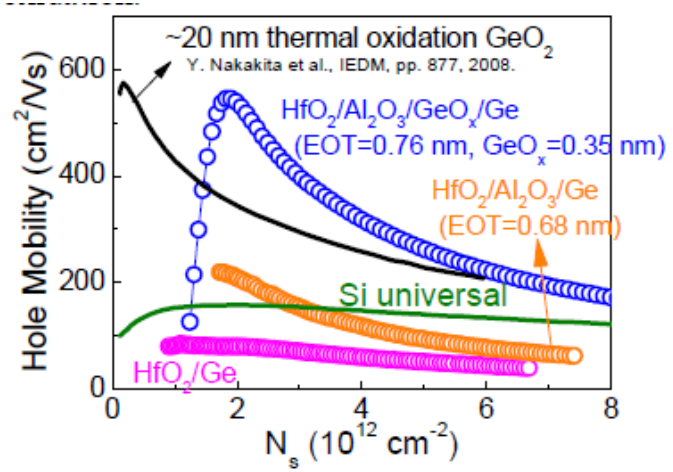
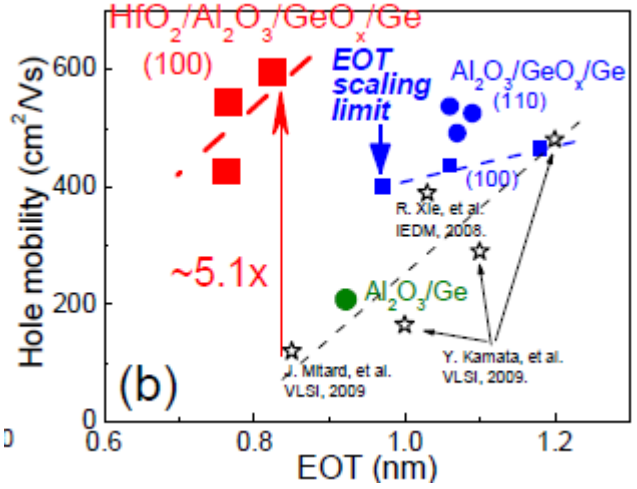


Fig. 9: Hole mobility of Ge pMOSFETs with a variety of MOS interfaces as a function of N_s



InGaAs on Si

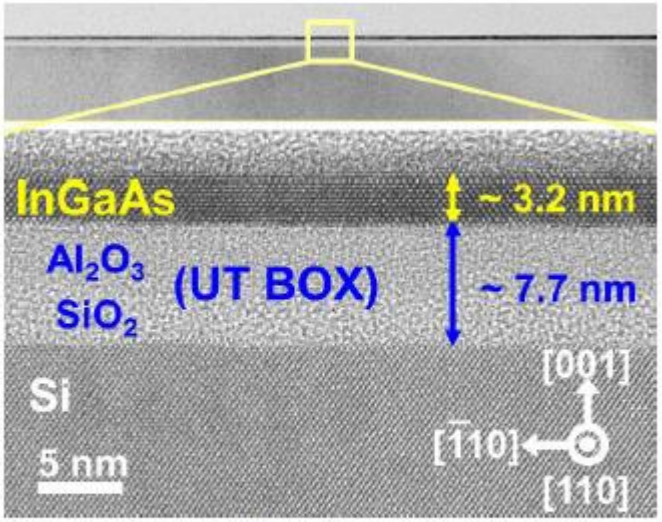


Fig. 13: TEM of a ultrathin body InGaAs substrate on Si with Al_2O_3/ SiO_2 BOX, fabricated by wafer bonding

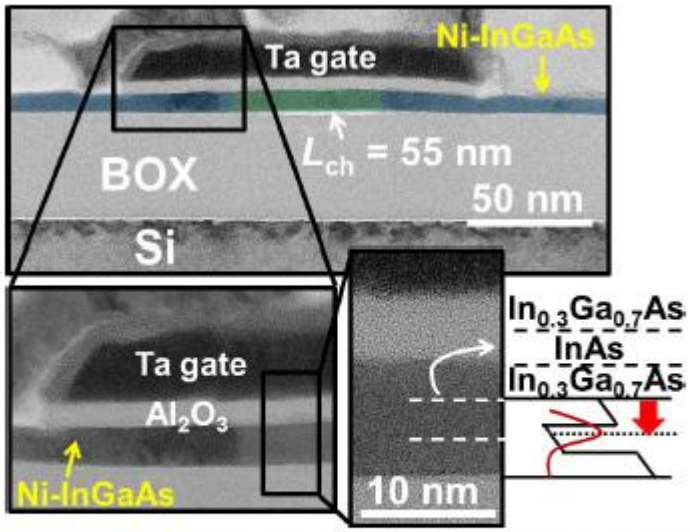


Fig. 16: TEM of 55-nm-L_g ultrathin body MOSFETs with $In_{0.3}Ga_{0.7}As$(3nm)/InAs (3nm)/$In_{0.3}Ga_{0.7}As$(3nm) and Ni-InGaAs metal S/D.

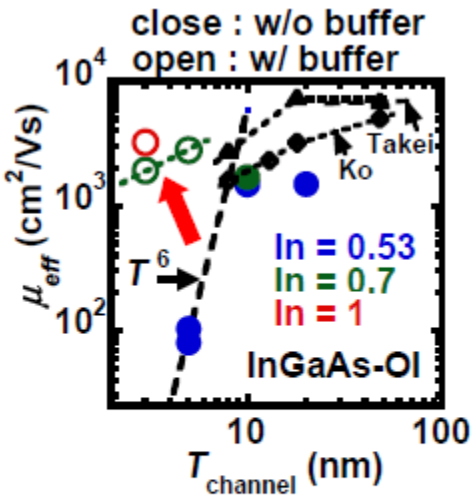


Fig. 14: Body thickness dependence of electron mobility in InGaAs/InAs-based MOSFETs.

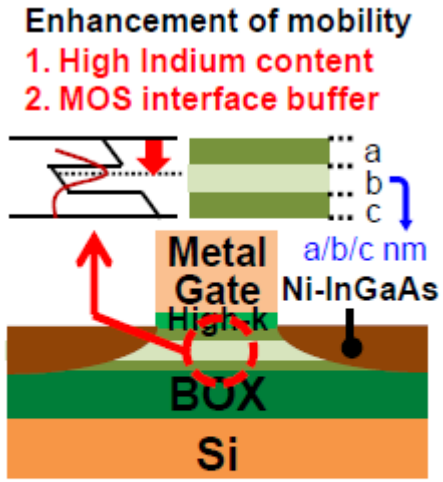


Fig. 15: MOS channel engineering for enhancing mobility in ultrathin body InGaAs-based MOSFETs.

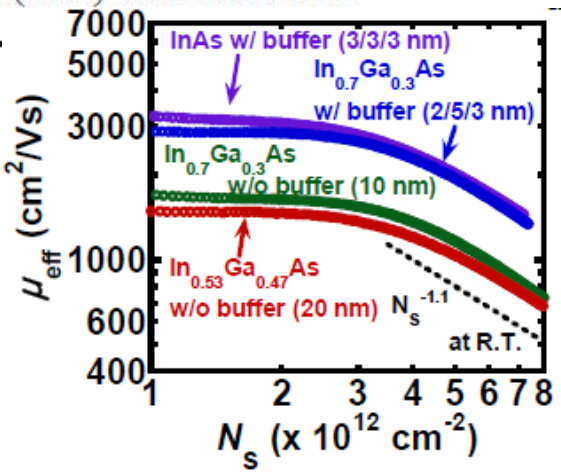


Fig. 19: N_s dependence of electron mobility at RT for InGaAs-based ultrathin body MOSFETs.

Ge and InGaAs Integration

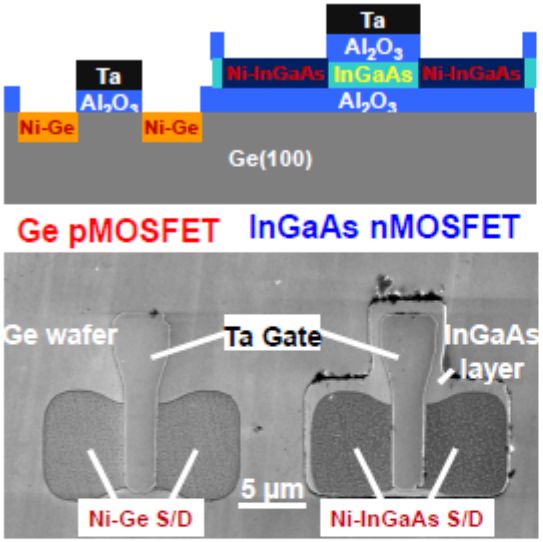


Fig. 27: Schematic view and a photograph of fabricated CMOS structure of InGaAs-OI nMOSFET and Ge pMOSFET by using common Al_2O_3-based gate stack and Ni-based S/D

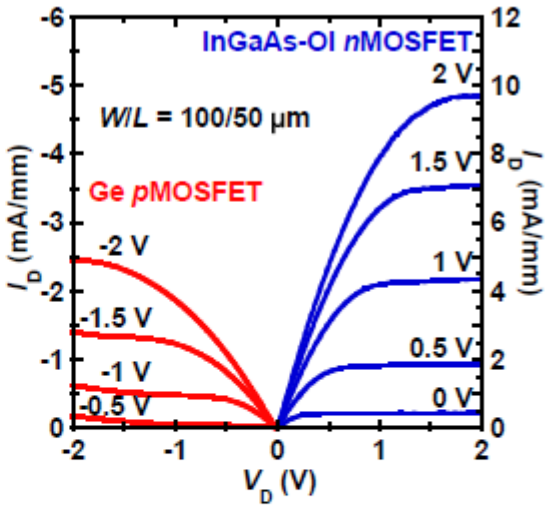


Fig. 28: I_d - V_d characteristics of a Ge pMOSFET and a 20-nm-thick InGaAs-OI nMOSFET, fabricated on a same wafer.

An Integration Path for Gate-first UTB III-V-on-insulator MOSFETs with Silicon, using Direct Wafer Bonding and Donor Wafer Recycling

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[2]Electron Microscopy Center, EMPA, Uberlandstrasse 129, 8600 Dübendorf, SWITZERLAND
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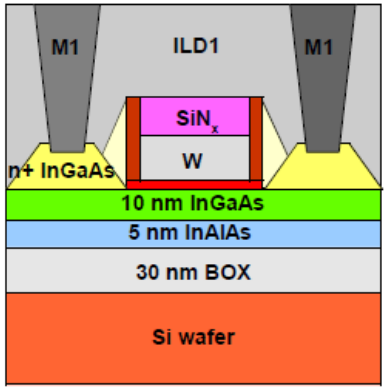


- UTB III-V transfer on Si
- High-k / Metal gate / Gate cap deposition
- Gate patterning
- Sidewall insulation
- III-V cleaning and S/D regrowth (600°C)
- ILD1 deposition and patterning
- M1 contacts

Fig. 11: Process flow and schematic for gate-first implant-free UTB InGaAs/InAlAs MOSFETs on silicon.

Wafers may be reused up to 25 times

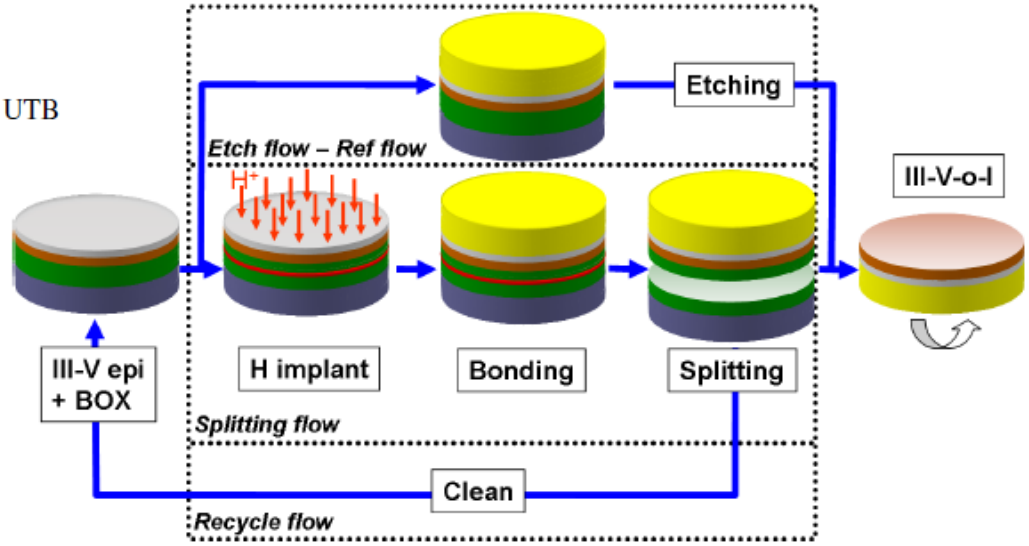


Fig. 2: Process flow of III-V-o-I wafer fabrication fully compatible with VLSI standards using DWB, hydrogen implantation, thermal splitting, selective etching and InP donor wafer re-use.

Materials Quality

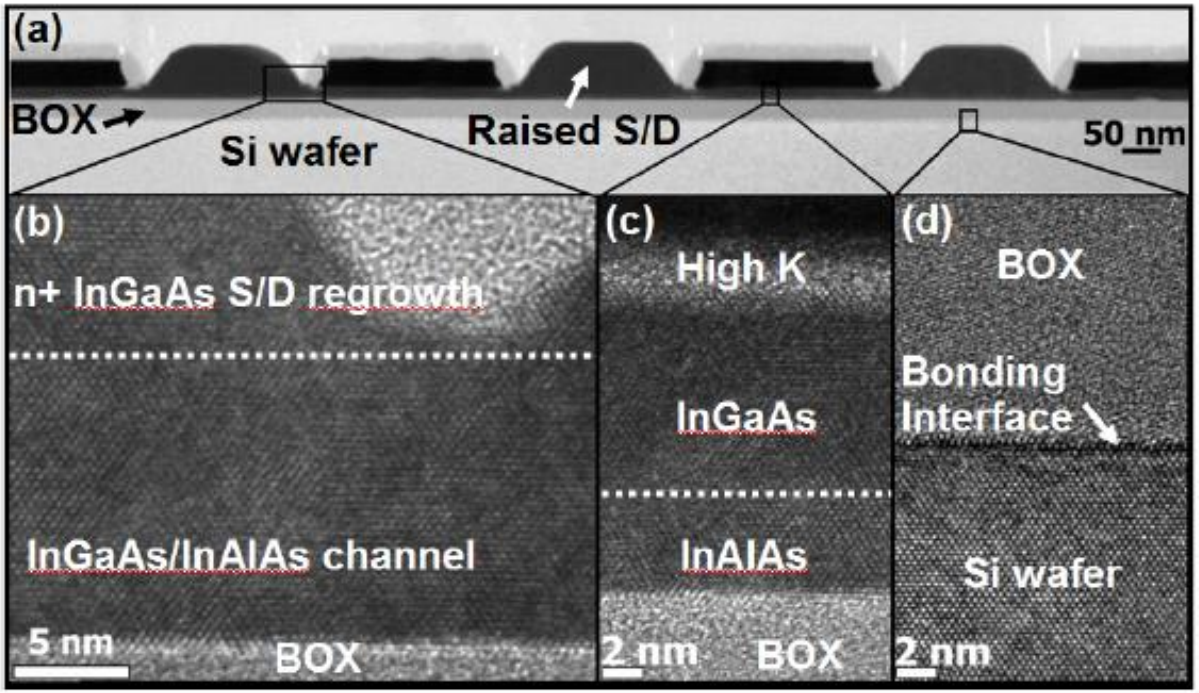
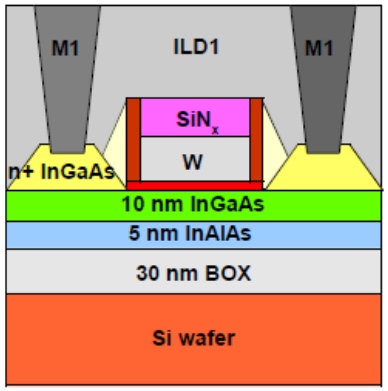


Fig. 12: (a) Cross-sectional STEM micrograph of gate-first implant-free UTB InGaAs/InAlAs MOSFETs on silicon, with raised S/D, 250 nm gate length and 500 nm gate pitch. (b) HRTEM cross-section of the UTB III-V / n+ regrowth interface showing ideal crystallinity. HRTEM cross-section of (c) the high-k / UTB III-V / BOX region and (d) the BOX-Si region showing sharp interfaces.

High material quality

InGaAs MOSFETs



- UTB III-V transfer on Si
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Fig. 11: Process flow and schematic for gate-first implant-free UTB InGaAs/InAlAs MOSFETs on silicon.

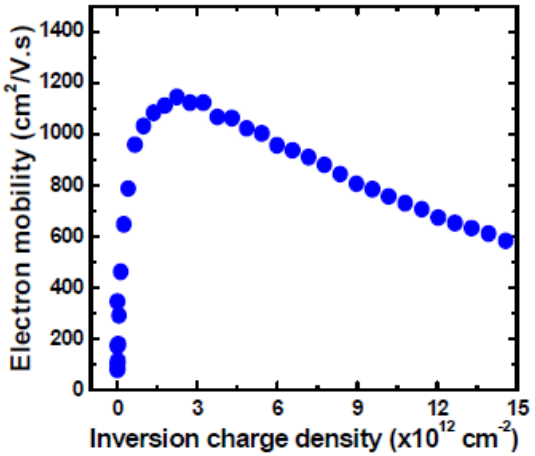
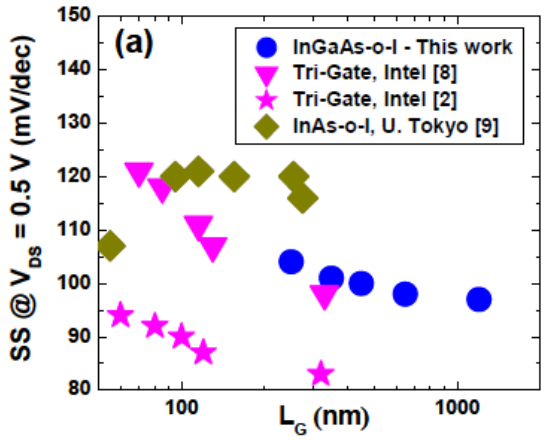
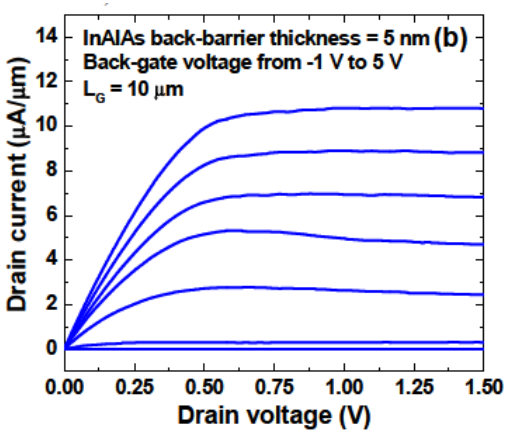


Fig. 14: Electron mobility vs inversion charge density on a long-channel MOSFET. This device exhibits a comparable mobility than previously reported devices with a similar process on bulk InP [4].

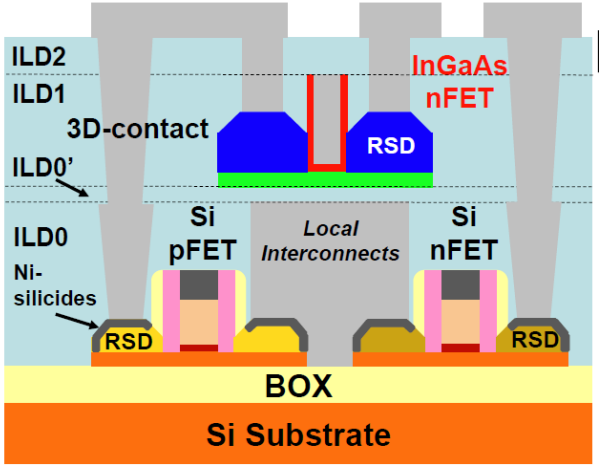




Very competitive transistor data

3D Monolithic Integration of InGaAs/Si CMOS Circuit

- **Si FDSOI CMOS prepared by LETI until W-plugs**
- **3D Monolithic integration of InGaAs FinFETs at IBM**
- **Proven no impact of InGaAs optimized process on Si FDSOI performance**



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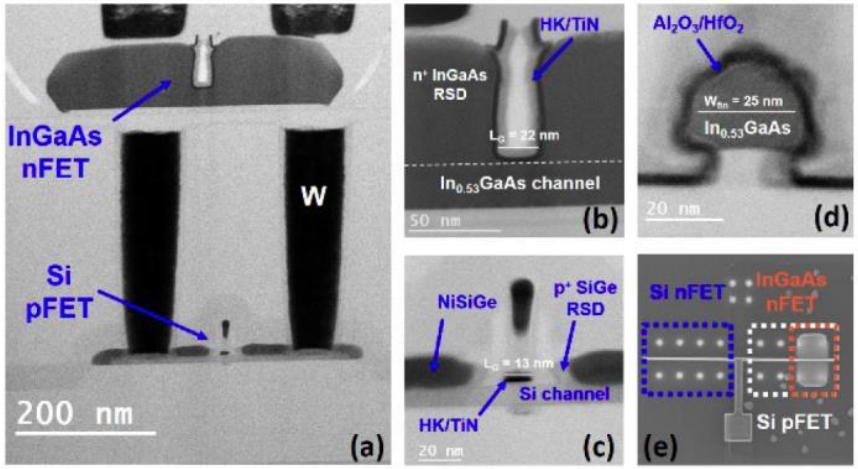
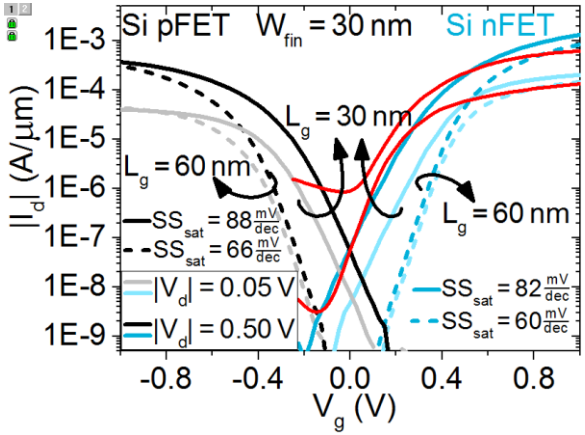
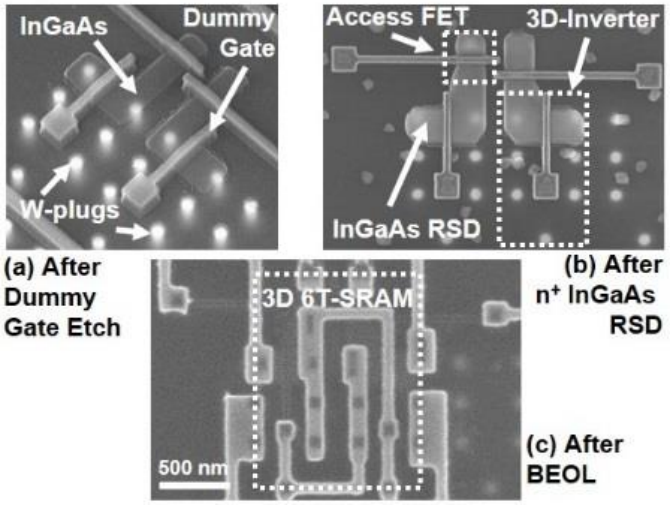


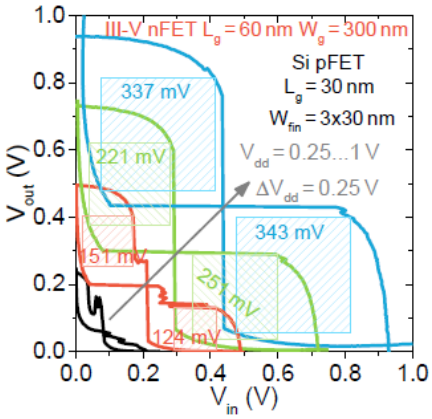
3D Integration scheme demonstrated

3D Monolithic Integration of InGaAs/Si CMOS Circuits

- **Operational Si CMOS and InGaAs n-FETs demonstrated**
- **Design, fabrication and operation of 3D 6T-SRAM cells**
- **InGaAs RFFETs also fabricated on top layer → III-V RF + Si CMOS**







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InAs-GaSb Nanowire Growth

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- **Au seeds of different diameter patterned on Si/InAs wafers using EBL.**

- **InAs-GaSb nanowires grown using MOVPE.**

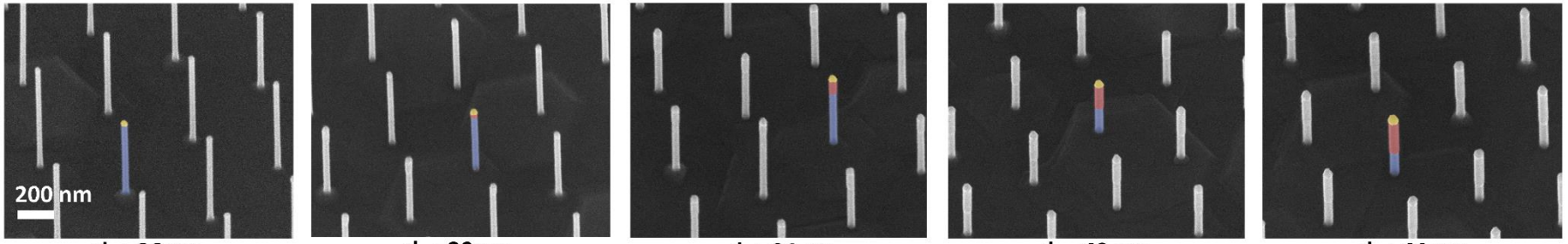
- **Gibbs-Thomson effect**

  Vapor pressure of Sb in Au increases with d_{Au} and when equal to that of gas phase, material transport to NW is inhibited.

- GaSb growth is suppressed for sufficiently small d_{Au}.

$$d_{crit} = \frac{4\gamma_a \Omega_a}{k_B T \ln\left(\frac{\alpha p_{TMSb}}{x p_v^*}\right)}$$

γ_a : surface energy of Au seed
Ω_a: molar volume of Au seed
α: utilization factor of TMSb
p_{TMSb}: precursor pressure
x: Sb fraction in seed
p^*_v: saturation vapor press



d_{Au}=26 nm | d_{Au}=30 nm | d_{Au}=34 nm | d_{Au}=40 nm | d_{Au}=44 nm

InAs-GaSb Nanowire Growth

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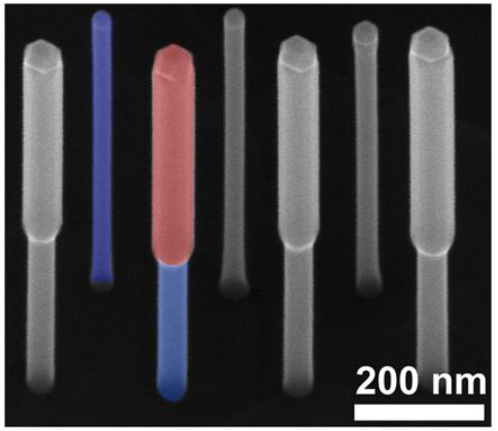
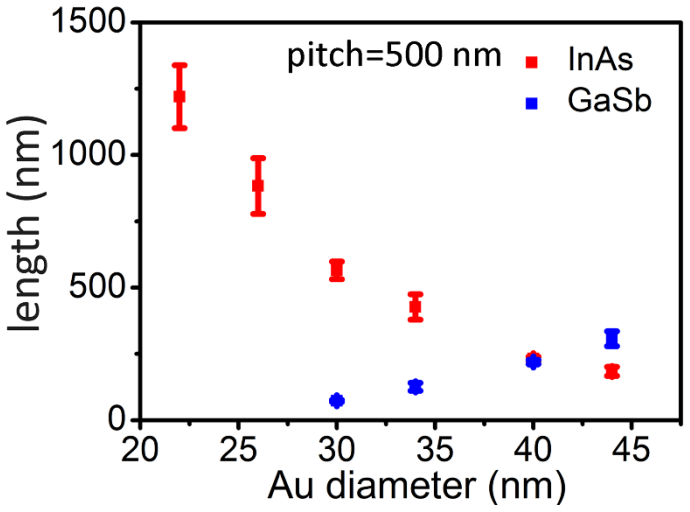
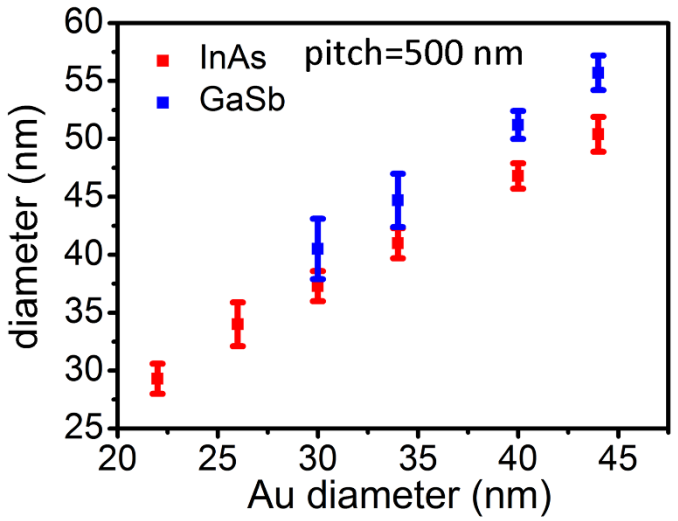
- **Length of InAs and GaSb have opposite dependence on d_{Au}.**
- **Diameter of GaSb larger than InAs since Sb enhances group III solubility in Au.**
- **Distance between two types of wires down to 200 nm.**







p- and n-MOSFET Layout

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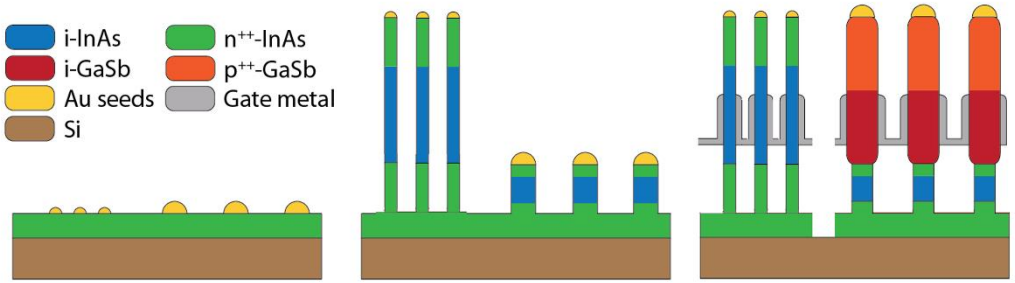
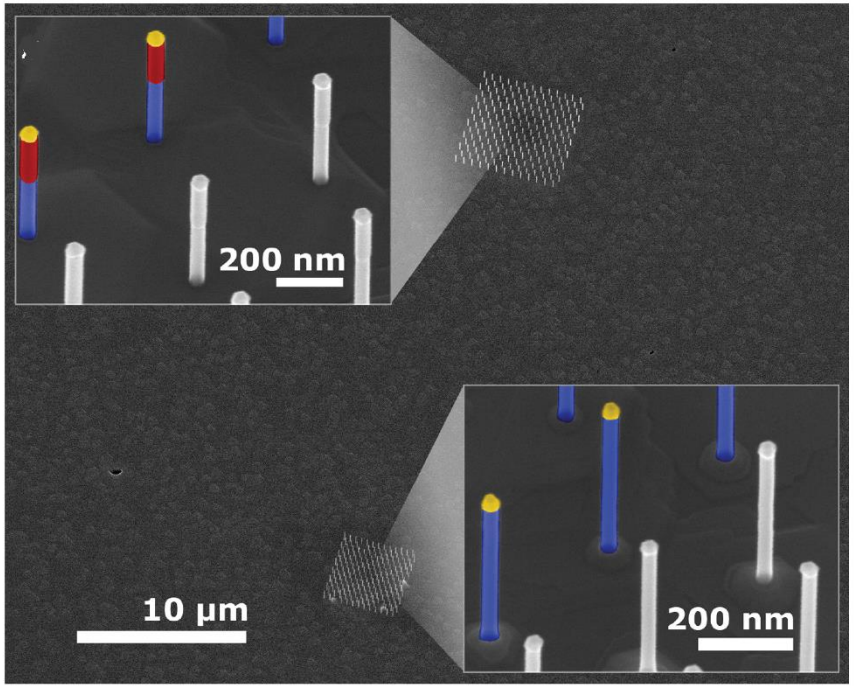
- **Tuning d_{Au} and pitch enables equal length of InAs and InAs/GaSb NWs.**

- **Doping profiles enable n.i.d. channel and good contacts.**

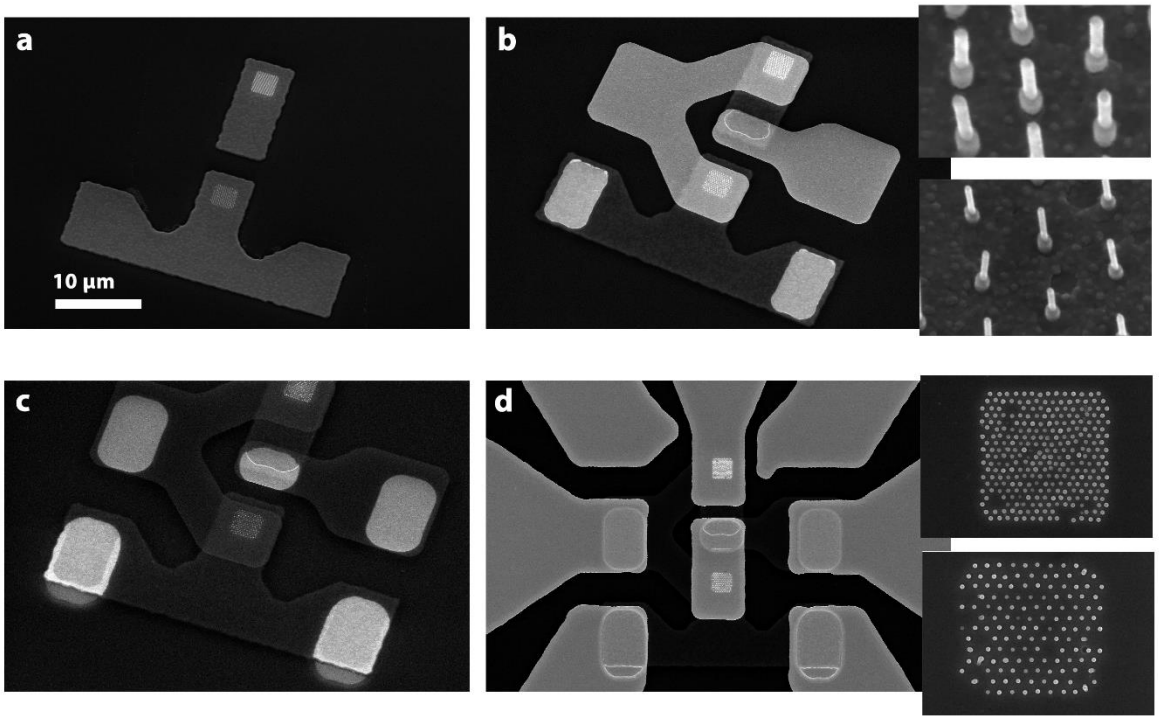


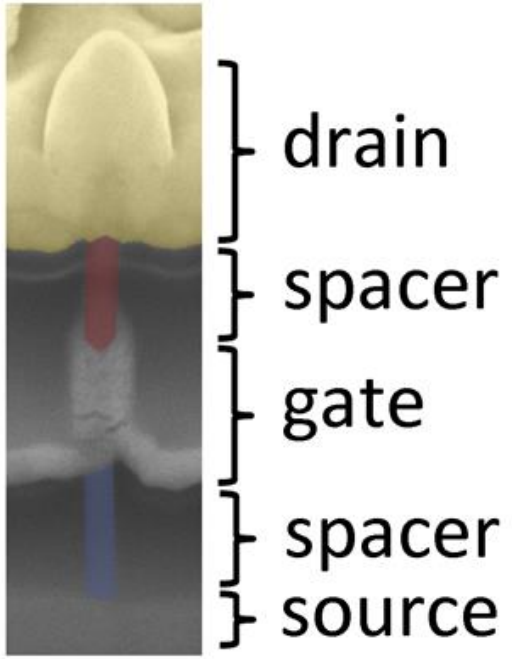


Device and Circuit Fabrication

NANO ELECTRONICS GROUP

1. High-k dep
2. InAs mesa (a)
3. Organic bottom spacer
4. W gate deposition
5. Gate length definition
5. Gate patterning (b)
6. Organic top spacer
7. Via holes (c)
8. Ni/Au drain deposition and patterning (d)





MOSFET Characteristics

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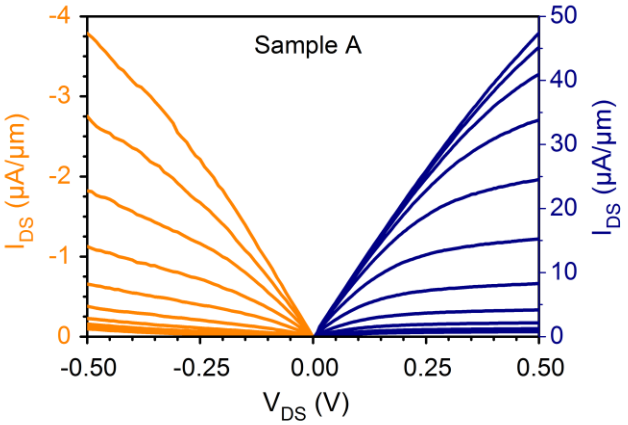
Sample A (1 nm doped GaSb shell):

InAs I_{on} = 44 μA/μm (V_{dd}=0.5V), SS = 525 mV/dec

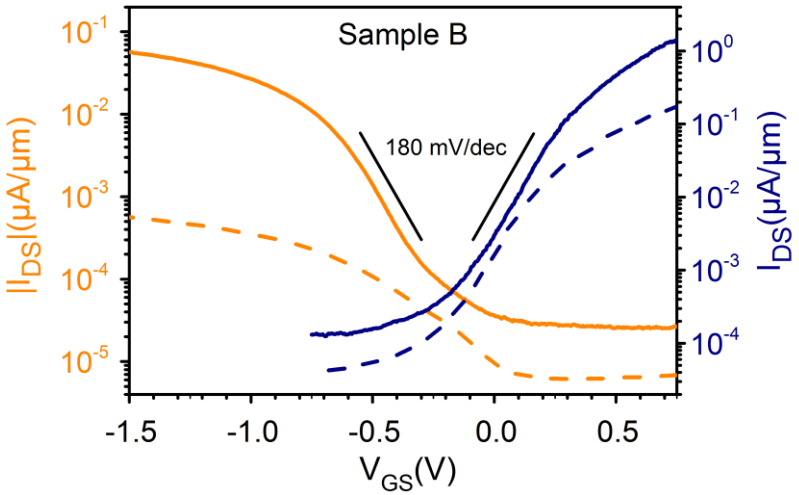
GaSb I_{on} = 7 μA/μm (V_{dd}=0.5V), SS = 300 mV/dec



Sample B (shell removed by digital etch):

InAs I_{on} = 0.1 μA/μm (V_{dd}=0.5V), SS = 180 mV/dec, $I_{on}/I_{off} = 10^3$

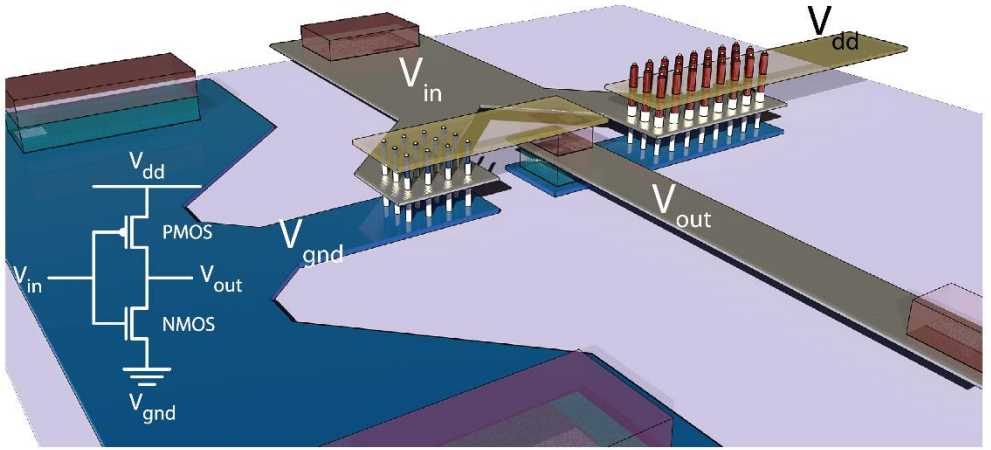
GaSb I_{on} = 0.1 μA/μm (V_{dd}=0.5V), SS = 180 mV/dec, $I_{on}/I_{off} = 10^4$

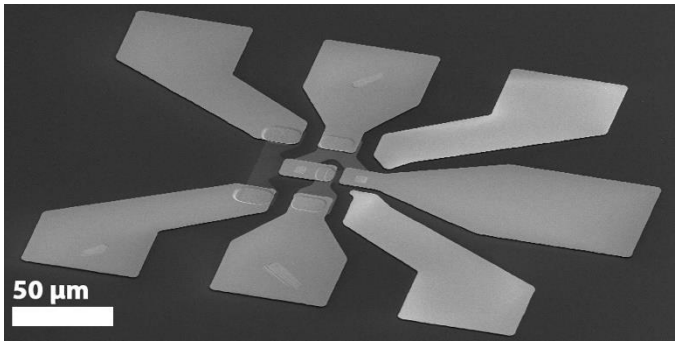


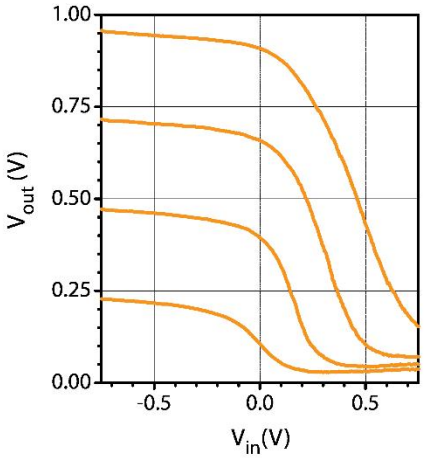
Inverter

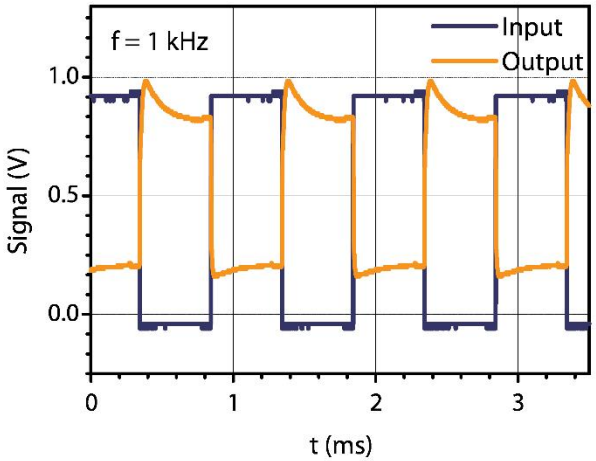
NANO ELECTRONICS GROUP

- Gain = 2 V/V (at V_{dd} = 0.5 V).
- Frequency response limited to 1 kHz due to parasitics.
- Can be improved by EBL patterned gate/drain electrodes and a self-aligned gate process.









NAND gate

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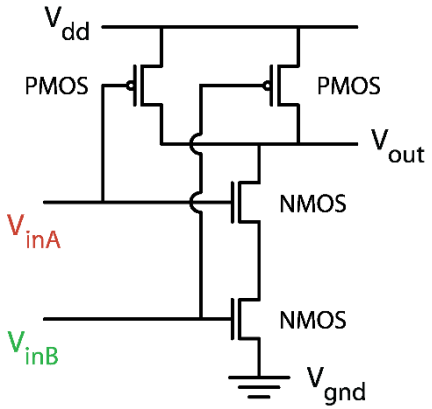
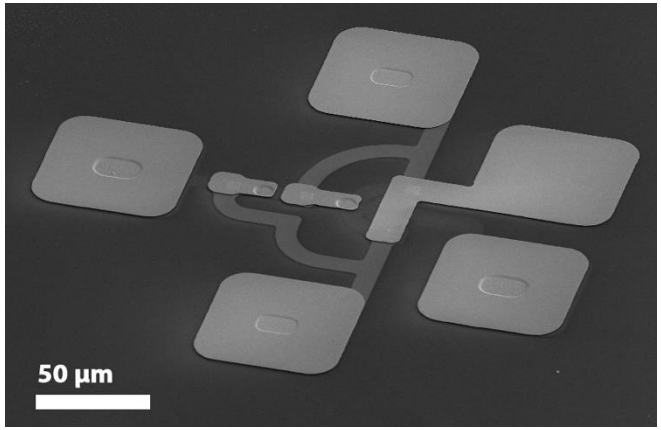
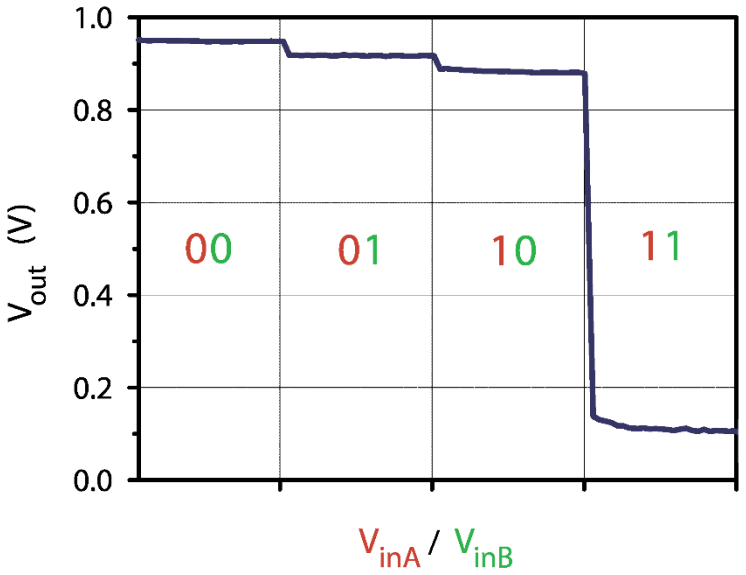
-Two p-MOSFETs in parallell + two n-MOSFETs in series.





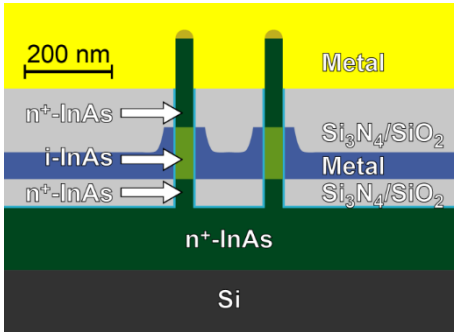


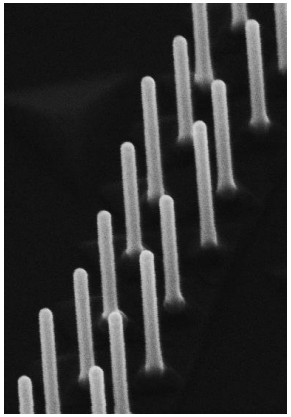
Why III-V Nanowires

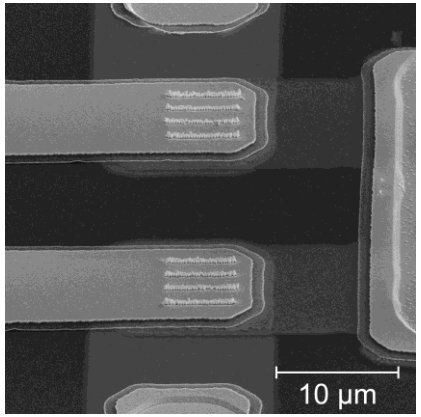
NANO ELECTRONICS GROUP

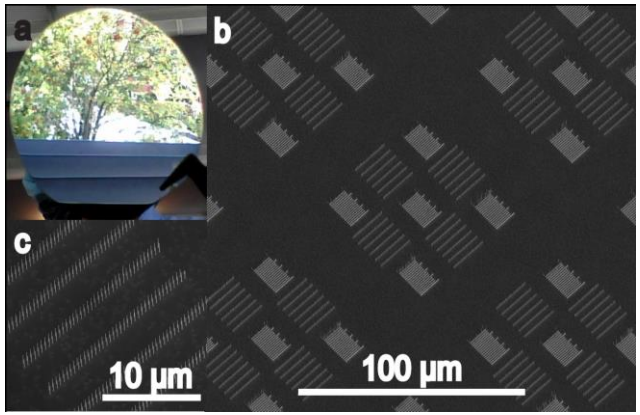
Why III-V Nanowires?

- **Advantageous transport → high transconduc. and I_{on}**
- **Wrap-gate geometry → low output conduc. and DIBL**
- **Band gap engineering → increased breakdown, reduced I_{off}**
- **Small nanowire footprint → reduced defect propagation probability**





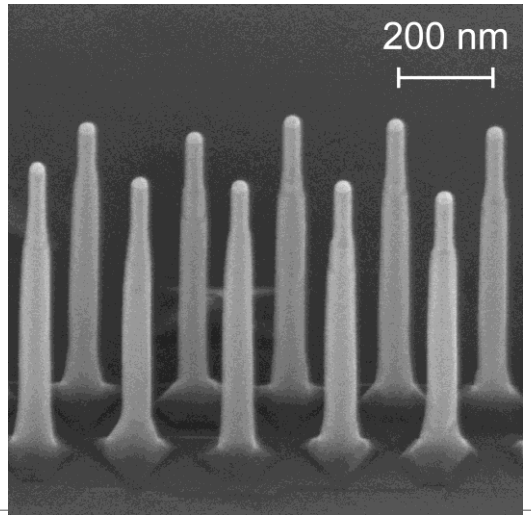




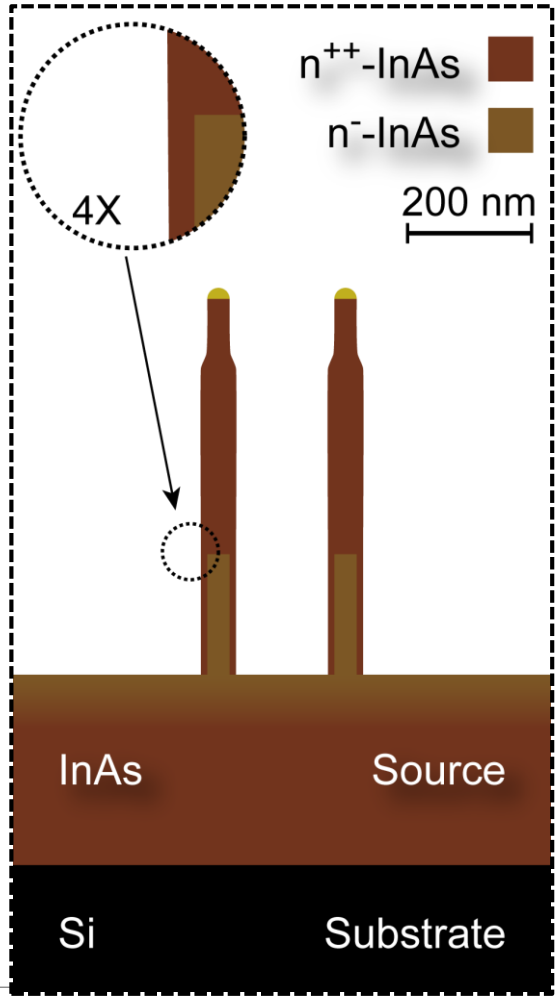
Gate-Last Process

NANO ELECTRONICS GROUP

- Nanowire growth
- Drain contact formation
  - HSQ/W/TiN
  - RIE Metal Etching
- SiO_2 Spacer formation
- Digital etching, HCl
- ALD High-*k*
  - Al_2O_3/HfO_2 300/120°C
- W Gate formation
- Organic spacer
- Device completion



Core Diameter 35 nm
10 nm overgrowth



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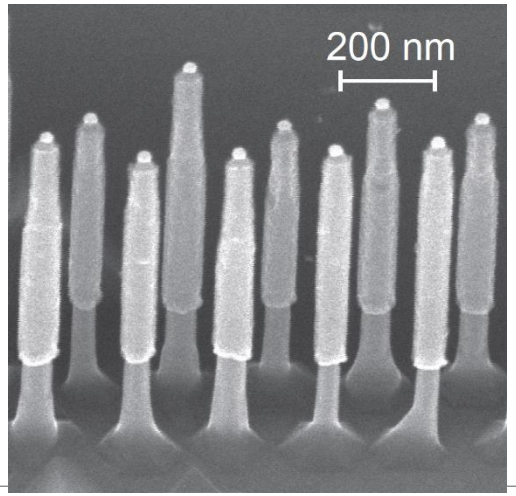

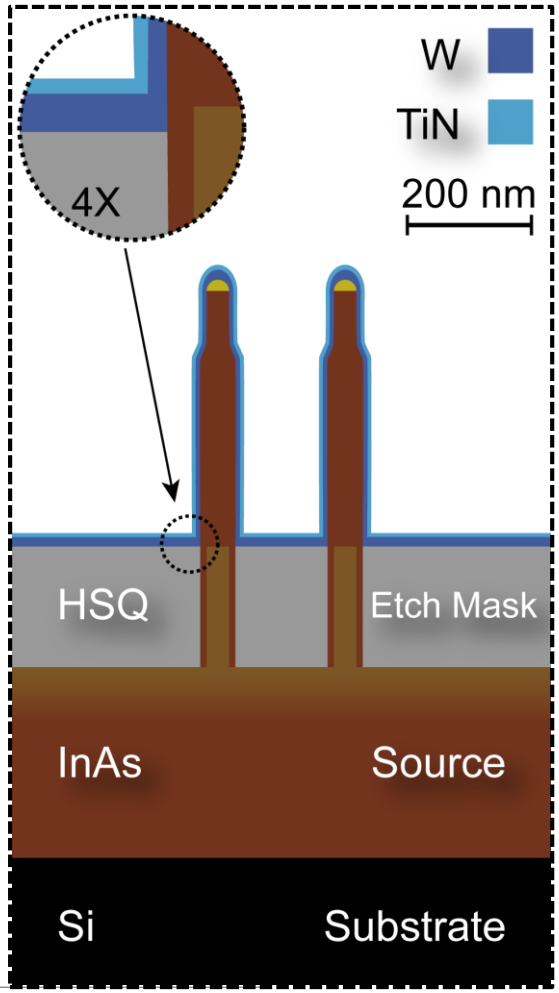

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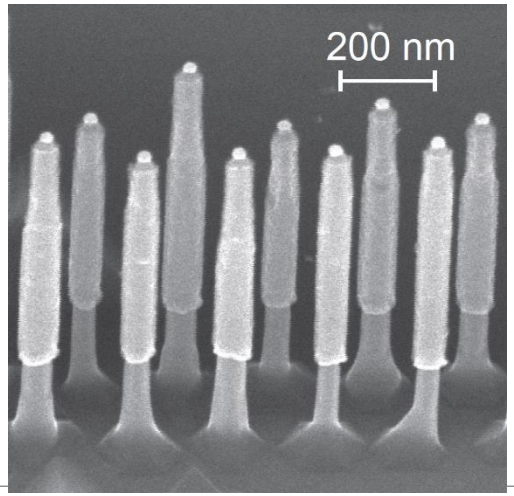

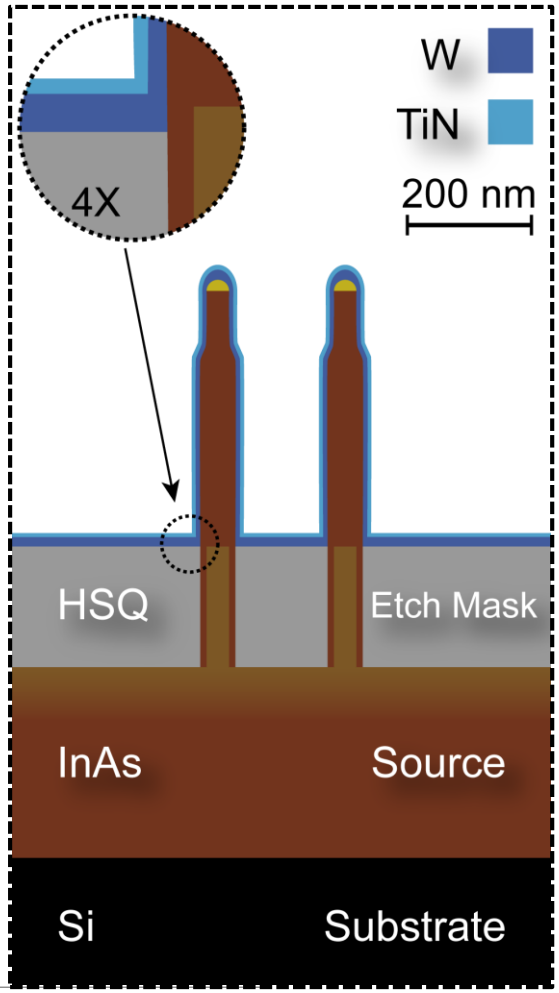

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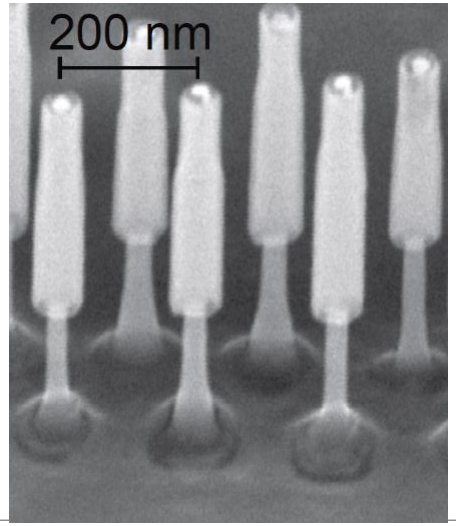
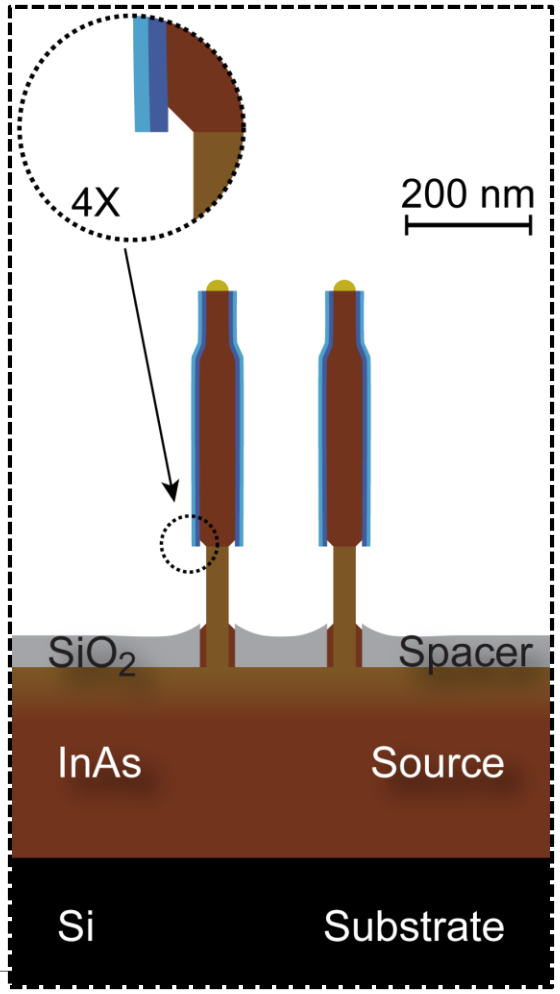


Diameter 28 nm



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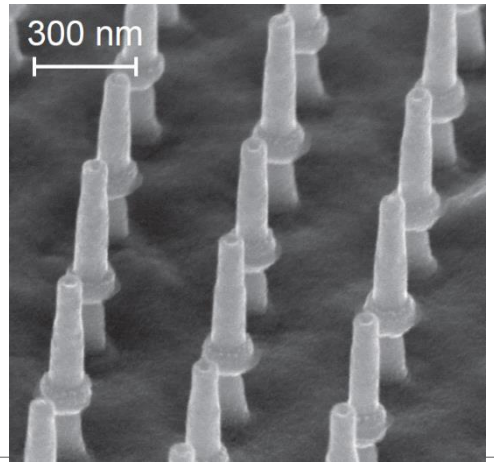

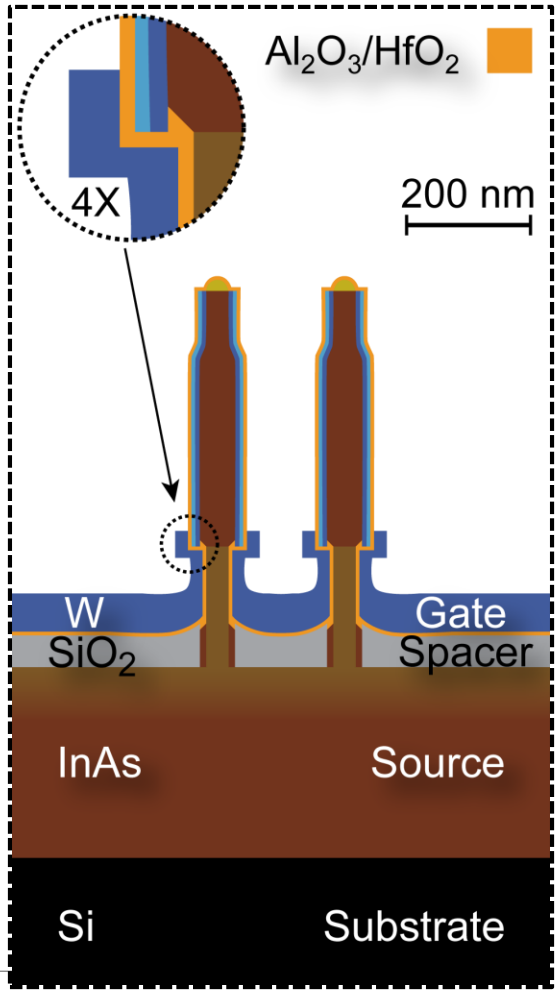

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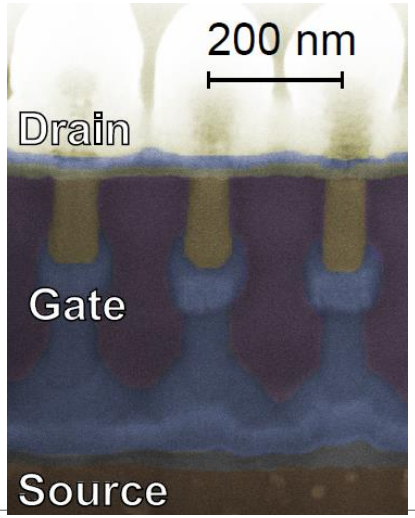

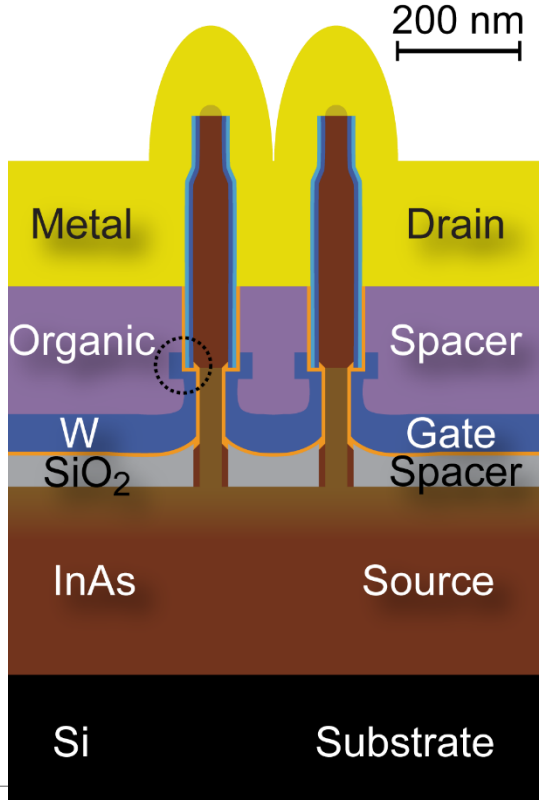

M. Berg et al., IEDM 2015

Gate-Last Process

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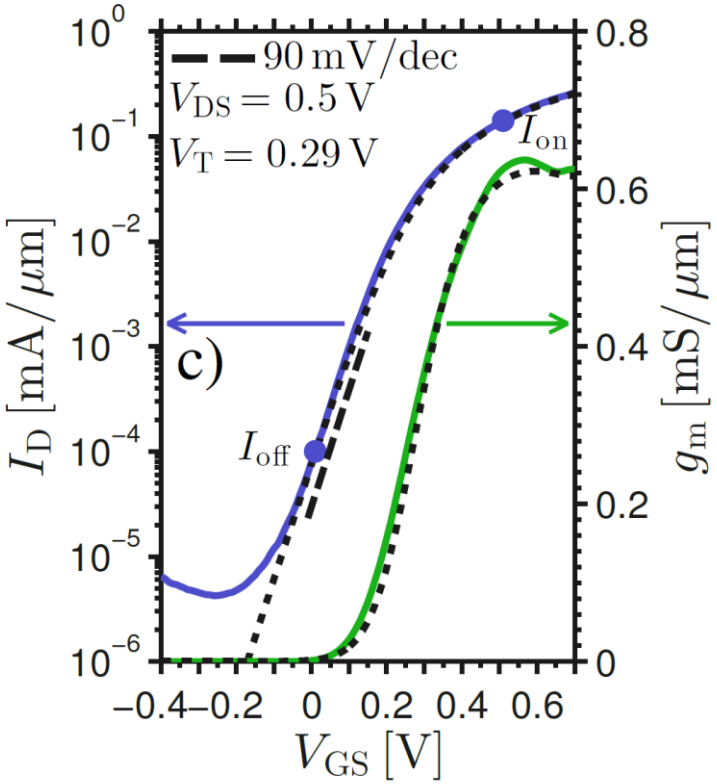
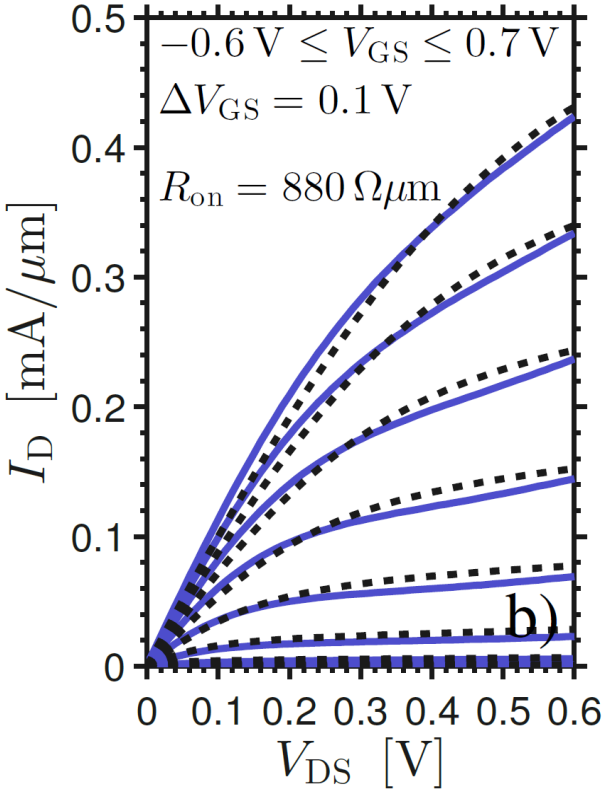
Best digital metric:

I_{on}=140 µA/µm, SS= 90 mV/dec

RF metric:

g_m=1.1 mS/µm, µ=1200 cm²/Vs





L_g 190 nm, EOT 1.5 nm, Ø 28nm

M. Berg et al., IEEE EDL 2016

Trap Distribution

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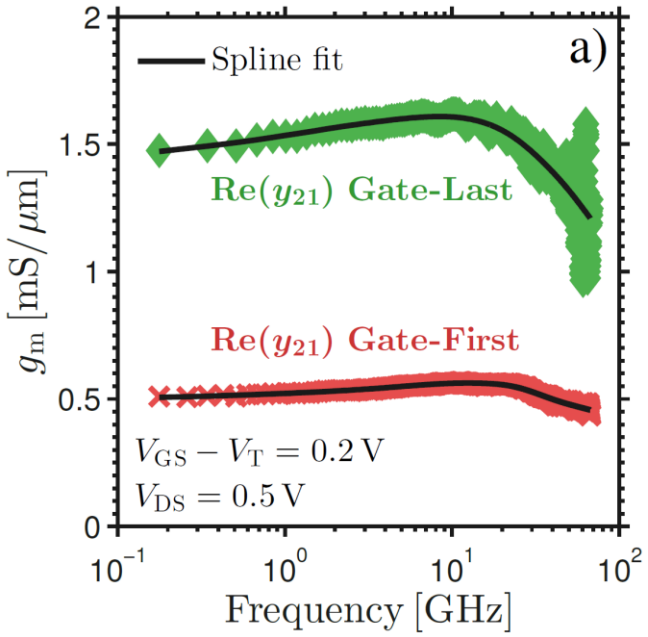
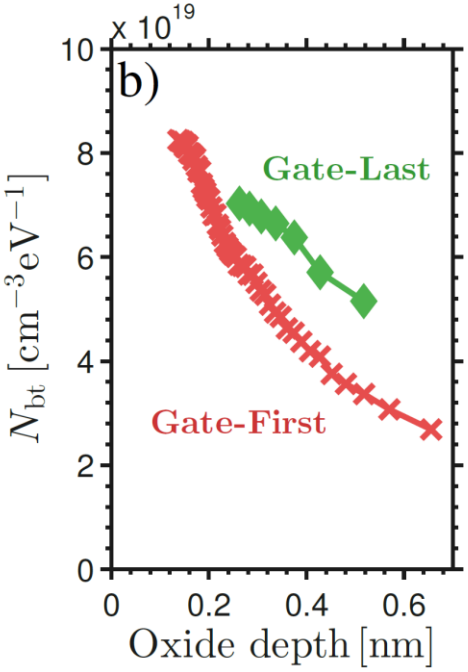
Use of g_m-f method





10 cylces Al_2O_3
40 cycles HfO_2
EOT 1.5 nm

$$N_{bt}(x) = \frac{(C_{ox} + C_s)\cdot g_{mi}}{q\lambda \cdot \left(1 - x_m(\omega)/t_{ox}\right)\cdot g_m^2(\omega)} \cdot \frac{\partial g_m(\omega)}{\partial \ln(\omega)}$$

$x_m = \lambda \ln(\omega/\omega_0)$
λ: decay rate of wavefunction

M. Berg et al., IEEE EDL 2016

LETTER

doi:10.1038/nature11293

A III–V nanowire channel on silicon for high-performance vertical transistors

Katsuhiro Tomioka[1,2], Masatoshi Yoshimura[1] & Takashi Fukui[1]

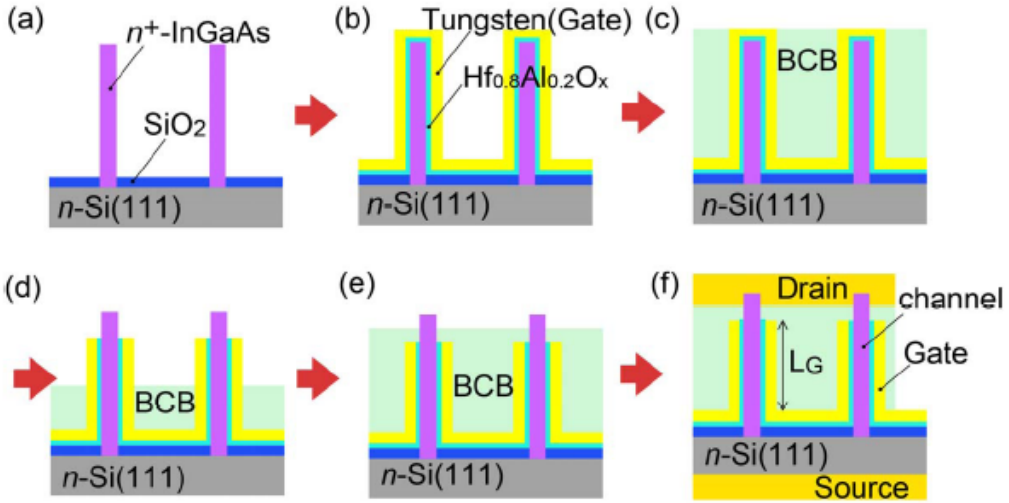
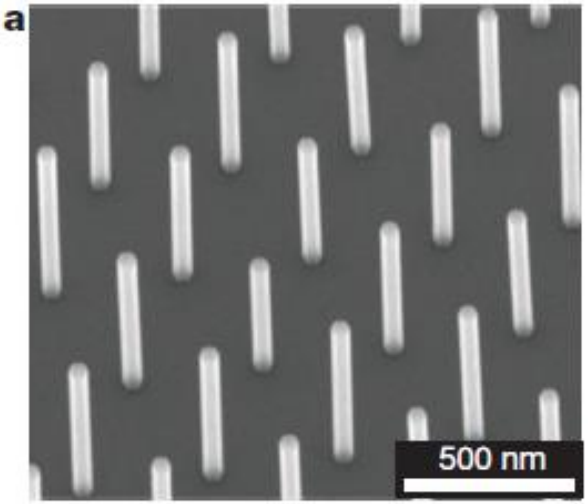
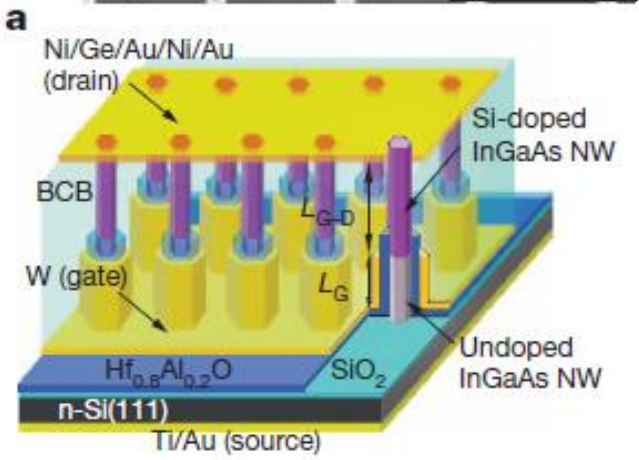


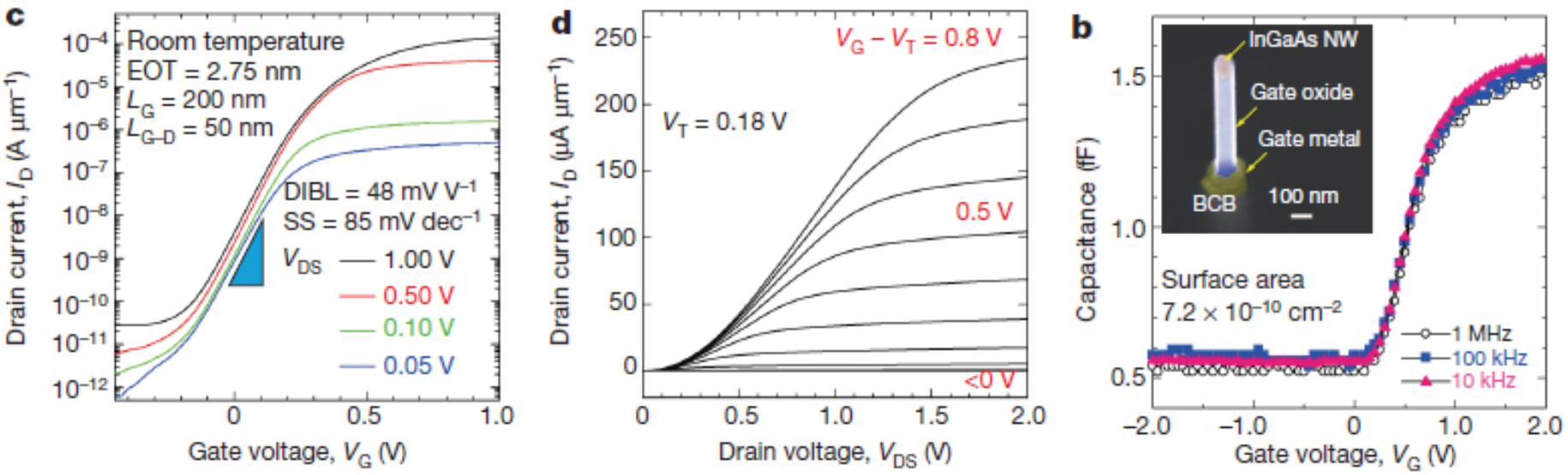
Figure 3: Device fabrication processes: (a) InGaAs NW growth. (b) Atomic layer deposition of $Hf_{0.8}Al_{0.2}O_x$ and sputtering of W-gate metal. (c) Spin-coating of BCB polymer. (d) RIE of BCB, gate oxide and W metal. (e) Spin-coating of BCB and RIE etch back for electrical separation layer formation. (f) Drain and source metal evaporation.





Nanoelectronics: III-V Nanowires

Device Performance



Gate length 200 nm

Nanowire diameter 60 nm

10 nanowires in the array

Transconductance of 280 µS/µm at Vd=1V

SS 98 mV/dec.

Device Performance

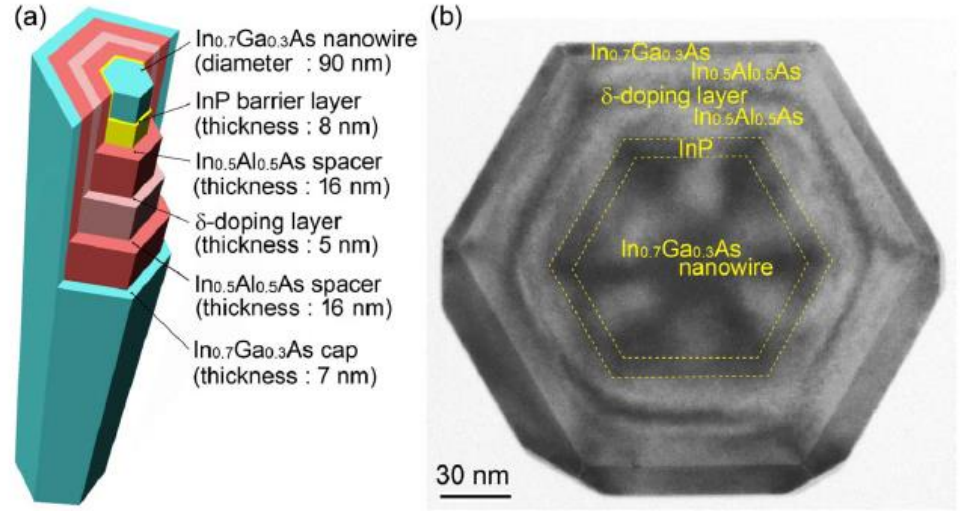
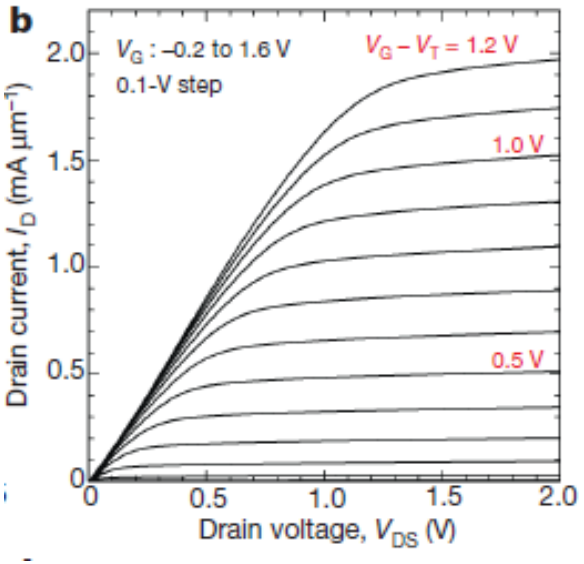
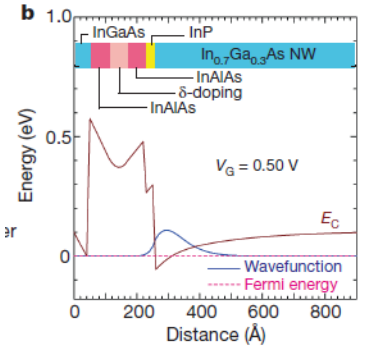
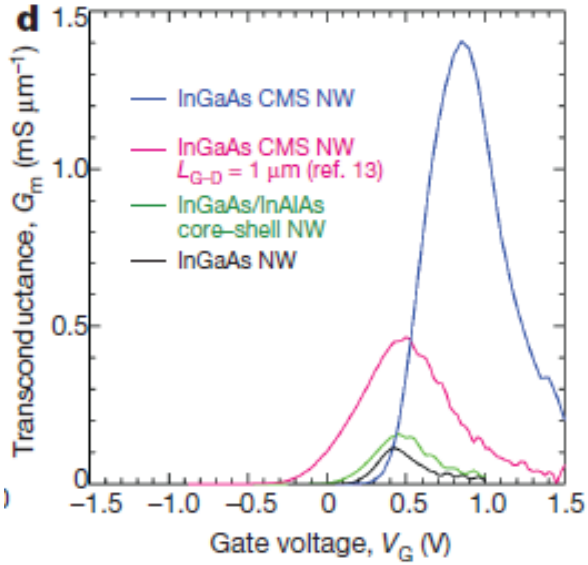


Figure 9: (a) Illustration of InGaAs/InP/InAlAs/δ-dope InAlAs/InAlAs/InGaAs core-multishell NW. (b) Cross-section TEM image of the growth results of Fig. 9(a). The InGaAs NW is 90 nm in diameter.







Gate length 200 nm

Nanowire diameter 90 nm

10 nanowires in the array

g_m=1.42 mS/μm at V_d=0.5 V

SS 75 mV/dec.