Lecture 8: Heterogeneous Integration II

Contents:

Nanowire Capacitors:
J. Wu et al Nano Letters, 16, 2016, p 2418 ” Low Trap Density in InAs/High-k Nanowire... ”

Negative Capacitance:
S Salahuddin et al Nano Letters, 8, 2008, p 245 ” Use of Negative Capacitance ...”

Ferroelectric HfO_2:
P. Polakowski et al Applied Phys. Lett. 106, 215, p. 232905 ” Ferroelectricity...”

Negative Capacitance FETs:
D. Kwoon et al IEEE Electron Dev Lett. 39, 2018, p 300 ” Improved Subthreshold....”

Microelectronic Engineering 88 (2011) 1061–1065

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Is interfacial chemistry correlated to gap states for high-k/III–V interfaces?

W. Wang, C.L. Hinkle, E.M. Vogel, K. Cho, R.M. Wallace *

Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080, USA

ALD critical for III-V MOS structures

Alternative cycles of metal and oxide

Has self cleaning effect

Reaction at interface detected by XPS

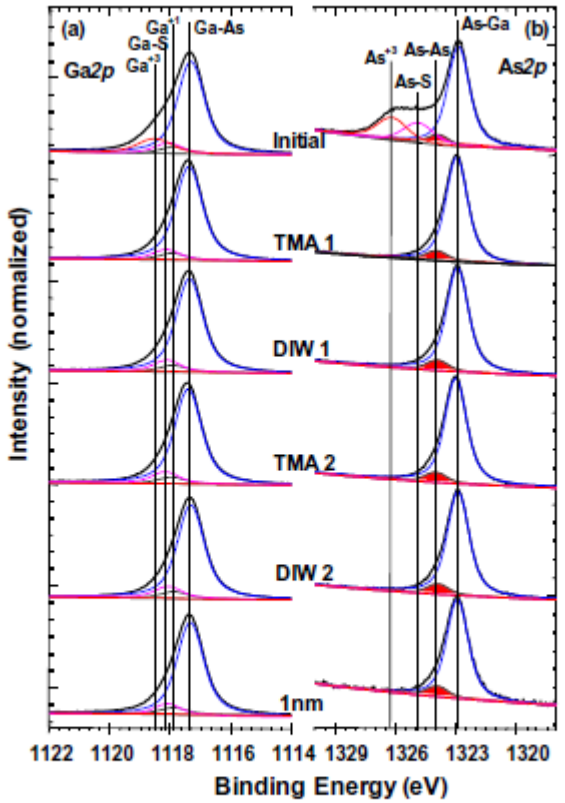


Fig. 4. *In situ* half-cycle ALD study of S-passivated GaAs showing (a) Ga 2p and (b) As 2p regions. The As-shaded feature corresponds to As–As bonding. Reprinted with permission from [28], © 2008, American institute of physics.

The Bad Guys

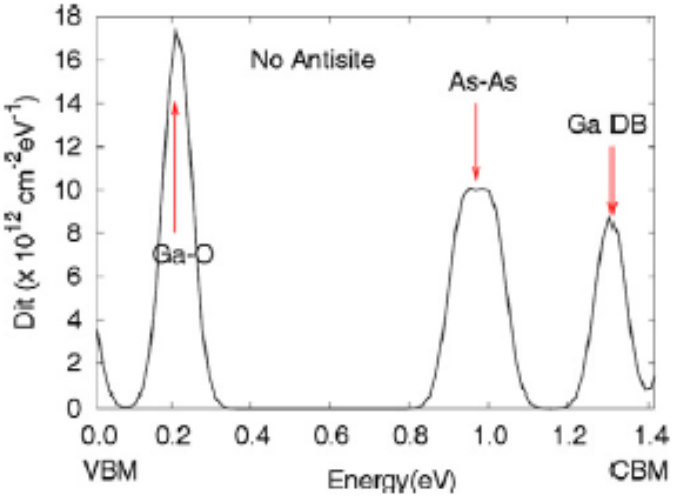


Fig. 6. Density of states calculated from the O-rich HfO_2/GaAs interface. The As–As dimer defect is seen to result in a significant density near the midgap, while Ga db and "Ga +3-like" states contribute near the band edges.

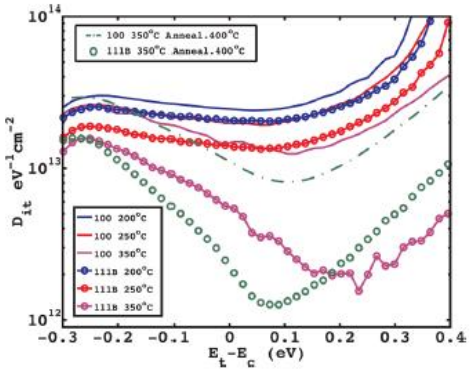


FIG. 2. D_{it} vs. E_t - E_c extracted using the low frequency fitting method (see Ref. 14) as a function of InAs orientation and oxide deposition temperature. The x-axis denotes the position of the trap level E_t in the band gap with respected to the conduction band edge E_c.

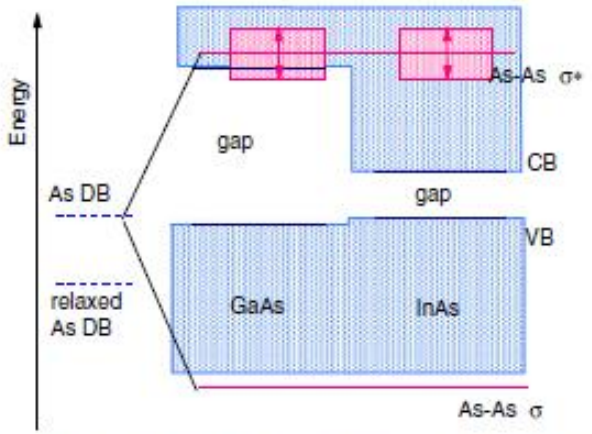


Fig. 4. Creation of bonding and antibonding states (σ and σ*) from As–As bonds, related to the band energies.

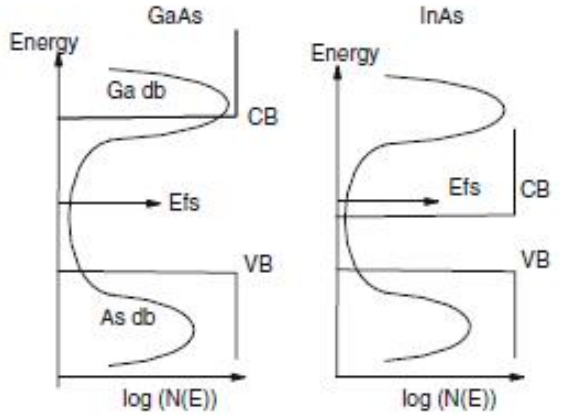
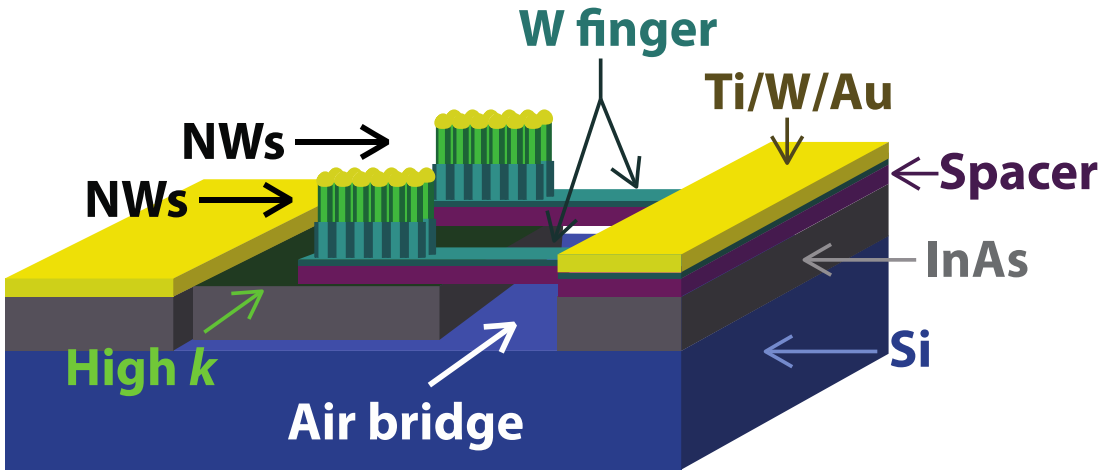


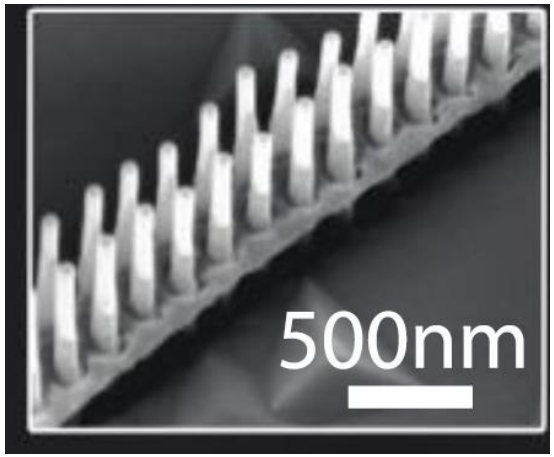
Fig. 5. Schematic of the density of interface states for GaAs and InAs, compared to the bulk band states, and their charge neutrality levels (CNL)/Fermi level stabilisation energies.

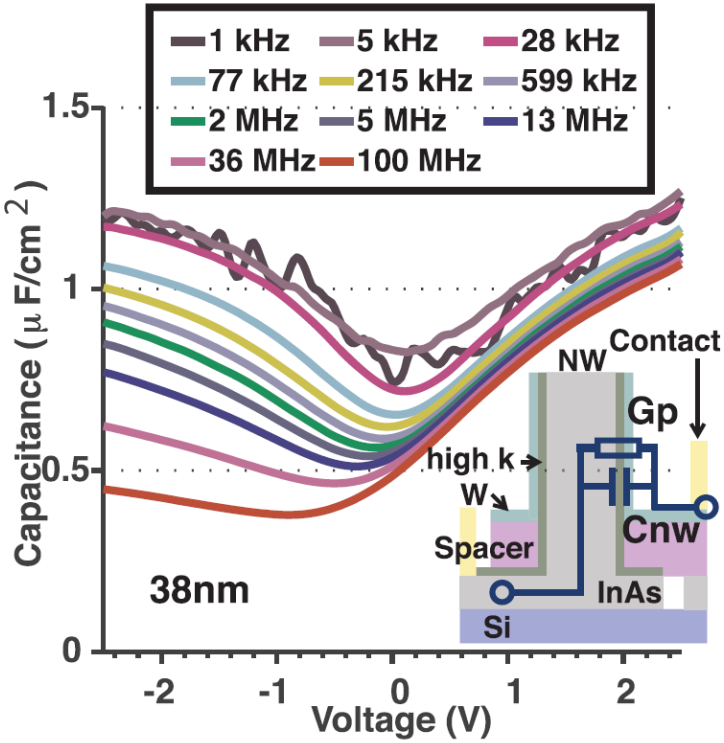
N S

CV for InAs Nanowires: Gen 1

NANO ELECTRONICS GROUP





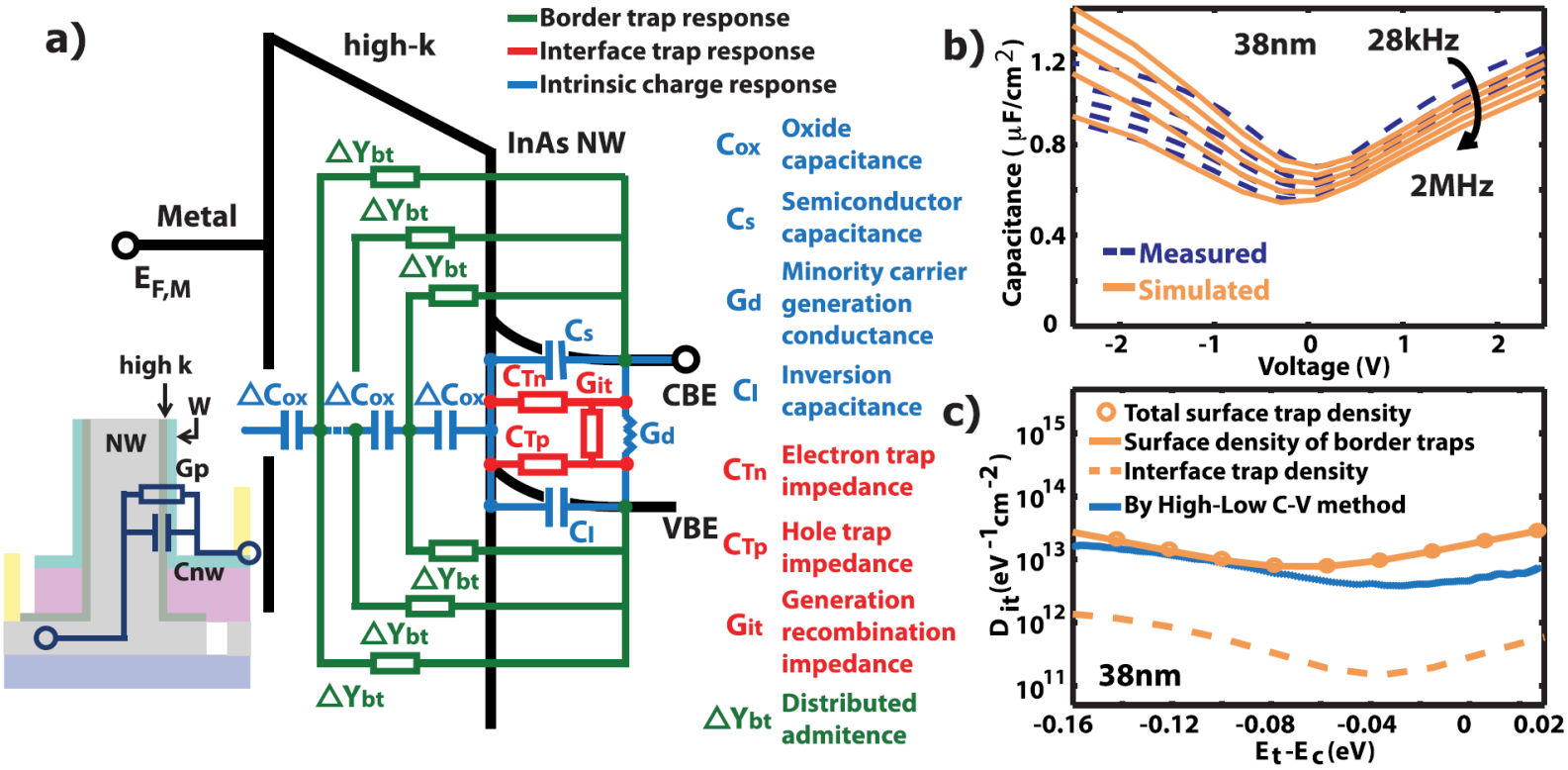


J. Wu et al., IEEE T-ED 2016

Vertical Nanowire Capacitors, T_{growth} 420 C
Doped bottom segment, Sputtered W
ALD @ 250/100C EOT 1.5 nm
Low Parasitic Capacitance
Good CV Modulation

Interpretation of the CV Data

NANO ELECTRONICS GROUP

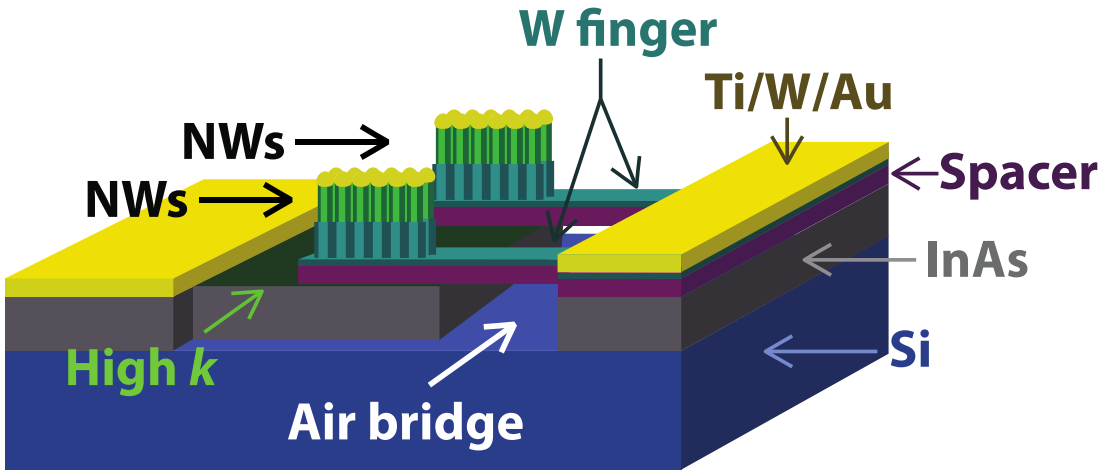


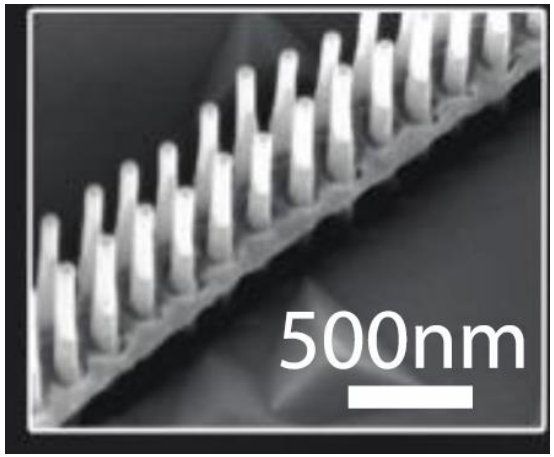
Data interpreted with a combined model with interface traps and border traps

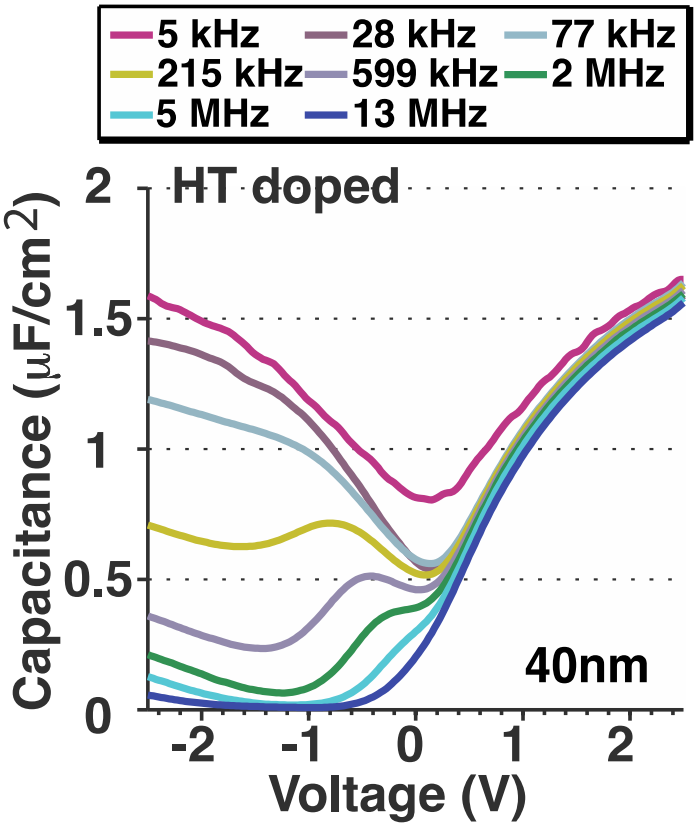
Similar N_{bt} to planar InAs references

Lower D_{it} than planar InAs references

Low D_{it} on InAs Nanowires: Gen 2





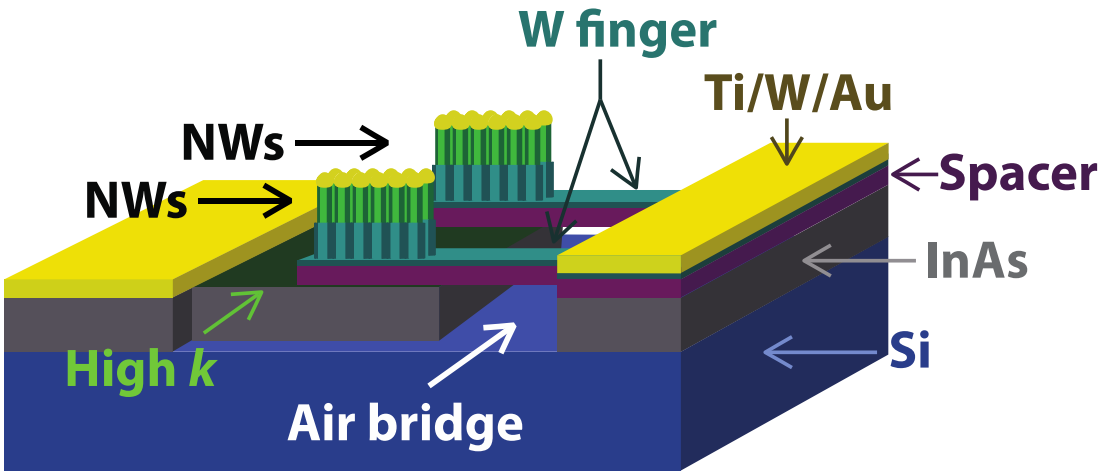


Vertical Nanowire Capacitors
ALD @ 250C EOT 1.7 nm
Low Parasitic Capacitance
Good CV Modulation

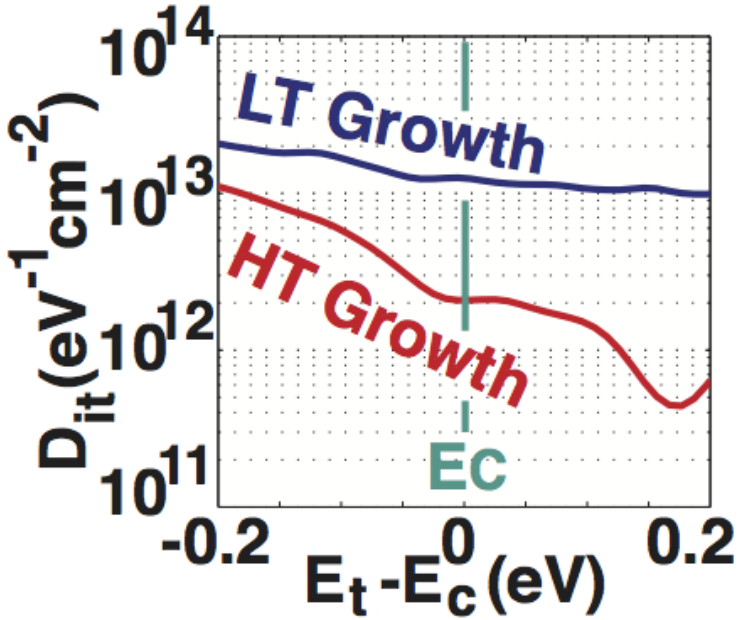
J. Wu et al., IEEE T-ED 2015

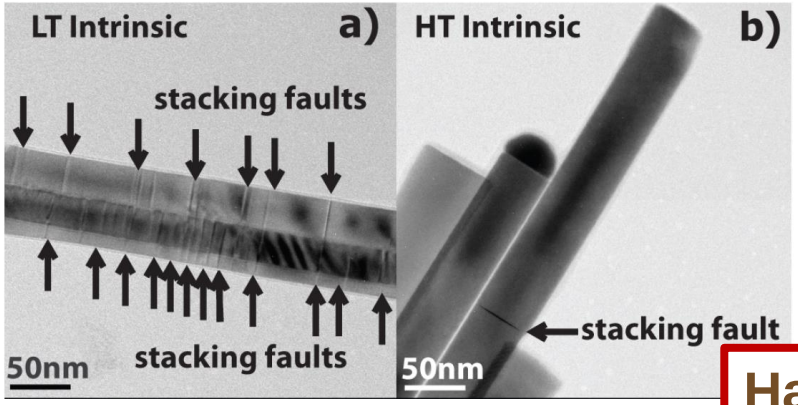
Low D_{it} on InAs Nanowires

NANO ELECTRONICS GROUP



Low-Frequency CV Fitting
Low D_{it} ($<10^{12}$ $ev^{-1}cm^{-2}$) around E_c





Has an InAs nanowire less traps?
WZ crystal structure, larger E_g
WZ crystal structure, more stable facets
Nanowire geometry, less volume for minority generation

J. Wu et al., Nano Lett. 2016

What if we use a Ferroelectric Insulator?

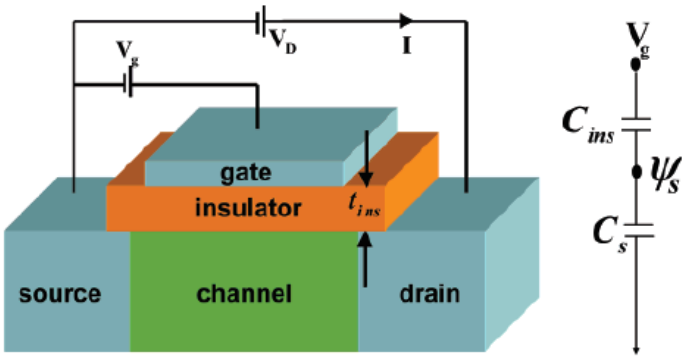


Figure 1. A standard FET structure where the current I in the drain circuit is controlled by the gate voltage V_g. The right panel shows an equivalent circuit for the division of the gate voltage between the insulator capacitance and the semiconductor capacitance (that comprises of the depletion, channel to source and channel to drain capacitances).

Use a series connection to stabilize the negative capacitance!

Surface potential in the channel

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}}$$

$$S \equiv \frac{\partial V_g}{\partial(\log_{10} I)} = \frac{\partial V_g}{\underbrace{\partial \psi_s}_{\equiv m}} \frac{\partial \psi_s}{\partial(\log_{10} I)}$$

Landau-Kahlatnikov relation:

$$\rho \frac{d\vec{P}}{dt} + \nabla_{\vec{P}} U = 0$$

$$E_{ext} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt}$$

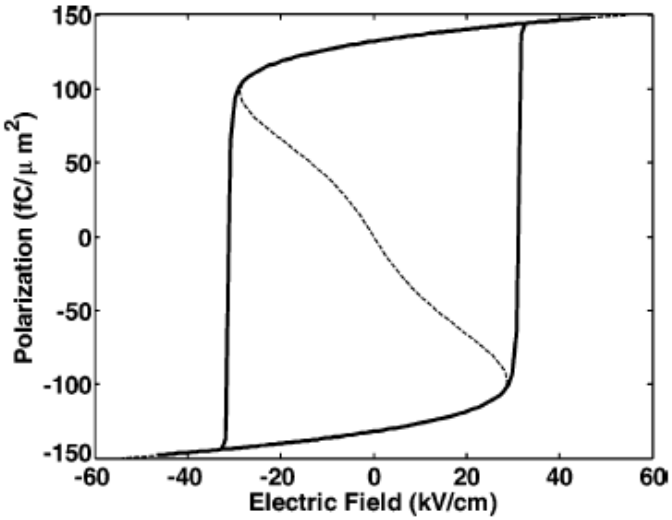
Use: $Q = P \qquad V = E_{ext} t_{ins}$

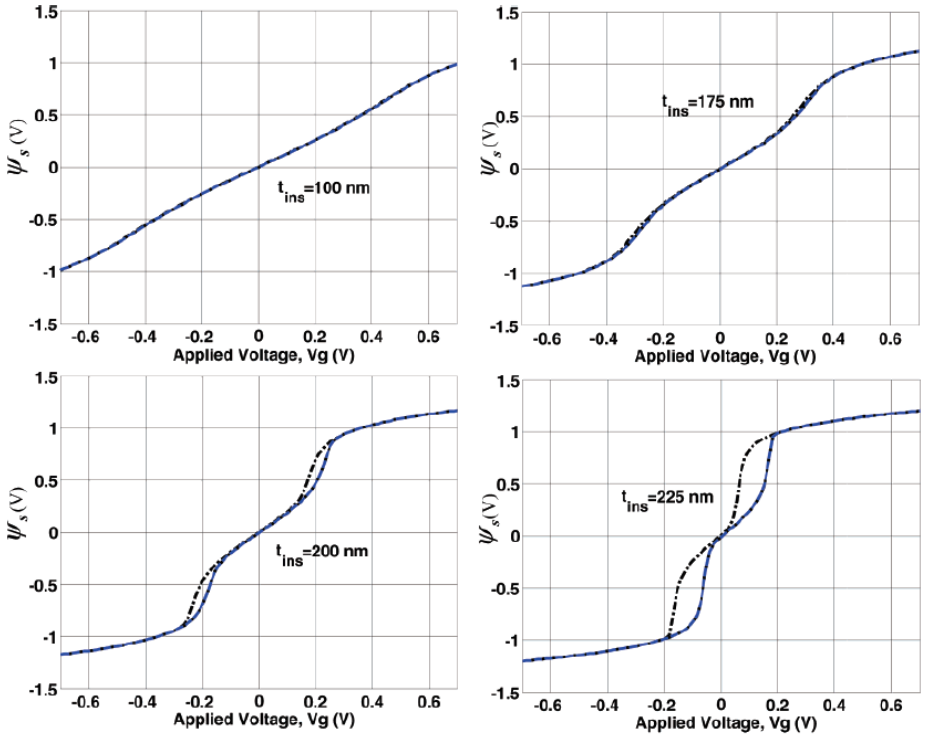
$$V \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0 \frac{dQ}{dt}$$

Very different from dielectric capacitor!

What if we use a Ferroelectric Insulator?

Calculation for $BaTiO_3$:

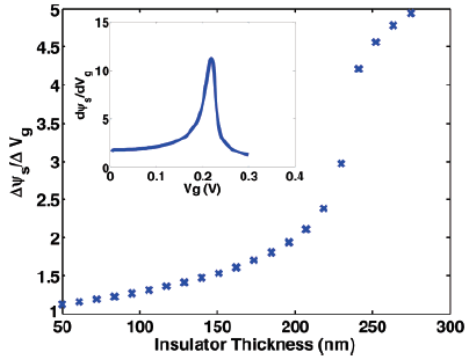




Definition of polarization:

$P=\varepsilon_0\chi_\varepsilon E=\varepsilon_0(\varepsilon_r-1)E$

Dielectric material - linear
Ferroelectric material - loop



Can HfO2 be Ferroelectric?

Ferroelectricity in undoped hafnium oxide

Patrick Polakowski and Johannes Müller
Fraunhofer Institute for Photonic Microsystems IPMS - Business Unit Center Nanoelectronic Technologies CNT, Dresden 01099, Germany

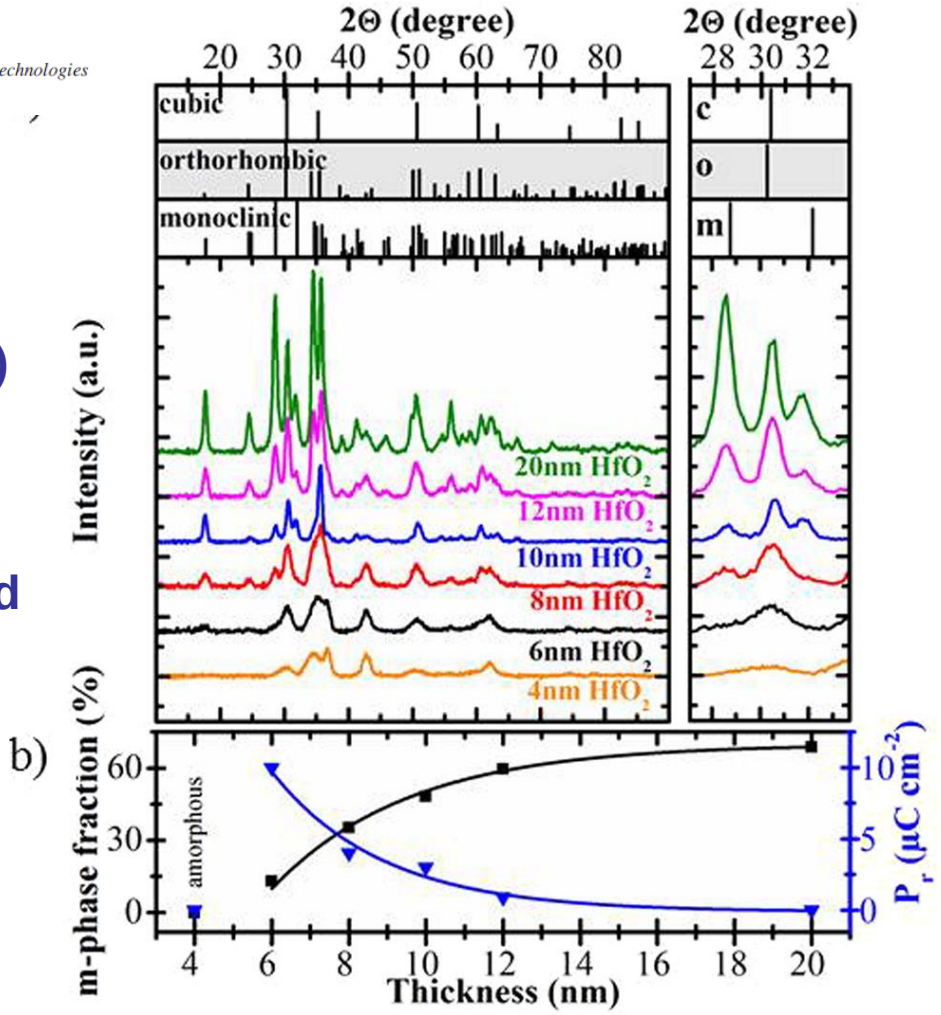
HfO_2 has several crystal structures

The phases depend on processing (ALD 300 C + spike anneal at 650 C)

O-phase are ferroelectric

For thin films about 60% is obtained

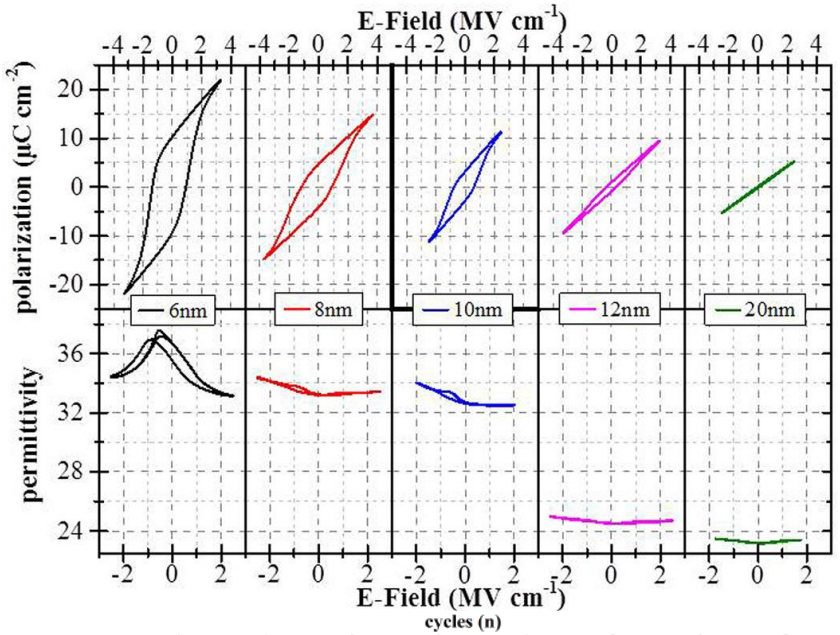
Other mechanisms:
- Doped HfO_2 (Si, Al, …)
- $Hf_{0.5}Zr_{0.5}O_2$

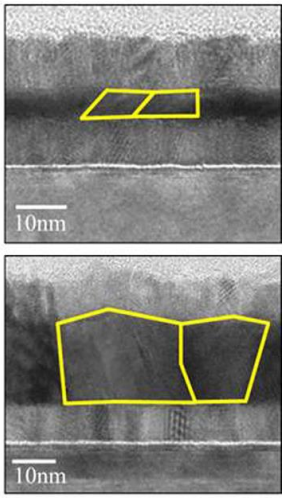


Can HfO2 be Ferroelectric?

Small grain sizes are required

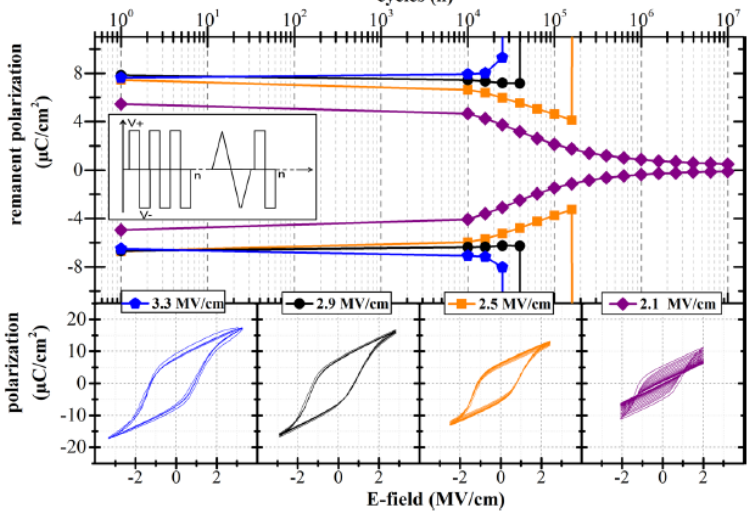
Note the high permittivity





The films have a life time issue with degradation

Might be solved!



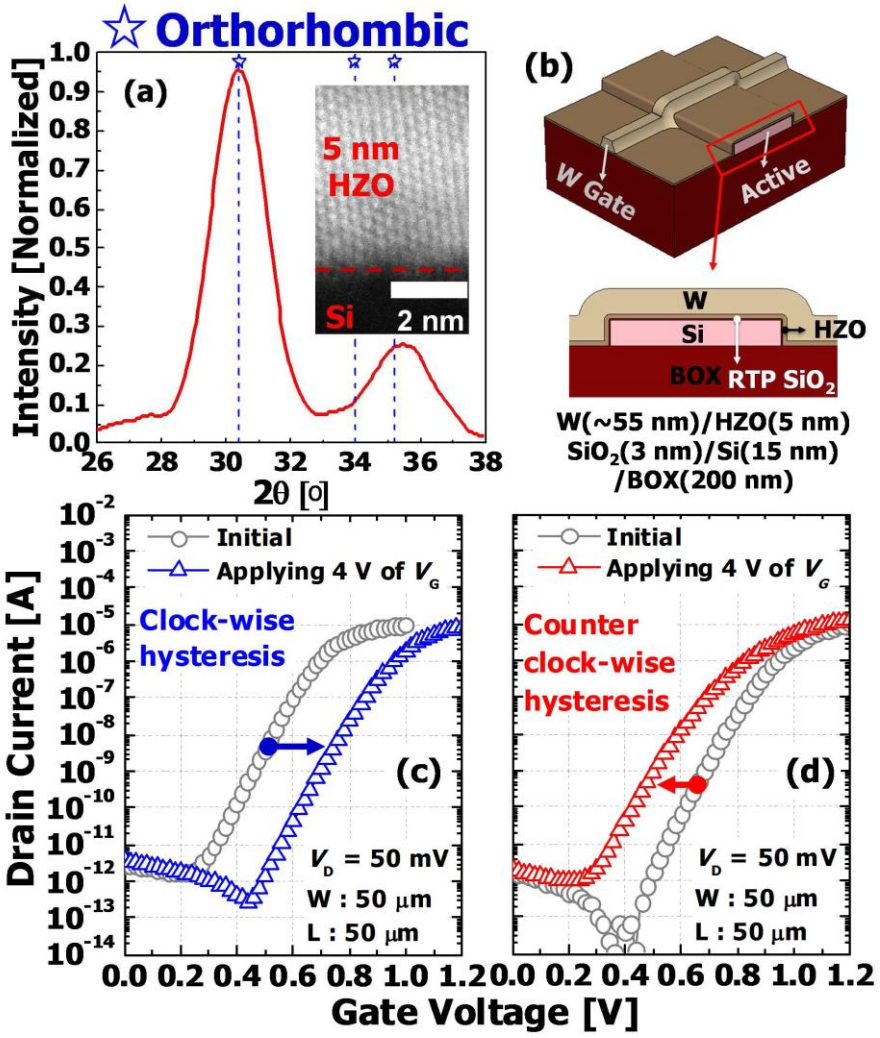
Effects on Transistors

Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors

Daewoong Kwon, Korok Chatterjee, Ava J. Tan, Ajay K. Yadav, Hong Zhou, Angada B. Sachid, Roberto dos Reis, Chenming Hu, and Sayeef Salahuddin

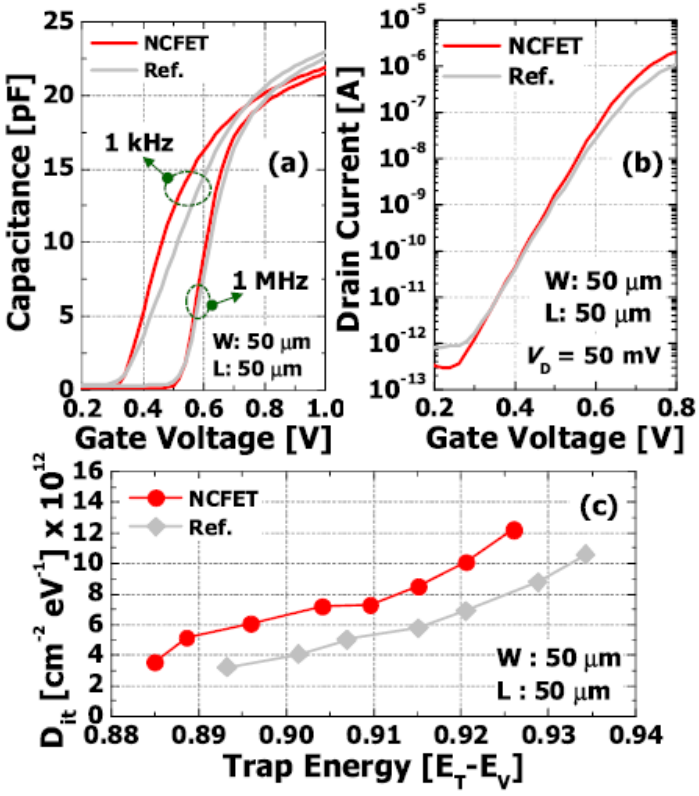
HZO used in Si SOI FETs

Hysteresis different for reference (left) and NCFET (right) verifying ferroelectric behaviuour



Effects on Transistors

The reference has lower D_{it} but the NC-FET has better characteristics!



Effects on Transistors

The NC-FET has better:
On-characteristics (higher ε_r)
Off-state characteristics (ferroelectric behaviuour)

Here not below 60mV/dec
Others have demonstrated