



Carbon Nanotube Electronics

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Outline

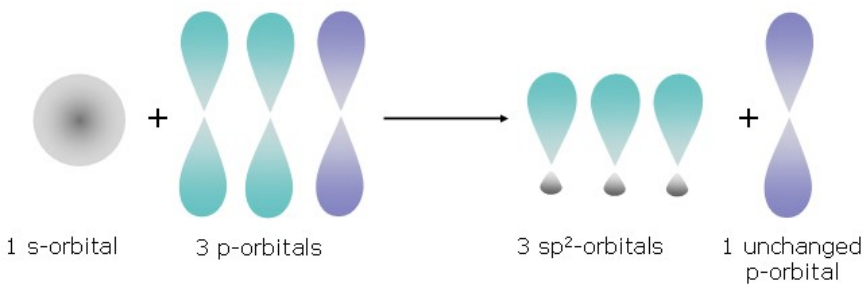
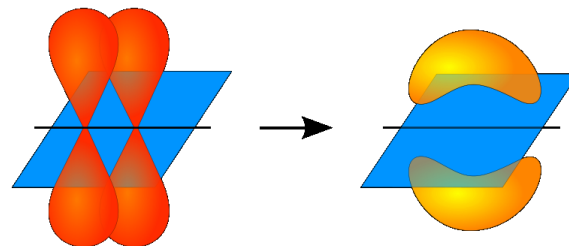
- Basics of graphene and CNTs
 - Structural
 - Electronic
 - Production of CNTs
- Advantages of CNTs for FETs
 - Electrostatics -> length scaling
 - High-k compatibility
 - Band-to-band tunneling
- Challenges of CNT integration
 - Contacts
 - Doping
 - Positioning
 - Chirality control
- Towards integration
 - Flexible electronics
 - High frequency performance

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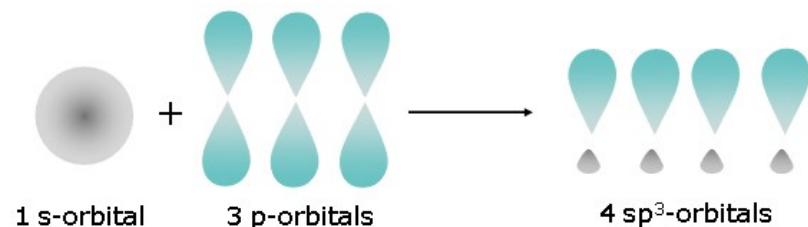
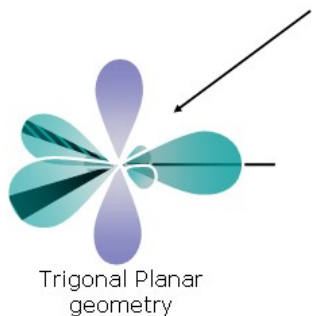
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Hybridisation of carbon orbitals

- 4 valence electrons
- 1 s-electron can "mix" with 1-3 p-electrons
- sp^2 have three σ -bonds in a plane + π -bond
- sp^3 have four σ -bonds



sp^2

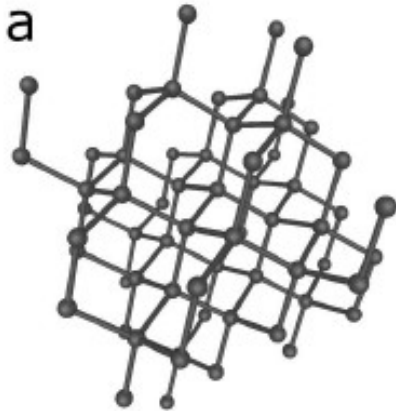


sp^3

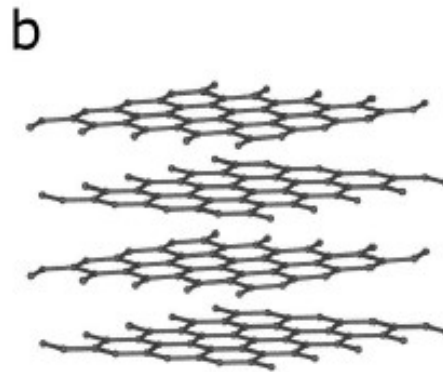


Carbon allotropes

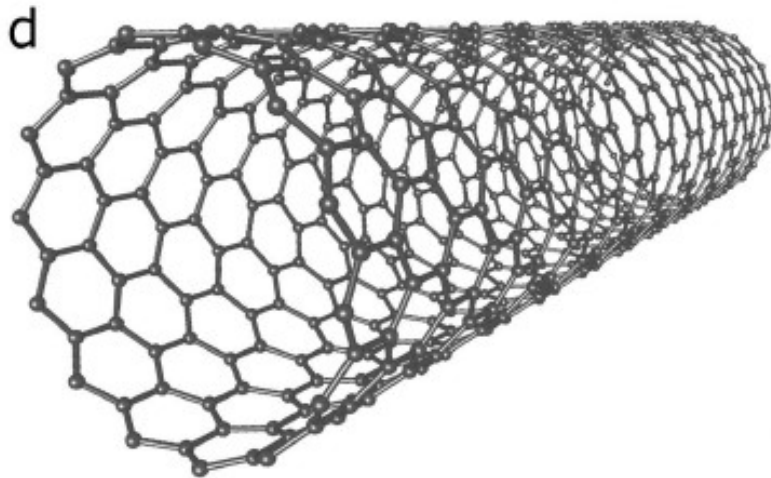
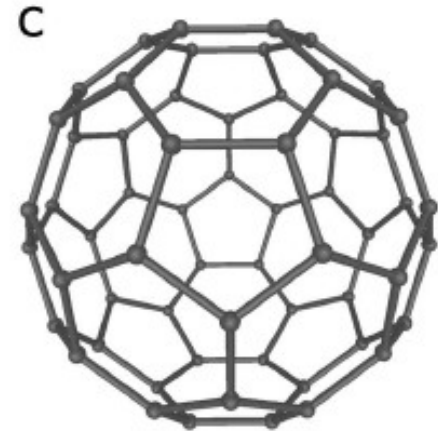
diamond



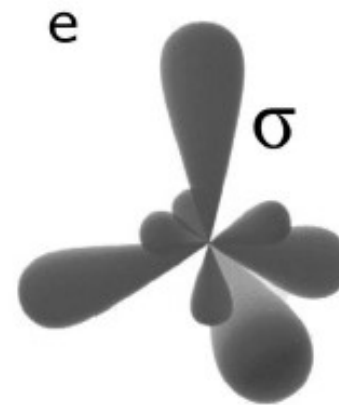
graphite



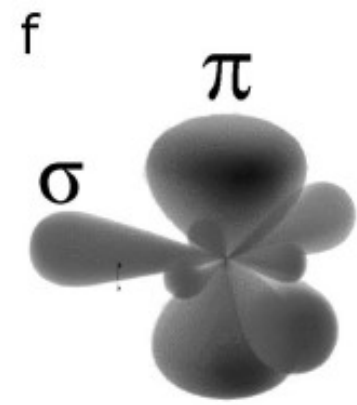
C₆₀ (fullerene)



Carbon nanotube

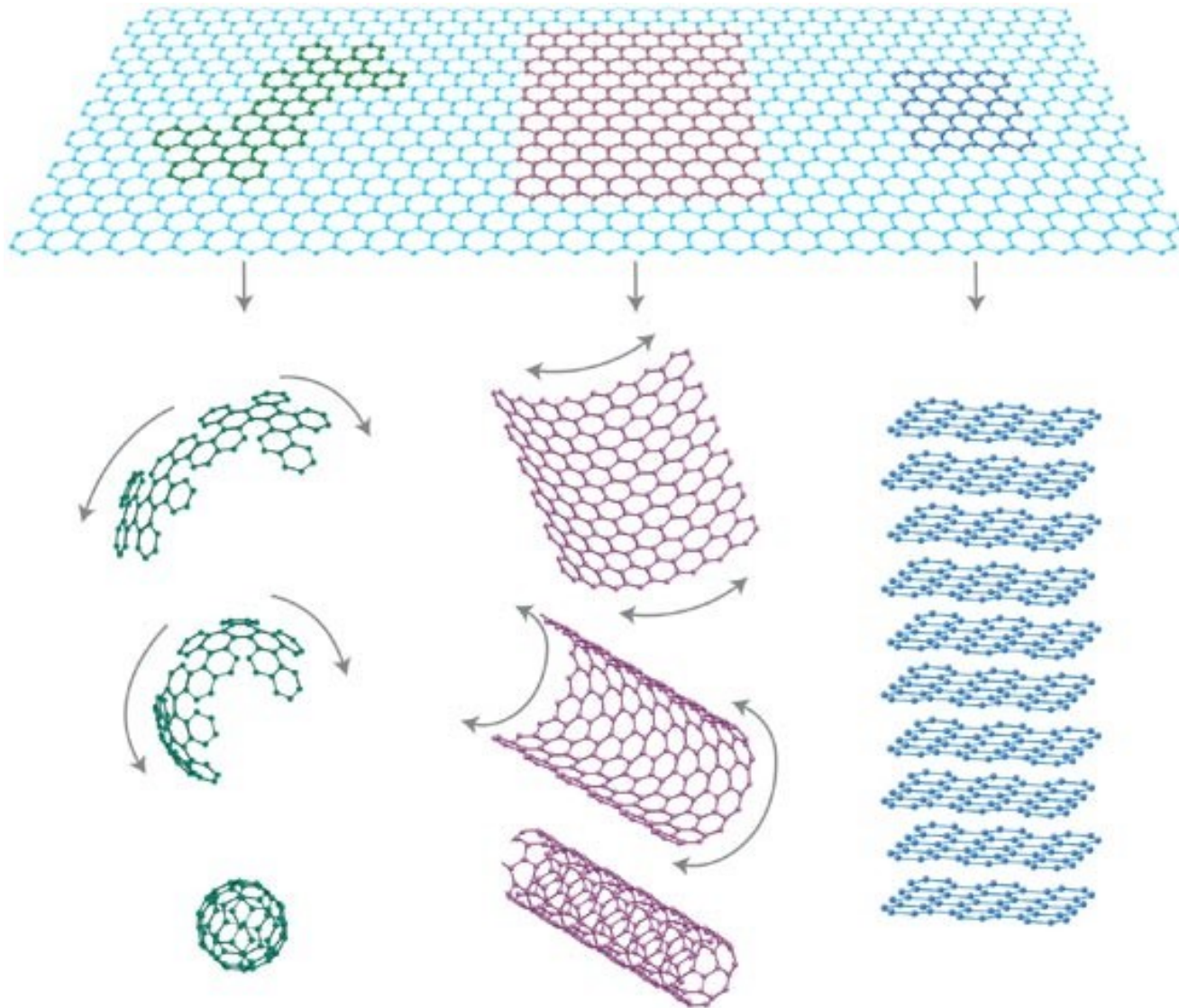


sp³



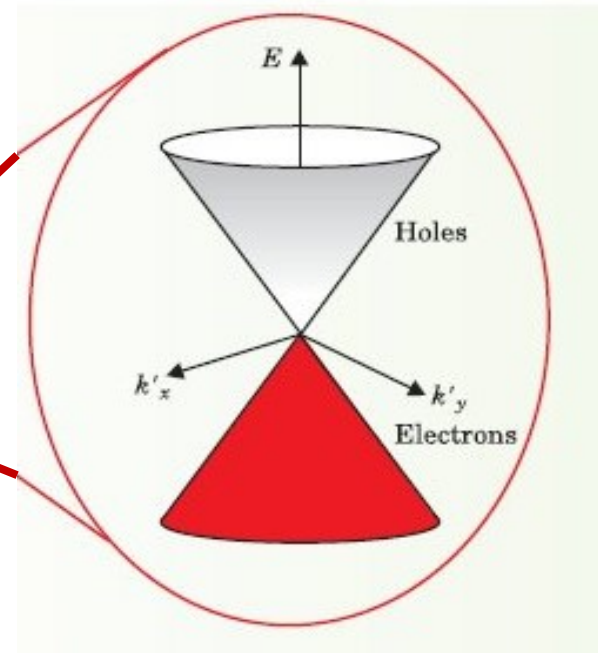
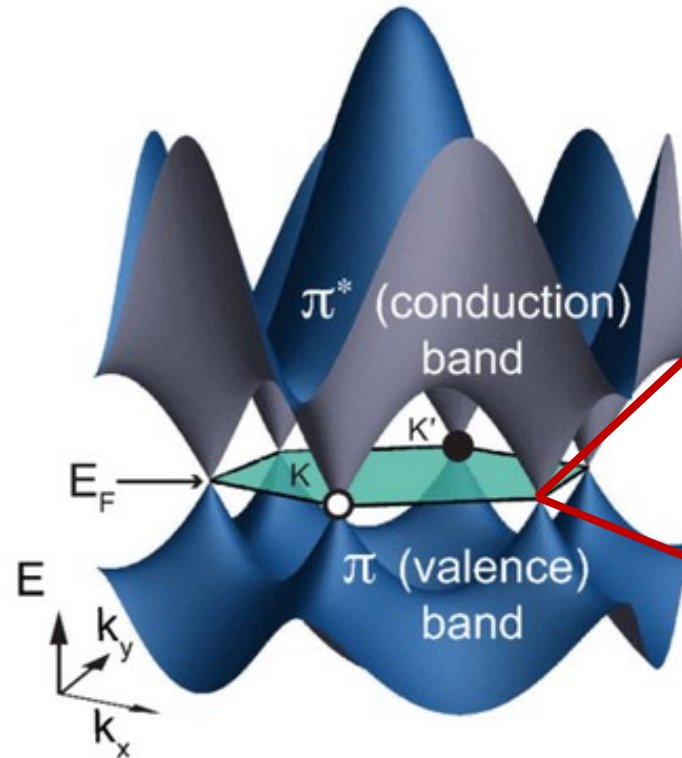
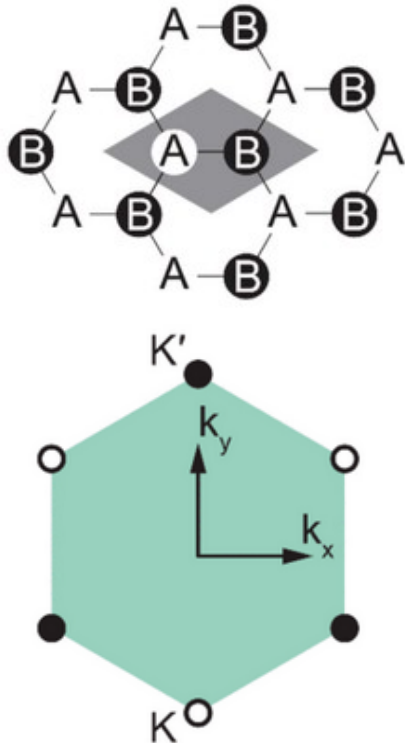
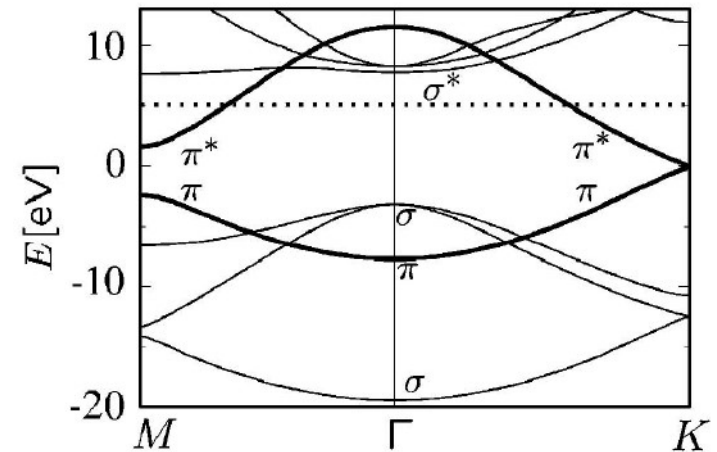
sp²

Graphene is mother of all sp^2 -carbon



Graphene band structure

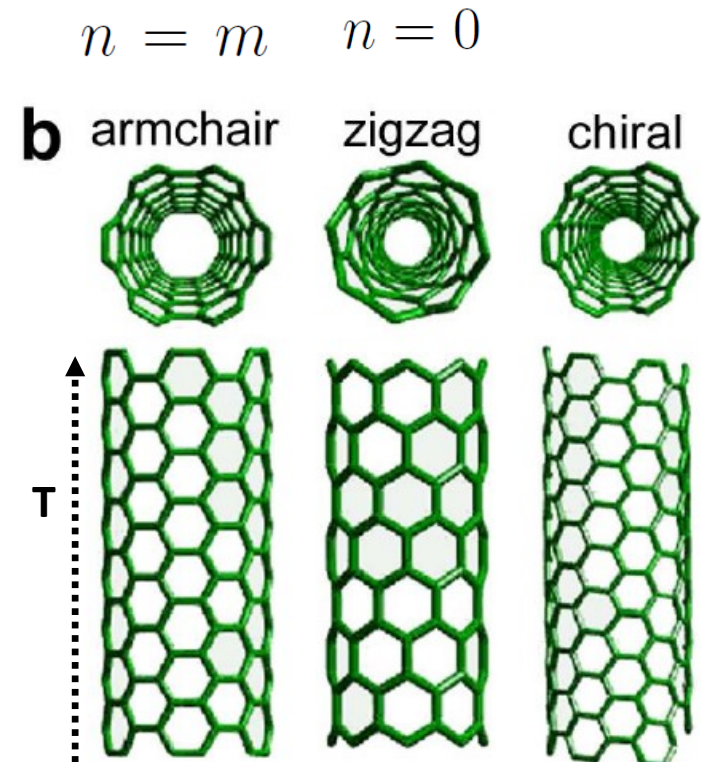
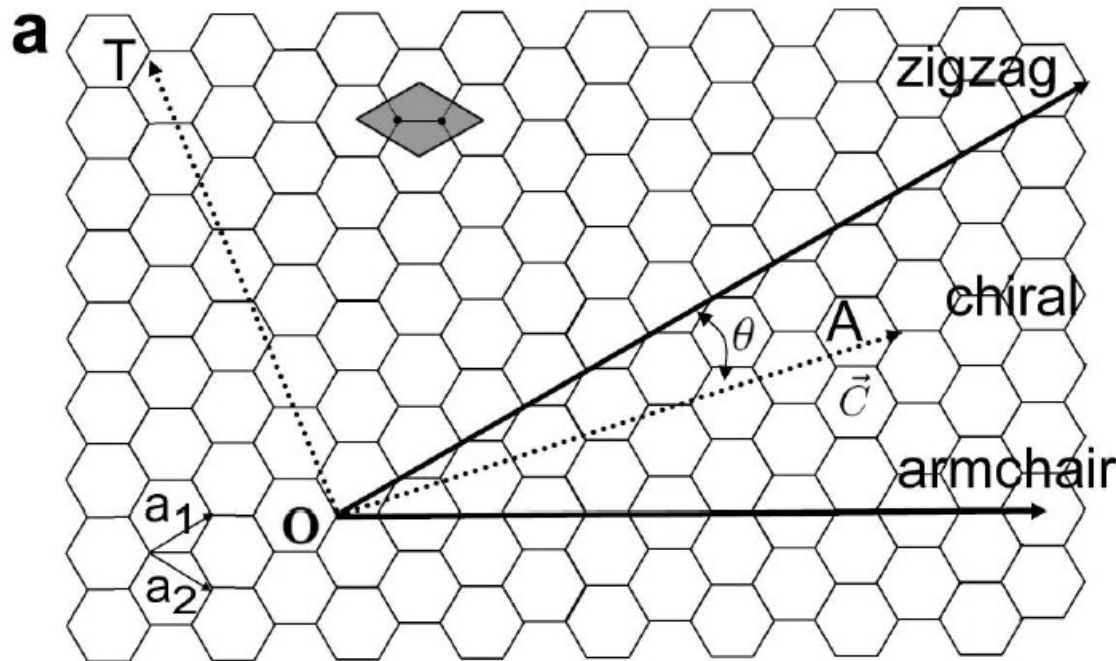
- Semimetal: no band gap and zero DOS at E_f
- Only π -bands are relevant for transport
- Conduction and valence bands meet at the K/K'-points
- Linear dispersion near E_f



Rolling graphene into CNT

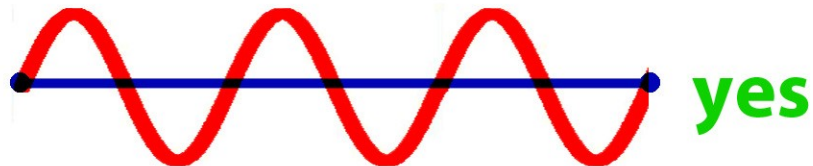
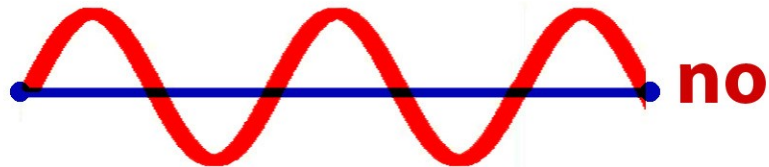
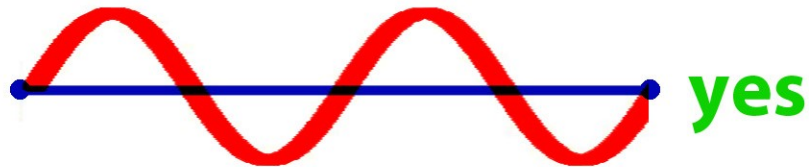
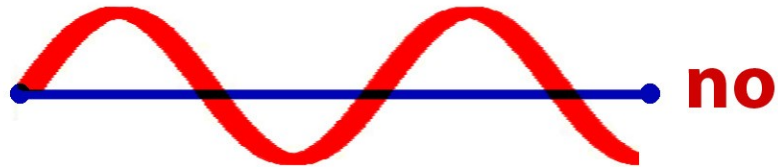
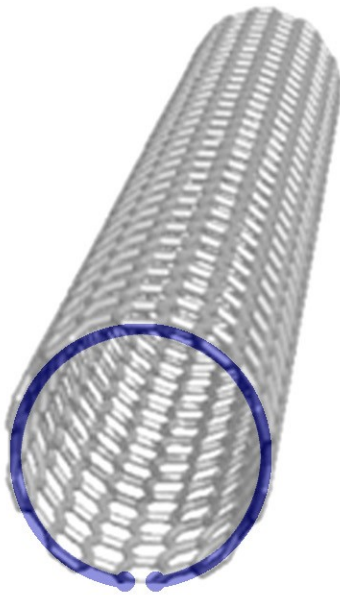
- Cut graphene into narrow strip and roll into tube
- Different structure depending on direction of cut
- Armchair, zigzag, chiral CNTs
- Chirality defined by index (n,m)

$$\vec{C} = n\vec{a}_1 + m\vec{a}_2$$



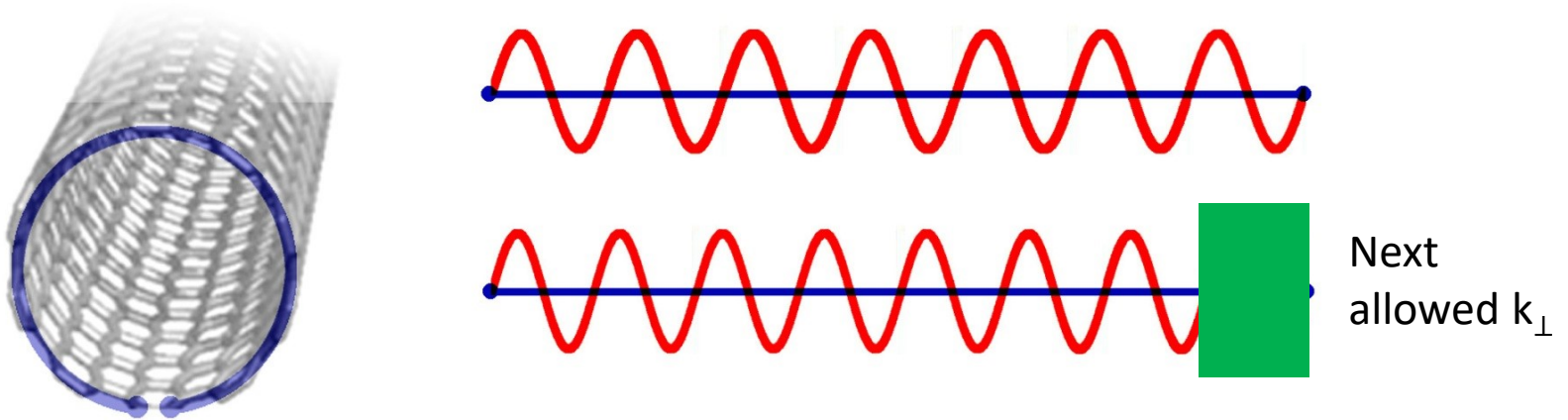
Confinement of electron wavefunctions

- Have to have continuous wavefunction around circumference
- Periodic boundary conditions
- Only some wavevectors $k_{\perp} = 2n\pi/C$ with $n=1,2,3\dots$ allowed

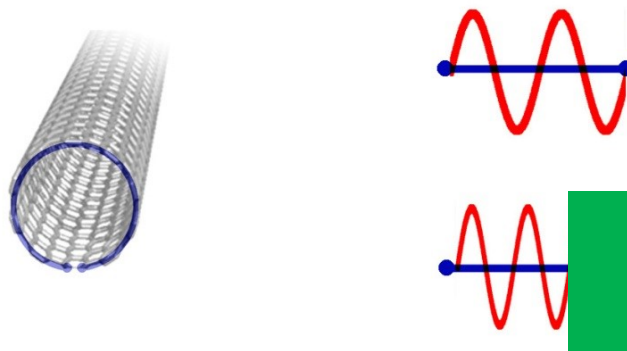


Diameter dependence of confinement

large diameter = small energy difference

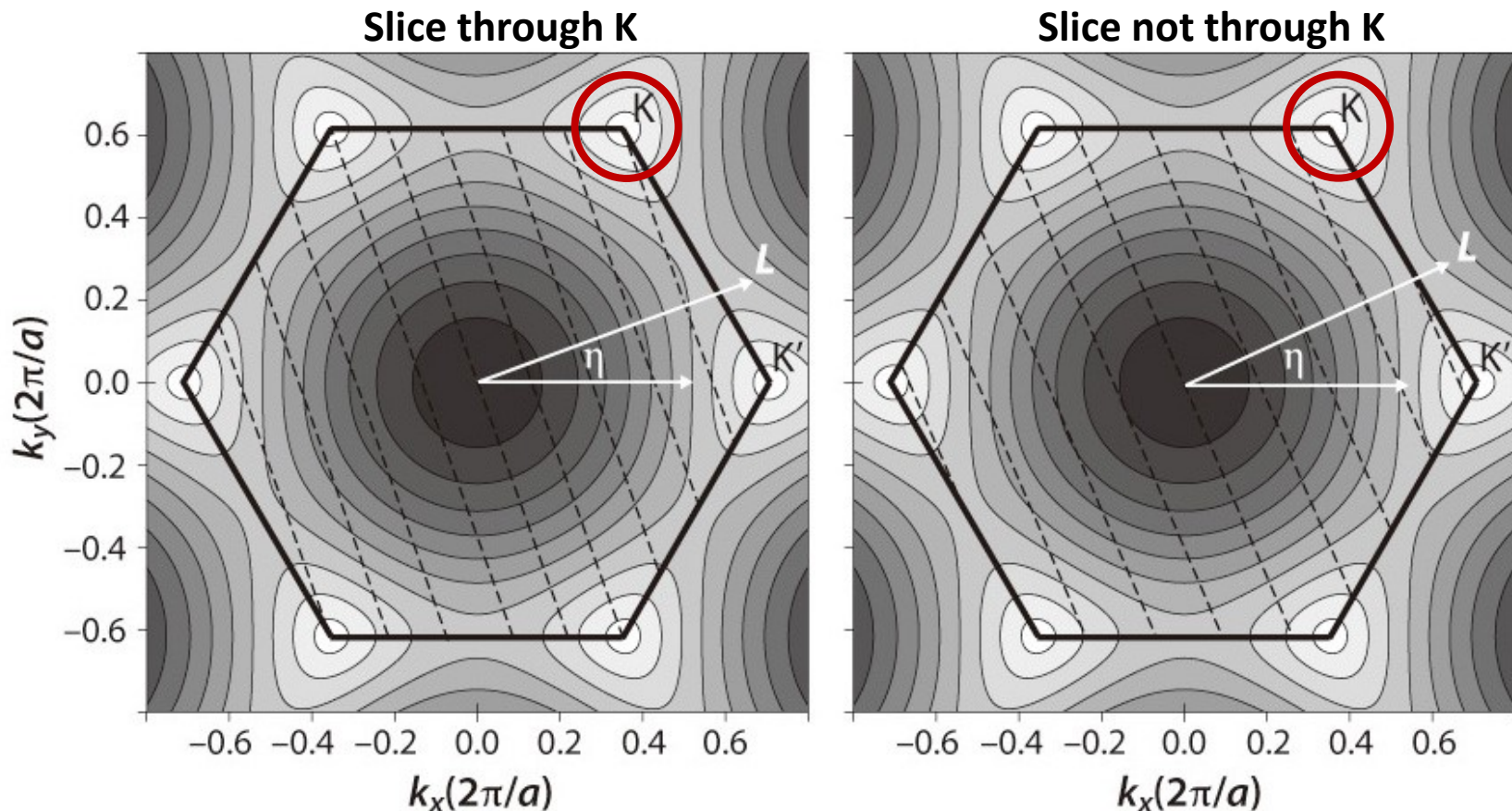


small diameter = large energy difference



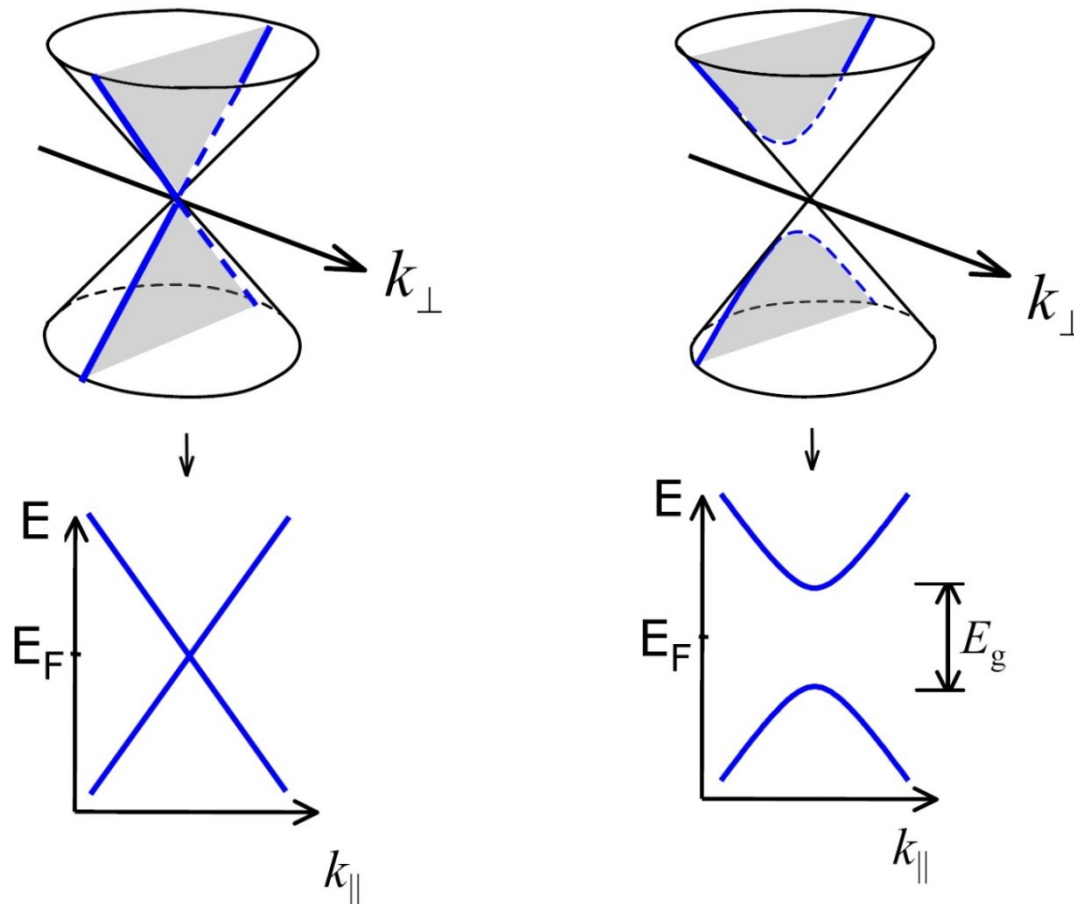
Confinement of electron wavefunctions

- Slices in graphene dispersion relation of allowed wavevectors around circumference
- Position of slices depends on chirality
- Small diameter CNT have larger distance between slices



Allowed wavevectors

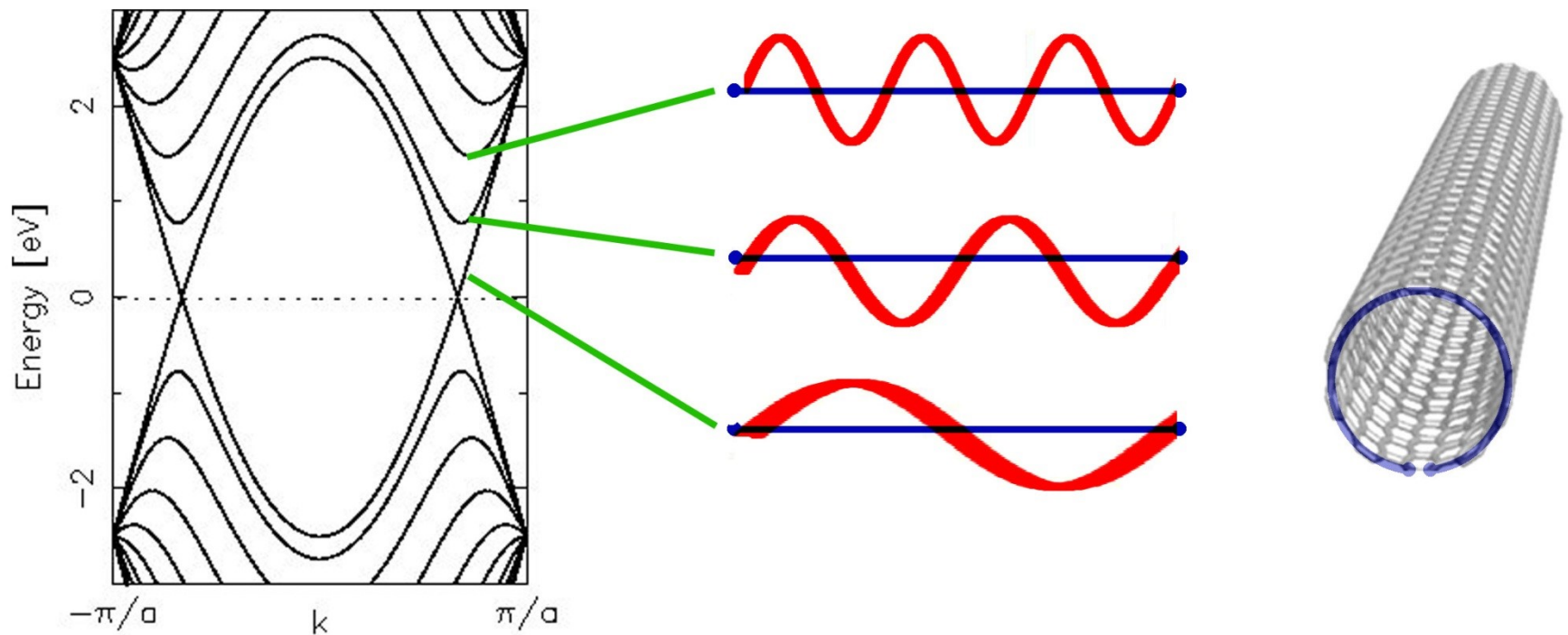
- $n-m = 3i$ with $i=1,2,3\dots$ -> slice goes through K-point -> metallic CNT
- $n-m \neq 3i$ -> slice does not go through K-point -> semiconducting CNT with parabolic bands



$$E(k) = \pm ((\hbar v_F k)^2 + (E_g/2)^2)^{1/2}$$

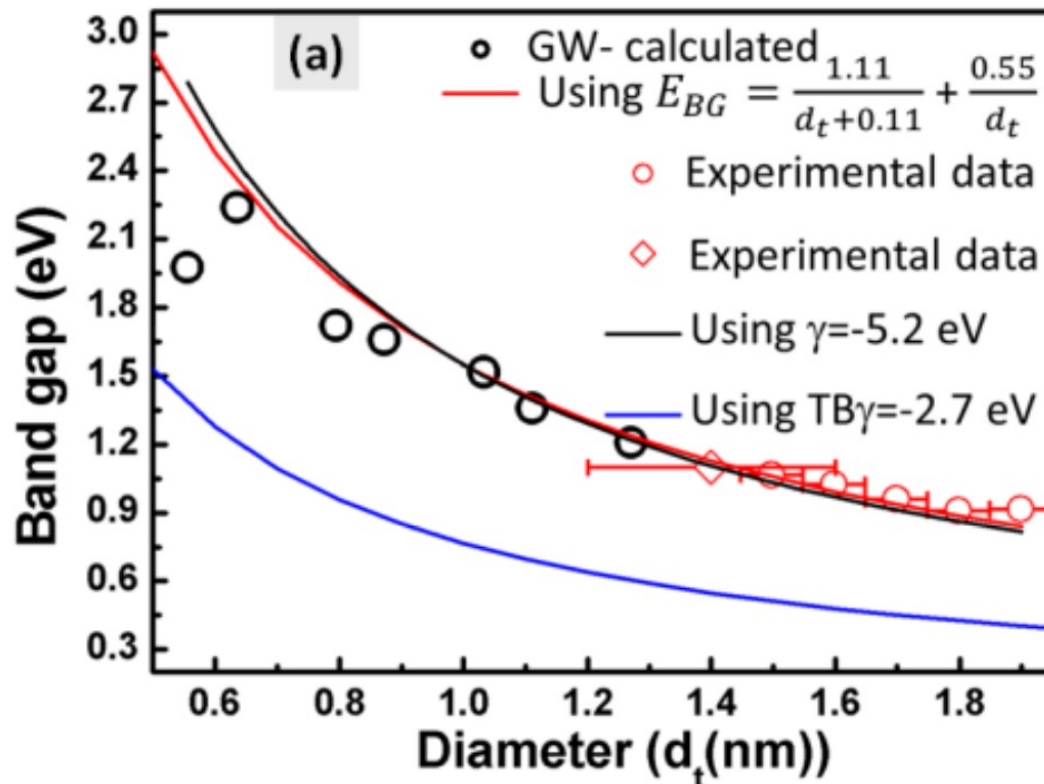
Subbands

- π -bands split into 1D subbands of increasing energy
- Mainly important at high gate voltages or for optical transitions
- Wavefunctions just schematic, need TB calculation



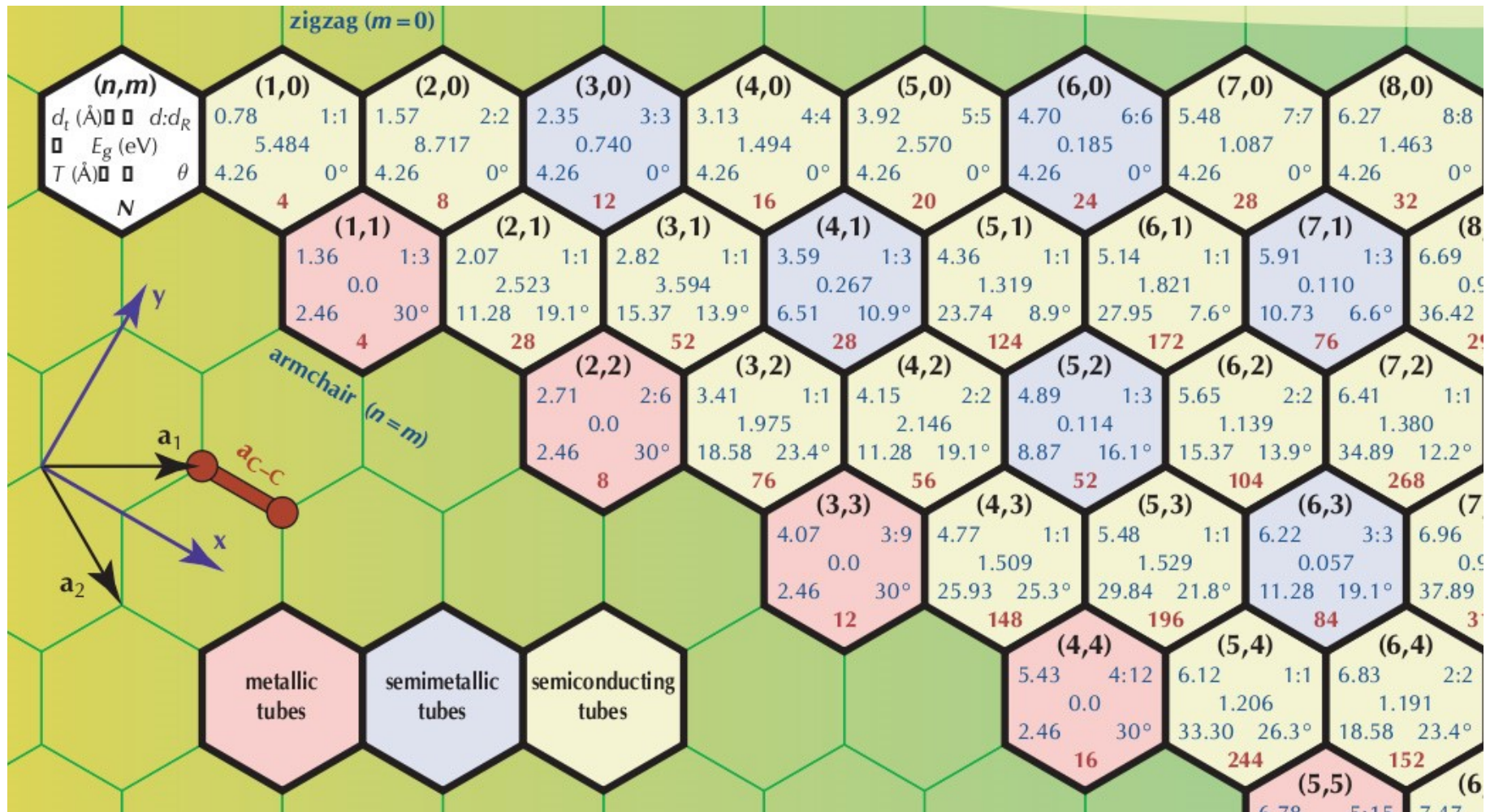
Band gap vs diameter

- Linear dispersion of graphene gives E_g inversely proportional to diameter for CNTs
- Curvature induced gap of 10's of meV in most of the "metallic" CNTs
- Only armchair CNTs truly metallic



All CNTs are different

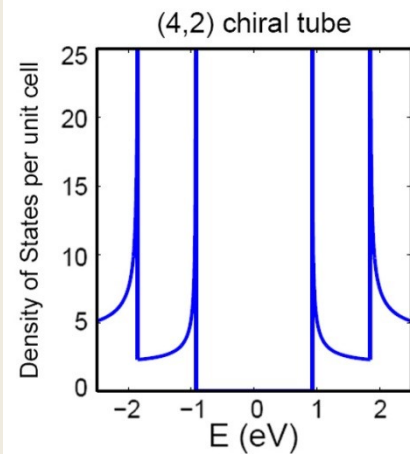
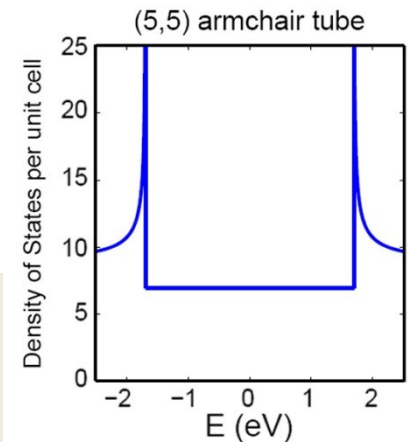
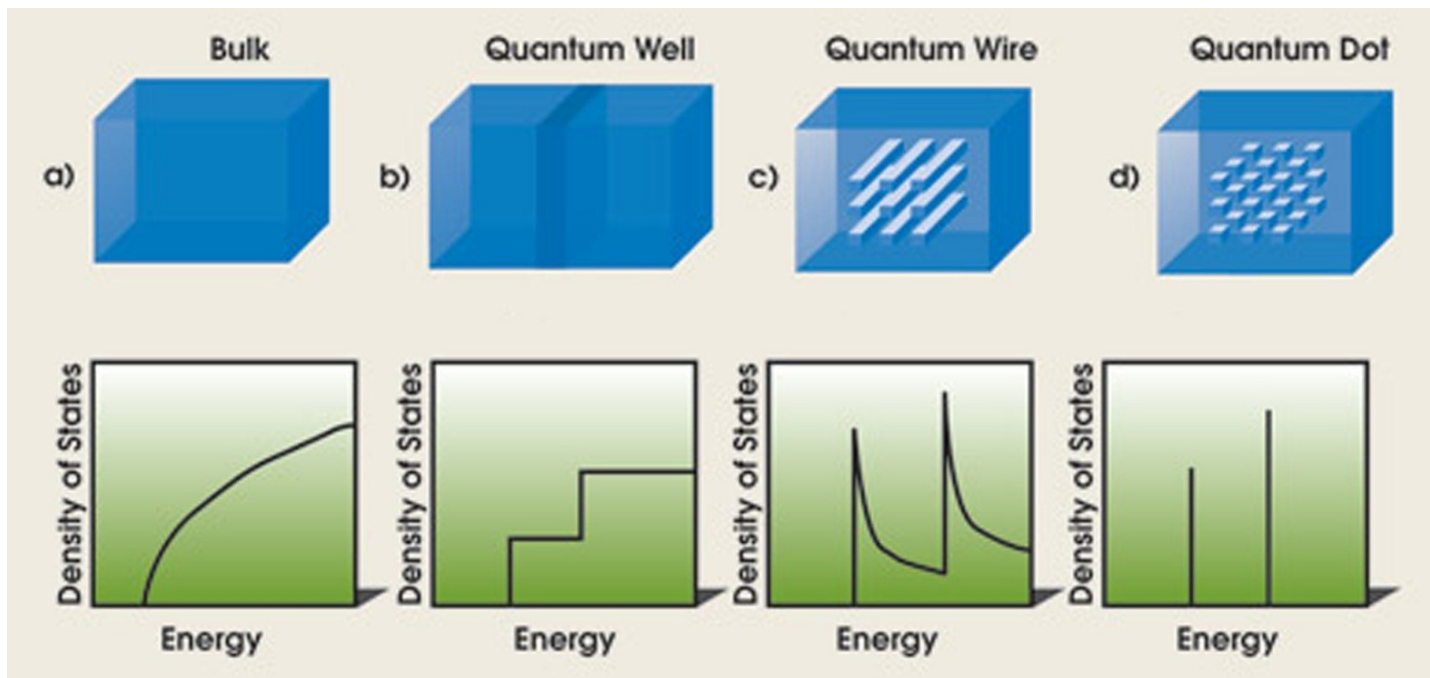
- 1/3 metallic or small gap
- 2/3 semiconducting with different gap



Density of states

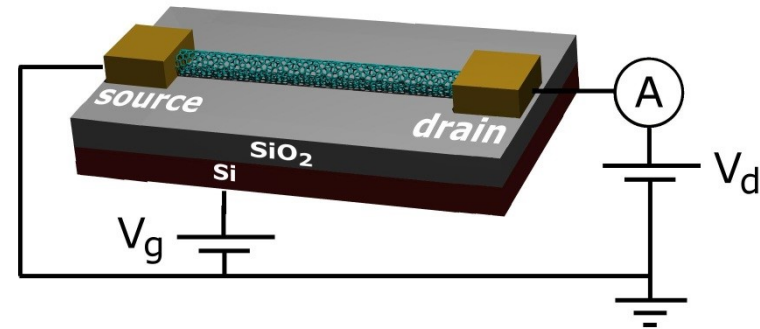
- Van Hove singularities with high DOS at band edges
- Can be seen in scanning tunneling microscope or capacitance measurements
- Strong influence on optical properties

$$g_i(E) = \frac{4}{\pi \hbar v_F} \left[1 - (E_g^i / 2E)^2 \right]^{-1/2}$$

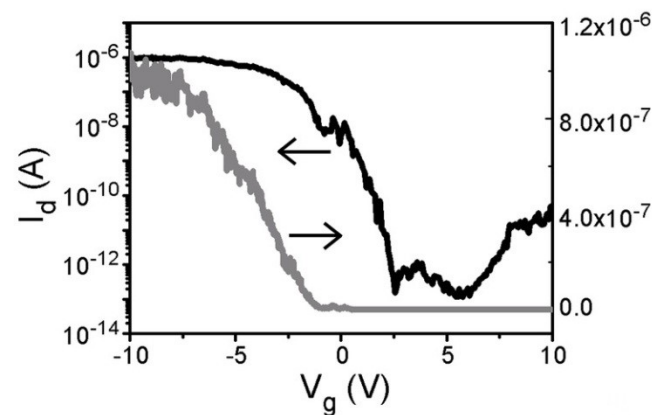


Electrical characteristics

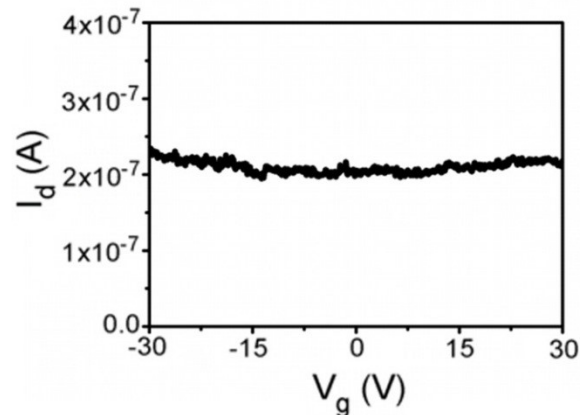
- Three types
 1. Semiconducting: strong gating effect
 2. Metallic: no gating effect
 3. Small gap semiconducting: some gating effect
- Can withstand 10^9 A/cm^2



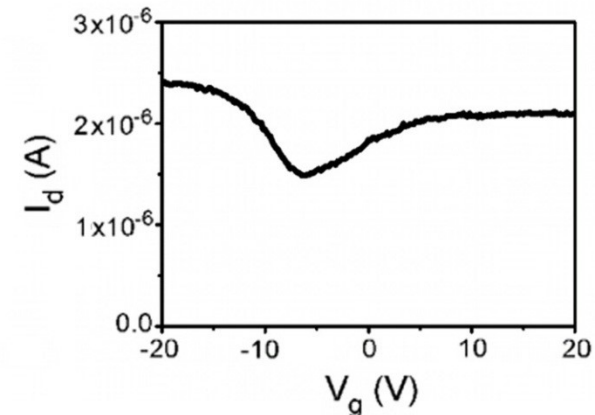
semiconducting



metallic

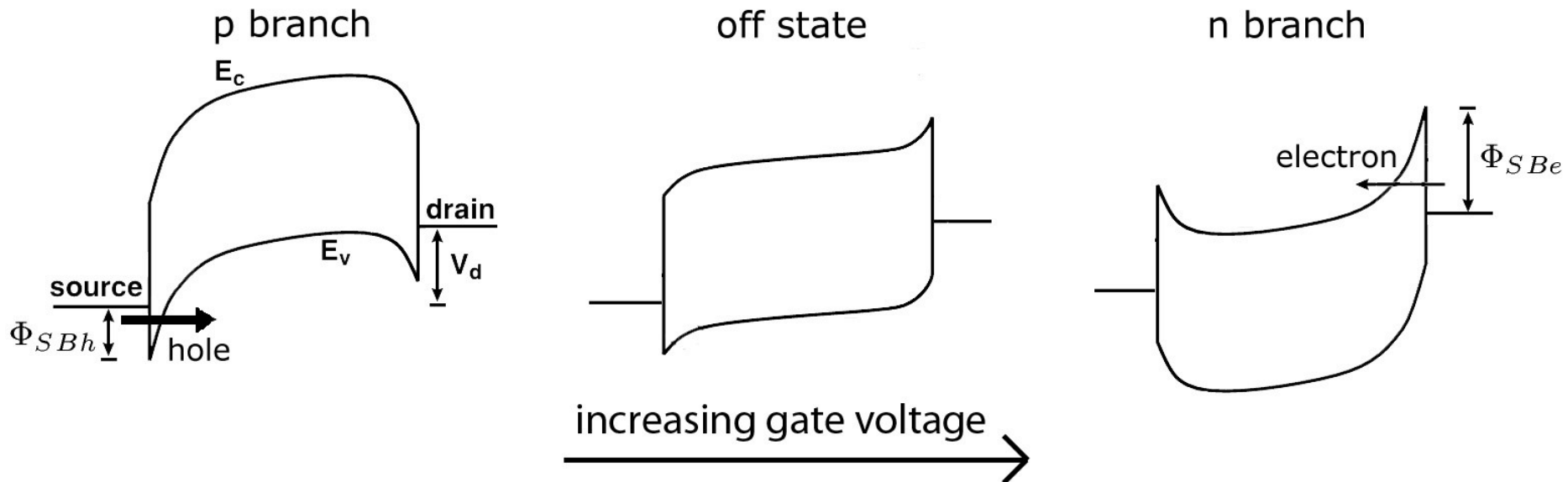


small band gap



Transport through Schottky barriers

- First CNTFETs had Schottky barriers at metal contacts
- Tunneling through SB determines transport
- Negative gate voltages -> hole transport
- Positive gate voltages -> electron transport
- Similar SB heights -> ambipolar characteristics

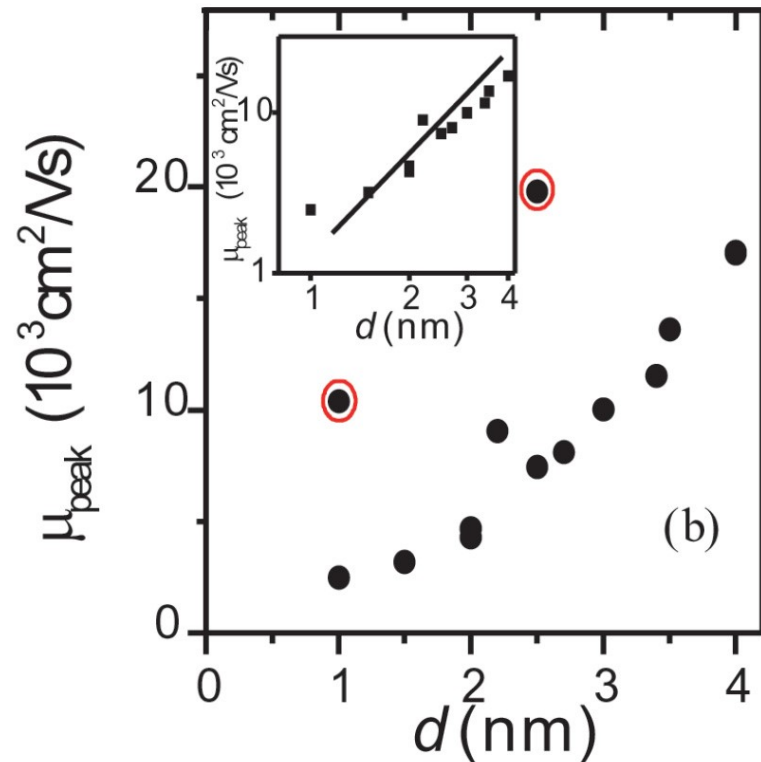
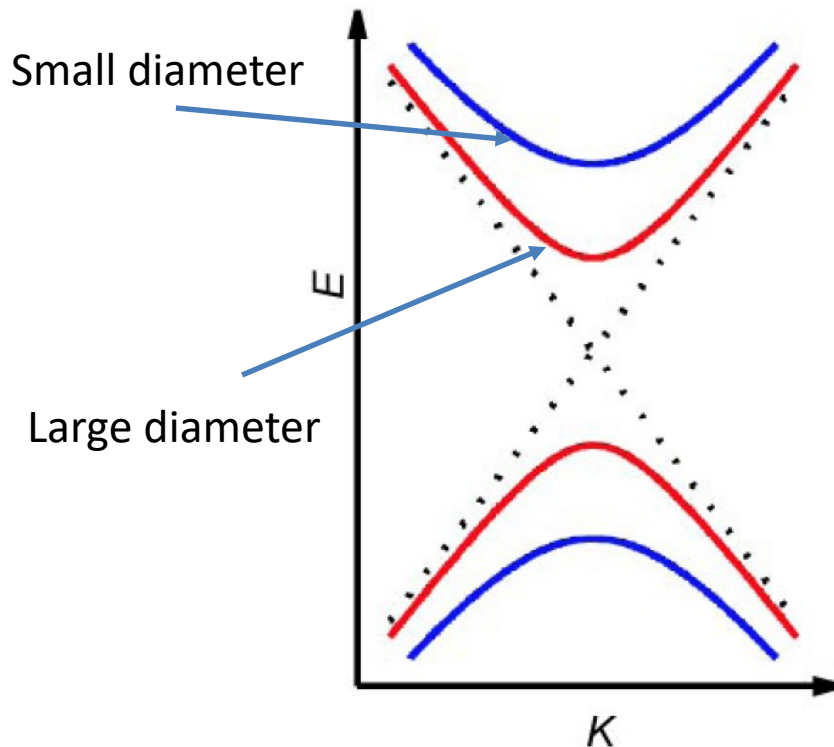


Mobility vs diameter

- Lower curvature of bands for smaller diameter -> mobility proportional to d^2
- $\mu > 100\,000\text{ cm}^2/\text{Vs}$ at 50 K

$$m^* = \hbar^2 \cdot \left[\frac{d^2 \epsilon}{dk^2} \right]^{-1}$$

$$\mu_{FE} = \frac{L^2}{C_g} \frac{\partial G}{\partial V_g}$$



Scattering

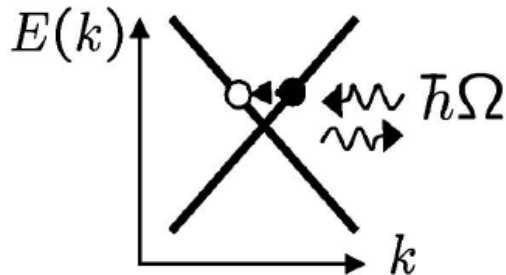
- Elastic scattering has to reverse direction of electron



- Acoustic phonon scattering dominates at low bias and gives mfp > 300 nm -> ballistic transport possible
- Optical phonons scattering dominates only at high bias and gives mfp = 15 nm
- Potential variations or phonons in substrate under CNT can also scatter electrons

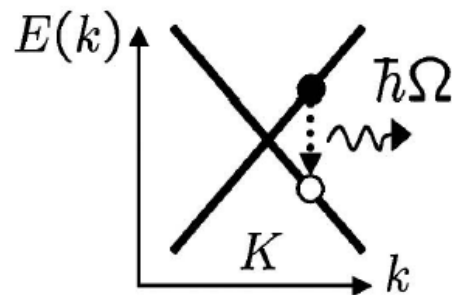
Acoustic phonon

$$q \sim 0, \hbar\Omega \ll k_B T$$



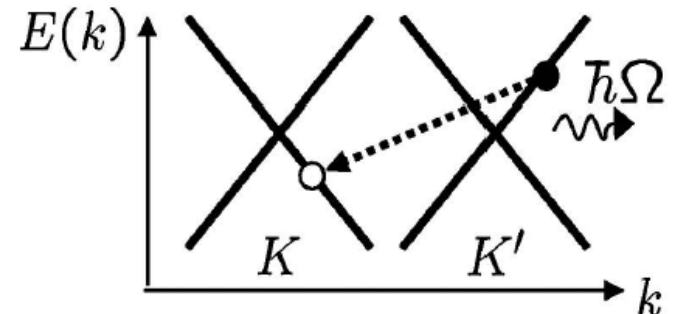
Optical phonon

$$q \sim 0, \hbar\Omega > k_B T$$



Zone boundary phonon

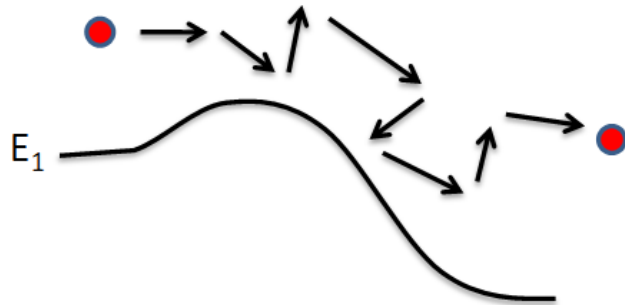
$$q > 0, \hbar\Omega > k_B T$$



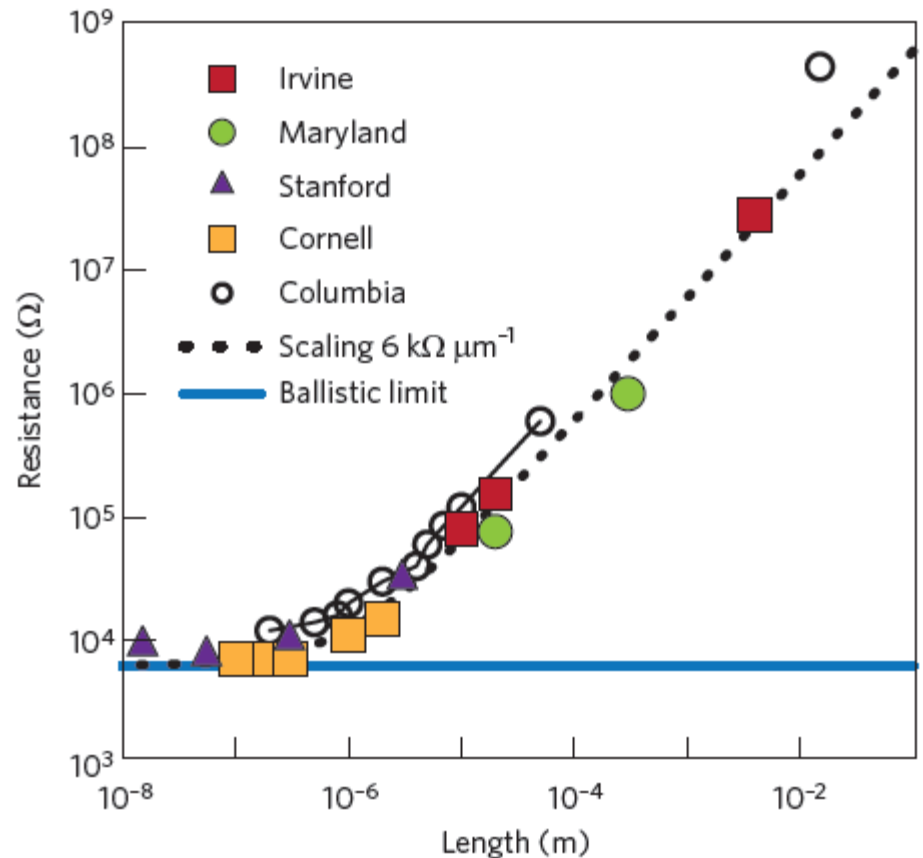
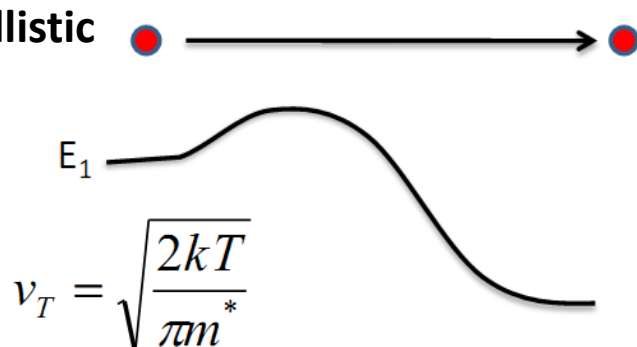
Ballistic transport

- Channel length \ll mfp \rightarrow no scattering in channel
- Mobility not relevant but injection velocity is
- $R_{\min} = h/4e^2 = 6.5 \text{ k}\Omega$ in ballistic 1D system with 4 modes

Drift-diffusion

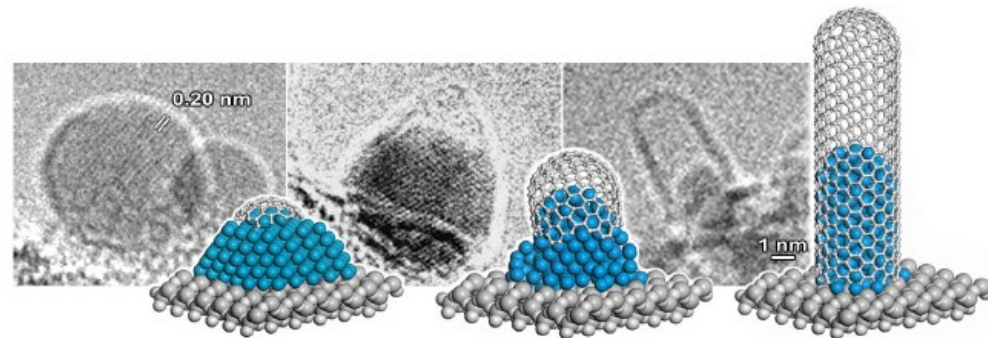
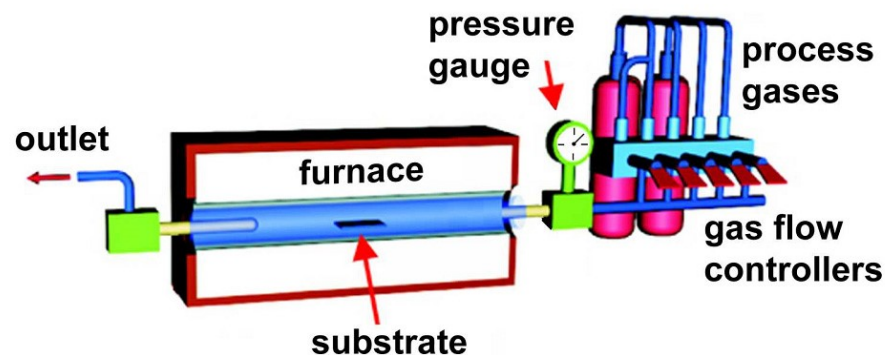
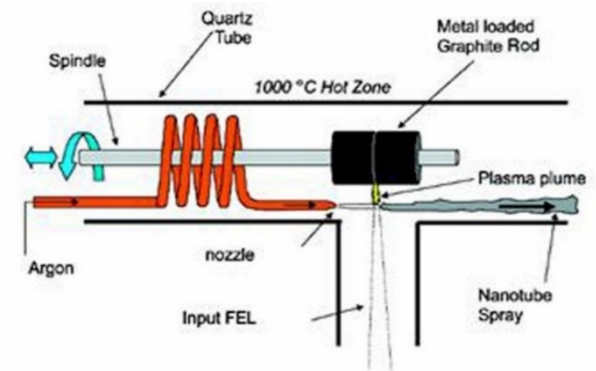
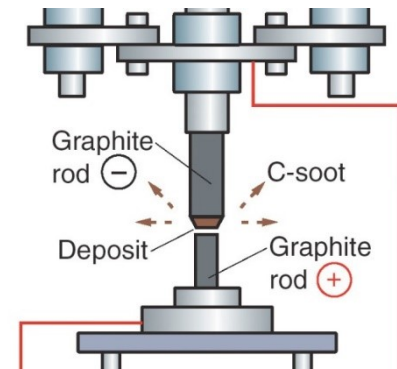


Ballistic



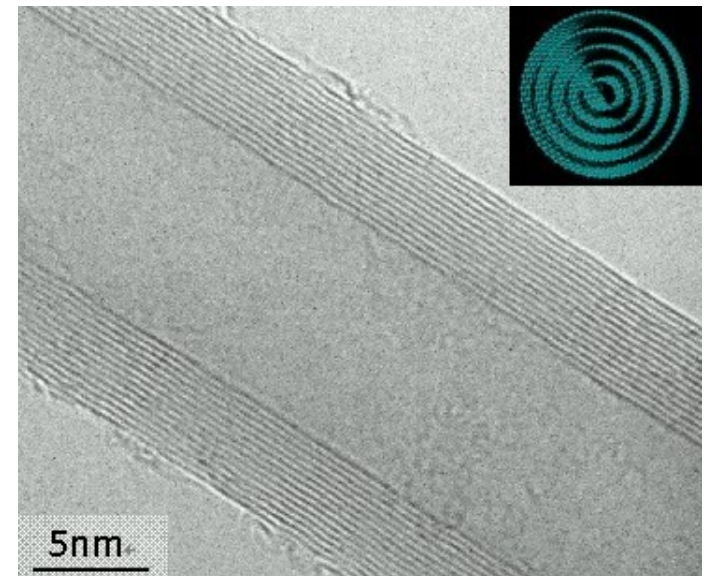
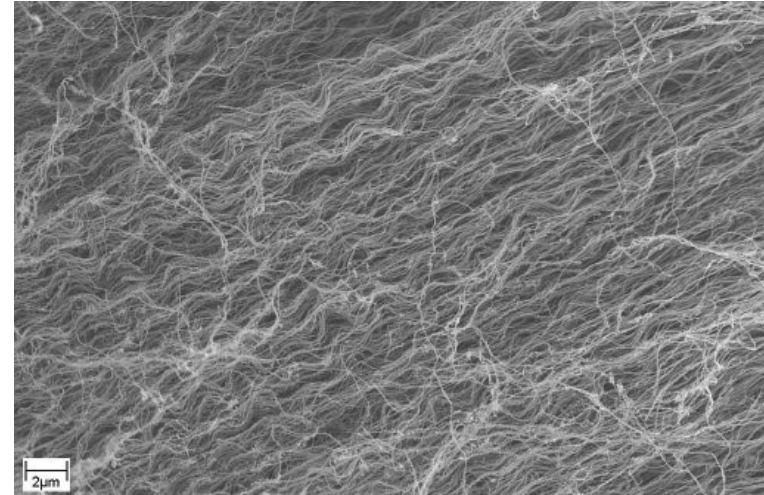
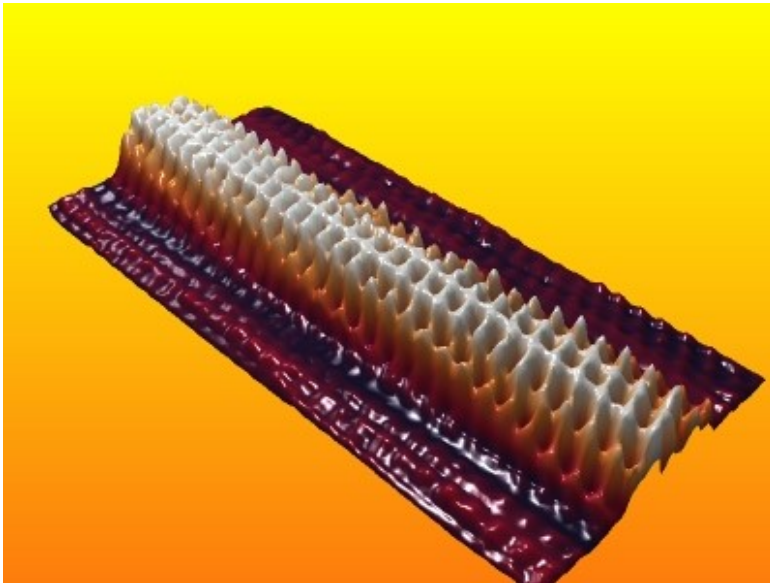
Production of CNTs

- Arc discharge: high voltage creates spark between graphite rods
- Laser ablation: laser vaporises graphite target
- Chemical vapor deposition: metal catalyst particles decompose hydrocarbon gas



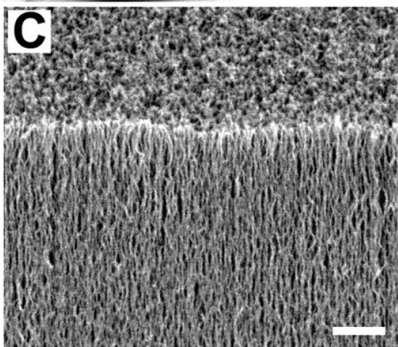
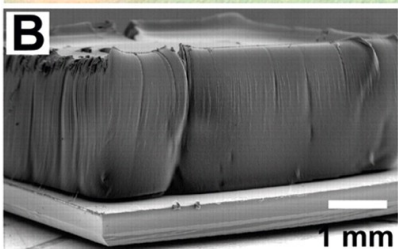
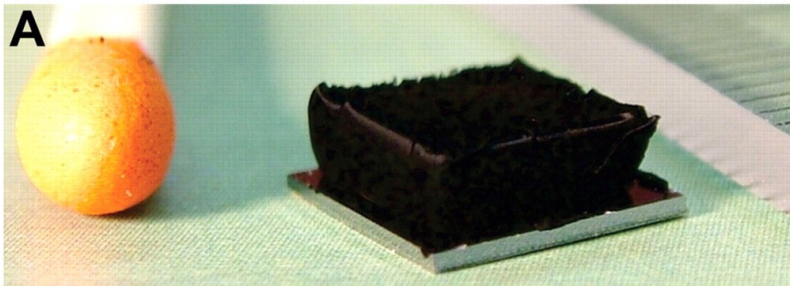
Grown CNTs

- $d=1-4\text{ nm}$, $L > 30\text{ cm}$
- Can be imaged using SEM, TEM, AFM, STM
- Deposit from suspension or grow on device substrate
- Mix of metallic, semiconducting and small band gap semiconducting



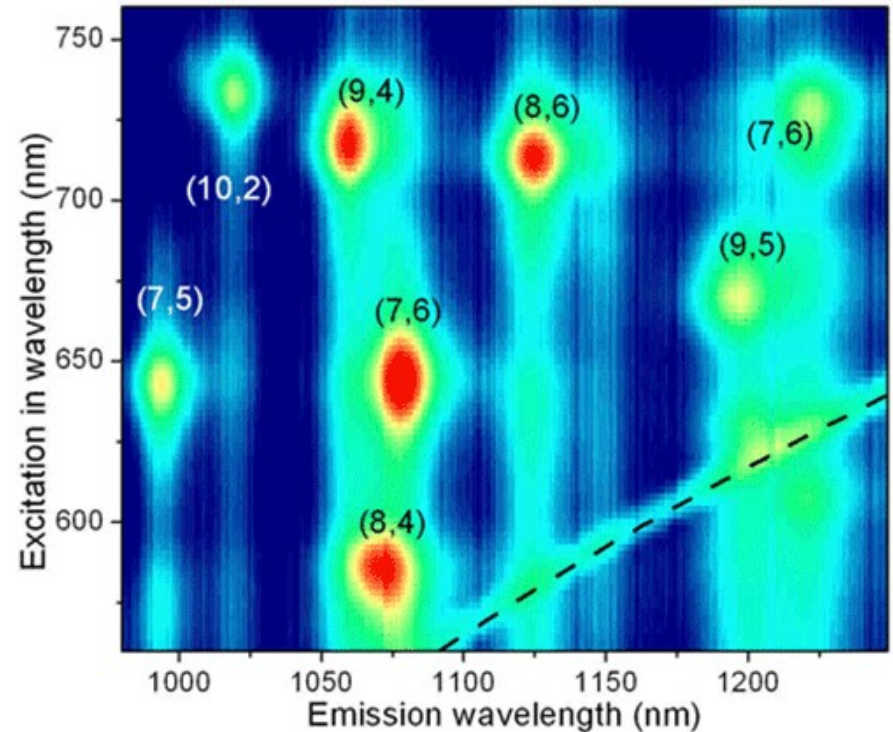
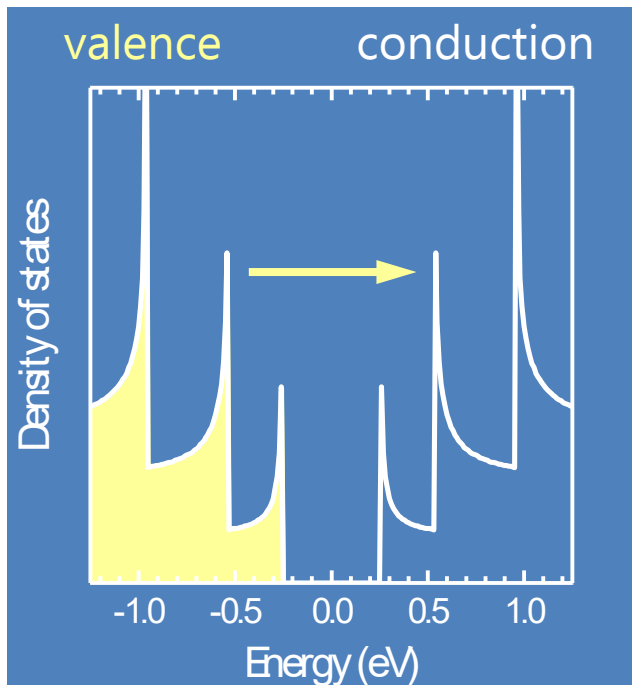
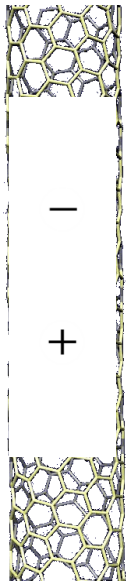
VANTA black

- **V**ertically **A**ligned **N**ano**T**ube **A**rray
- Absorbs 99.965% of visible light



Determination of type

- Photoluminescence with varying excitation λ
- Every (n,m) nanotube has specific pairs of transition energy



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Gate length scaling

- + Increased speed -> lower gate delay (CV/I), higher transconductance (g_m) and cut-off frequency (f_T)
- + Reduced power consumption - > lower energy delay product ($CV/I \cdot CV^2$)
- + Higher packing density -> less interconnect delay, cheaper
- Short channel effects (drain potential influence the channel) -> poor subthreshold slope, DIBL, high output conductance (g_d).

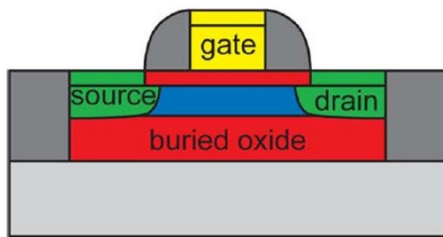
ITRS 2015 - 3 nm node: $L_g=10$ nm, $L_c=11$ nm, spacer=4 nm -> footprint =40 nm

Need to reduce gate dielectric thickness, increase dielectric constant or change geometry.

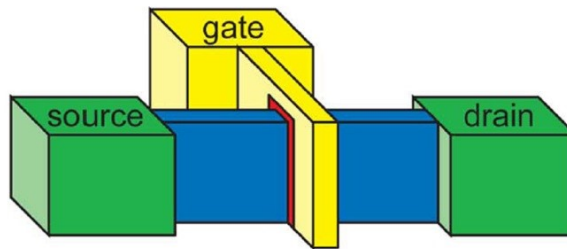
Different gate geometries

- λ = screening length, reduced by higher gate dielectric constant or thinner channel
- $L_g > 5 \lambda$ to avoid short channel effects
- More "wrapping" of the channel reduces λ -> enables L_g scaling
- CNTs and graphene allows for very good gate length scaling

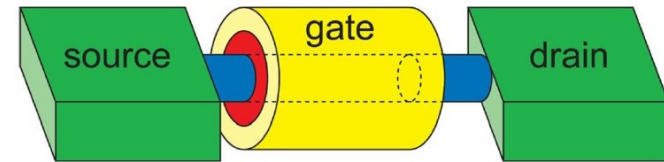
planar



trigate



gate-all-around



$$\lambda_1 \approx \sqrt{\frac{\epsilon_{ch}}{\epsilon_{ox}}} t_{ox} t_{ch}$$

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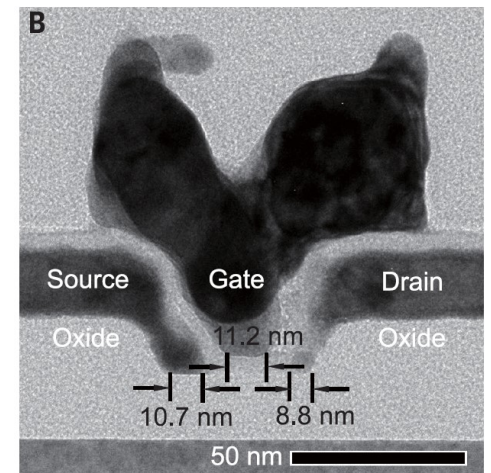
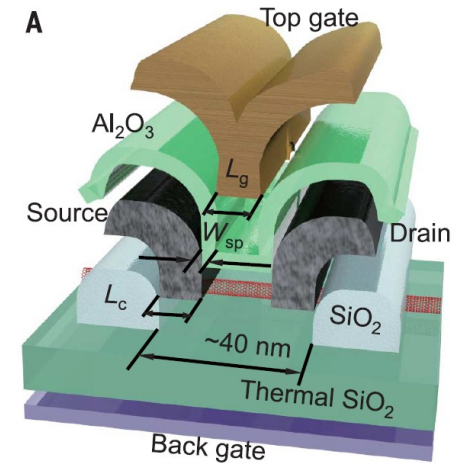
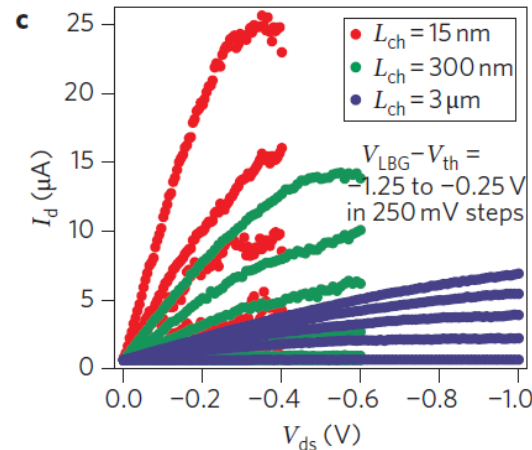
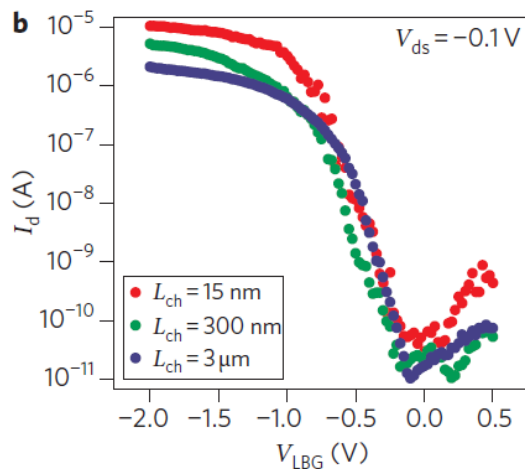
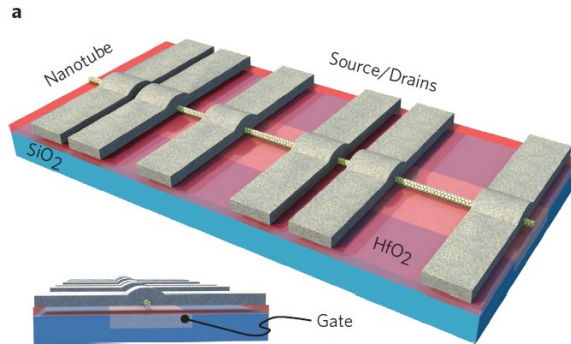
$$\lambda \approx \sqrt{\frac{\epsilon_{ch}}{2\epsilon_{ox}}} t_{ch} t_{ox} \left(1 + \frac{\epsilon_{ox}}{4\epsilon_{ch}} \frac{t_{ch}}{t_{ox}} \right)$$

>

$$\lambda \approx \sqrt{\frac{\epsilon_{ch}}{4\epsilon_{ox}}} t_{ch} t_{ox} \left(1 + \frac{\epsilon_{ox}}{4\epsilon_{ch}} \frac{t_{ch}}{t_{ox}} \right)$$

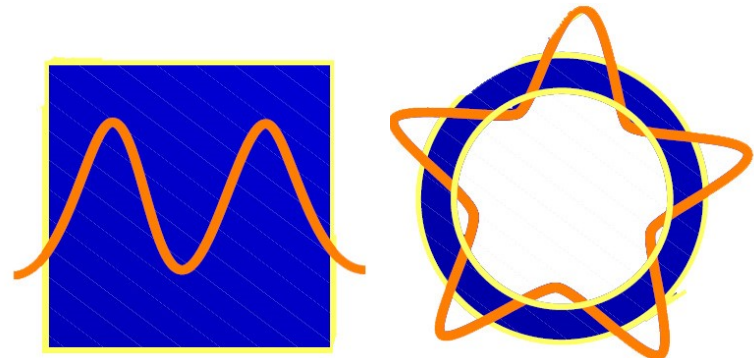
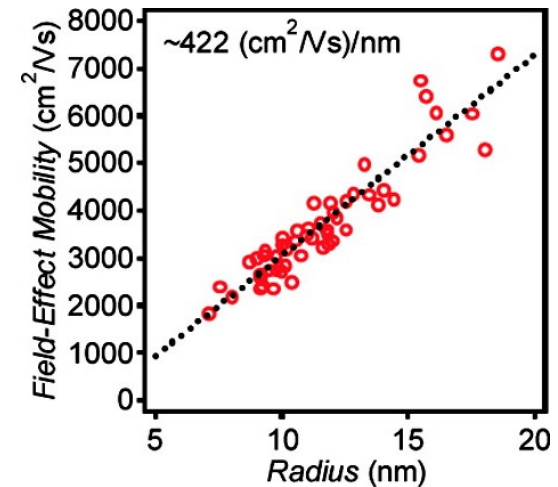
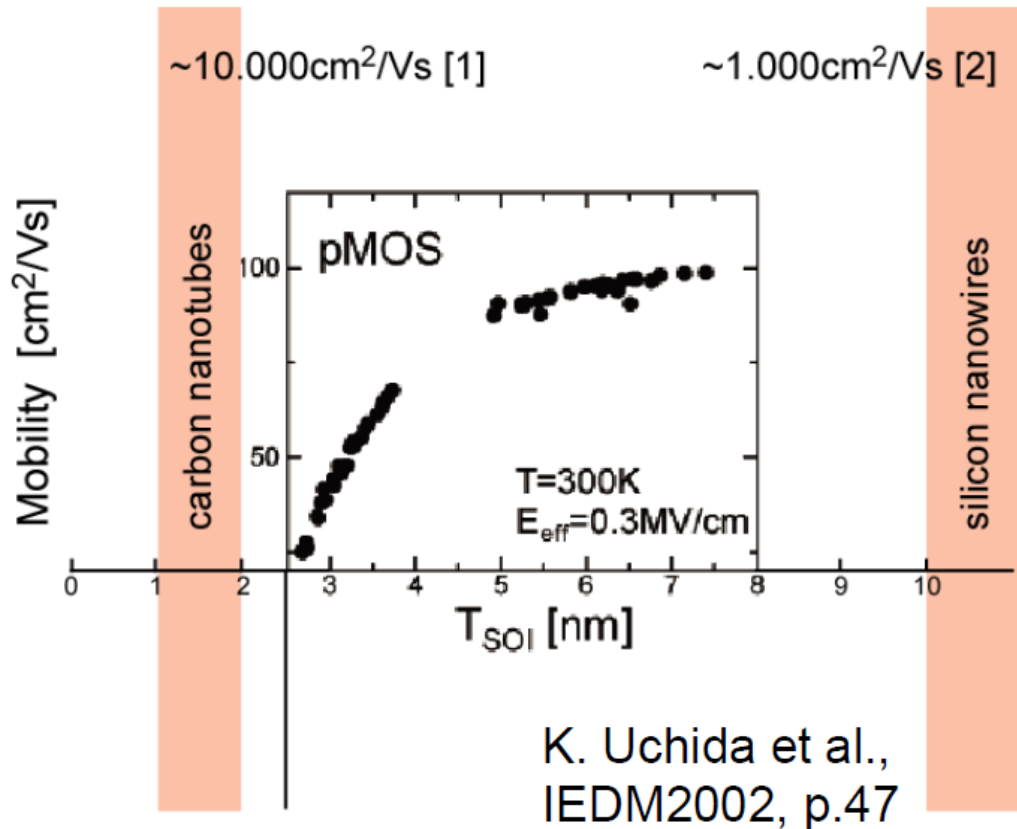
Gate length scaling

- No short channel effects (DIBL, SS degradation) down to $L_g=15$ nm
- $I_{on} = 0.9$ mA/ μ m \rightarrow normalisation ?
- on/off ratio = 10^5
- SS = 90 mV/dec also for short devices



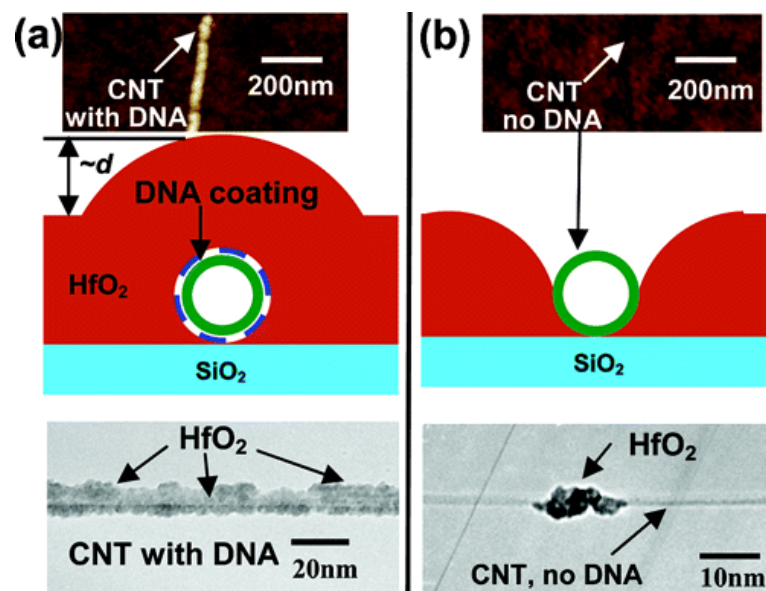
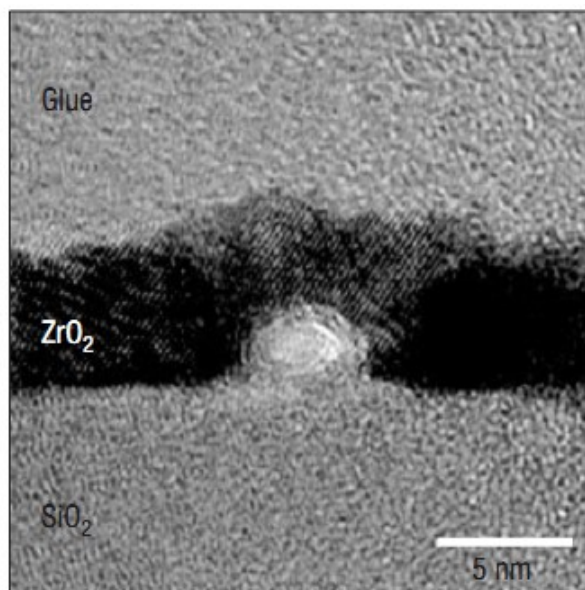
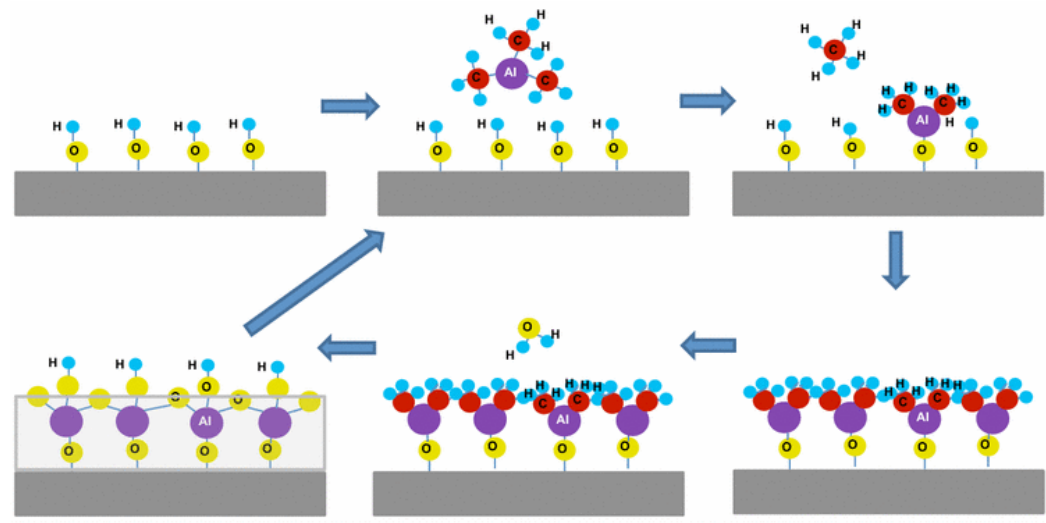
Surface scattering

- Need to reduce channel thickness to be able to reduce L_g
- Surface roughness scattering gives $\mu \sim t^6$ for SOI MOSFETs
- Not a problem for CNTs – no unsaturated bonds / no roughness



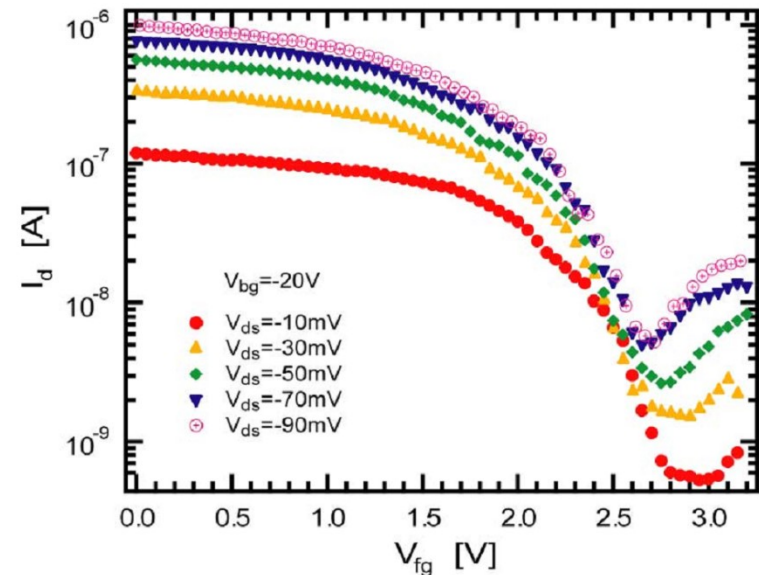
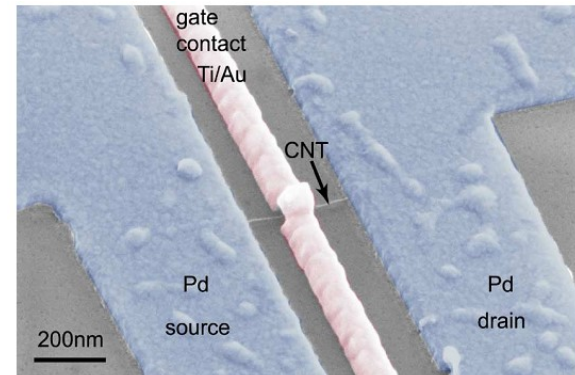
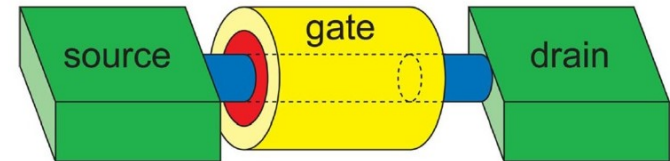
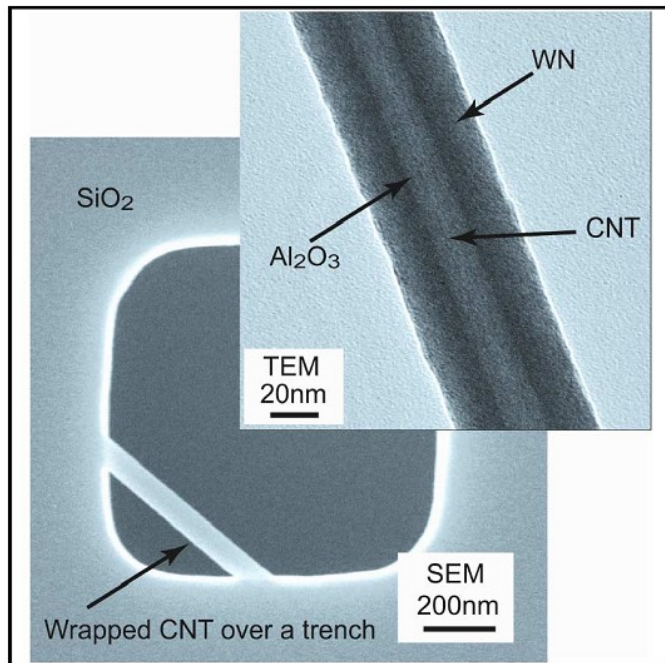
High k gate dielectrics

- Need OH groups for ALD.
- Overgrow from surface or functionalize CNT.
- No dangling bonds give nice interface? Traps in oxide?



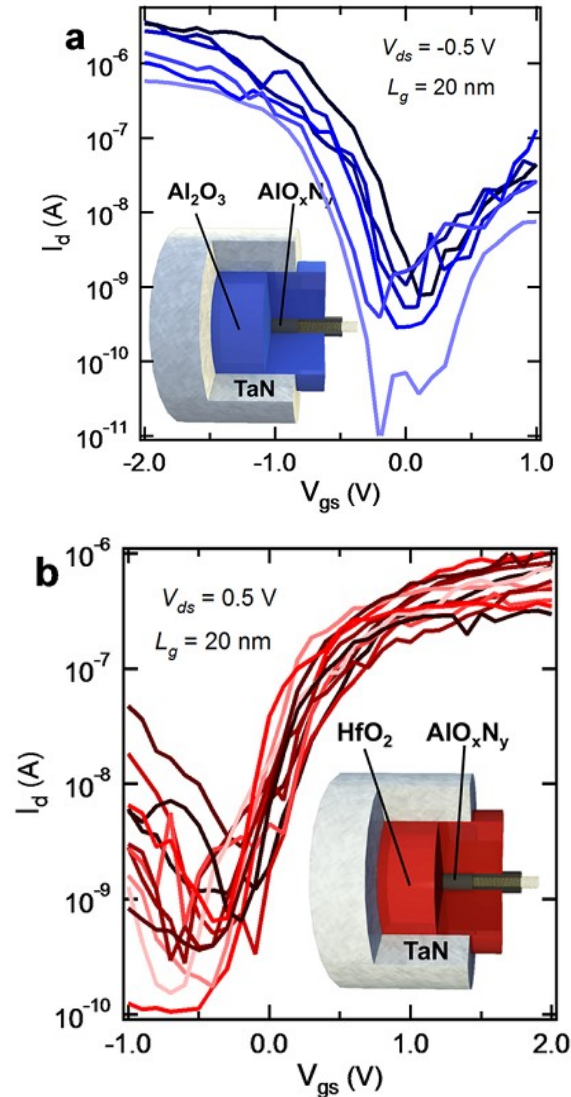
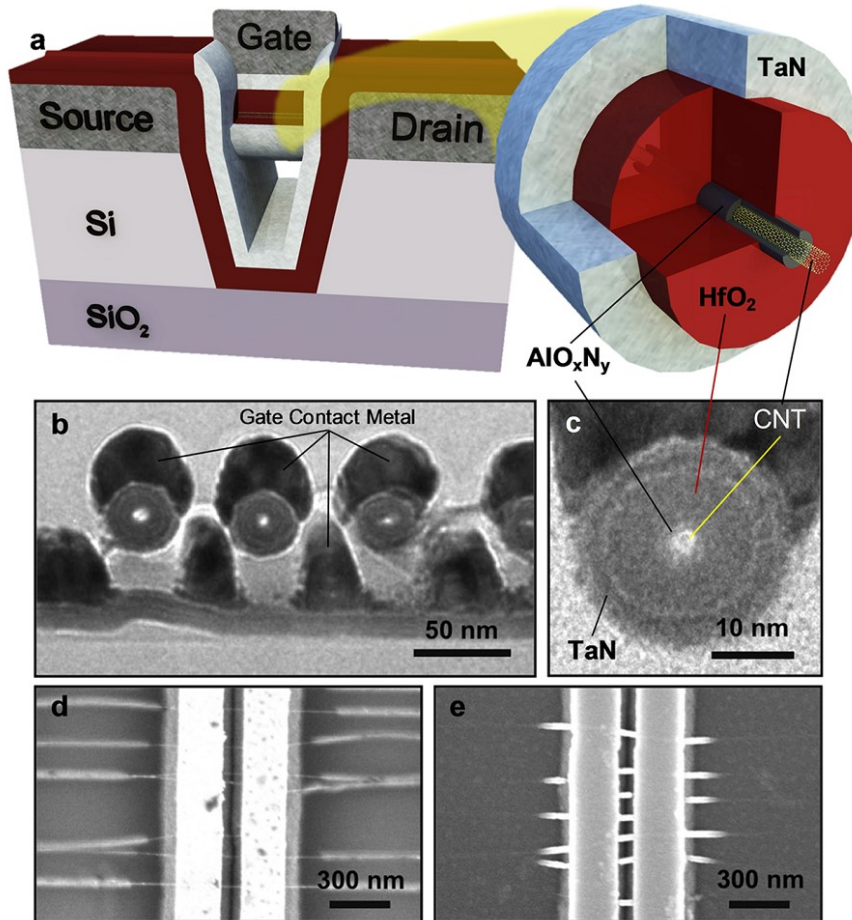
Gate-all-around CNTFET

- Wrap CNT in Al_2O_3 and WN using ALD
- Poor subthreshold swing due to interface traps and short channel effects



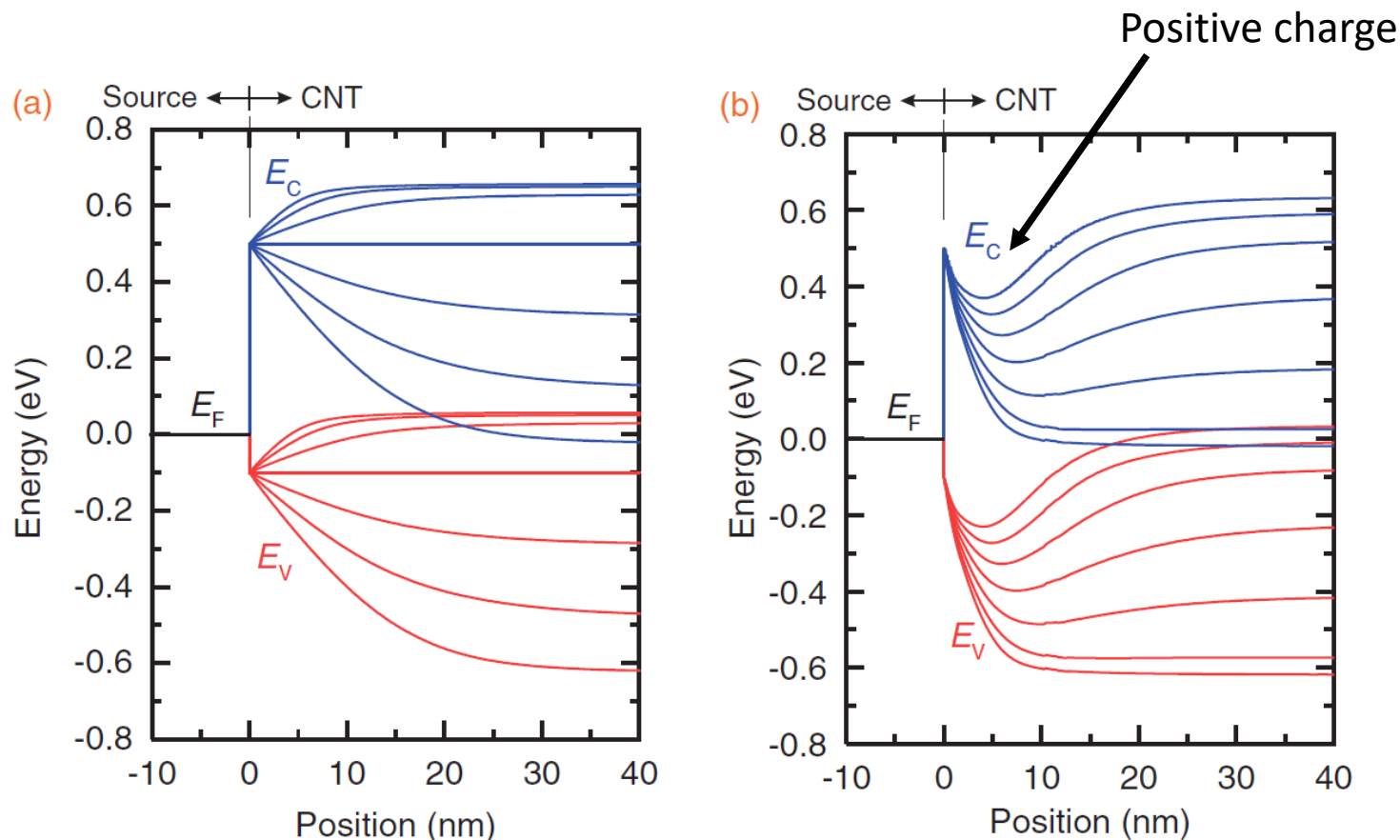
Different high-k

- Control p or n-type by different high-k



Conversion from p- to n-type

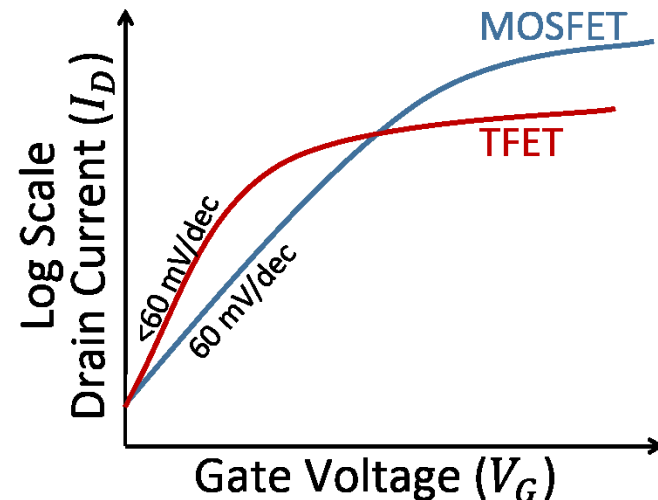
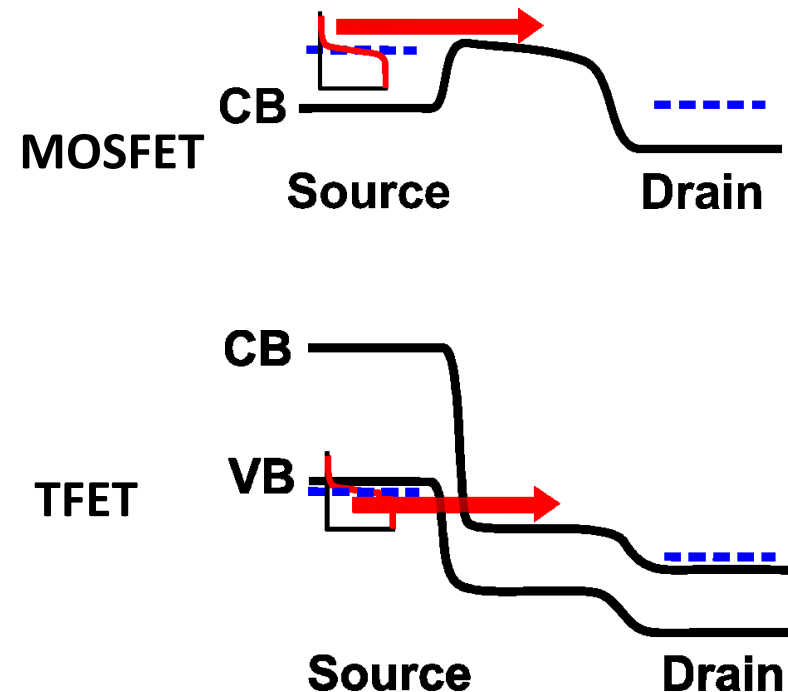
- High work function metal \rightarrow low Schottky barrier to valence band
- Positive charge (in e.g. oxide) close to contact increases barrier to valence band and thins down barrier to conduction band.



Improving the inverse subthreshold slope

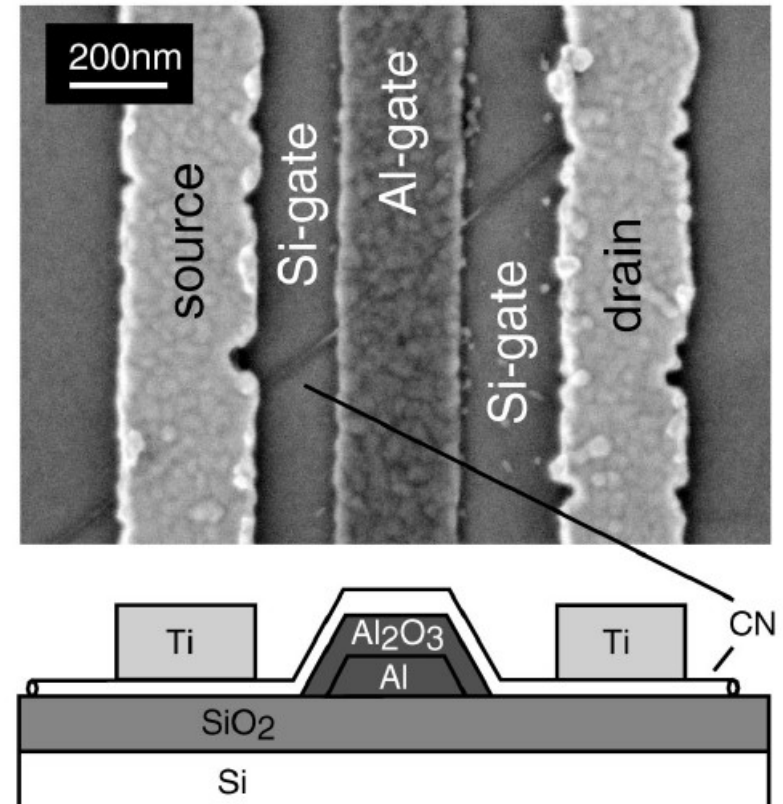
- "conventional" FETs rely on thermionic emission over a barrier
- $SS \geq \ln(10) k_B T = 60 \text{ mV/dec}$ at room temperature
- A decreased SS enables a lower V_{dd} while keeping the same on/off ratio -> increased speed and reduced power consumption

$$S = \left(\frac{d \log_{10}(I_d)}{dV_g} \right)^{-1}$$



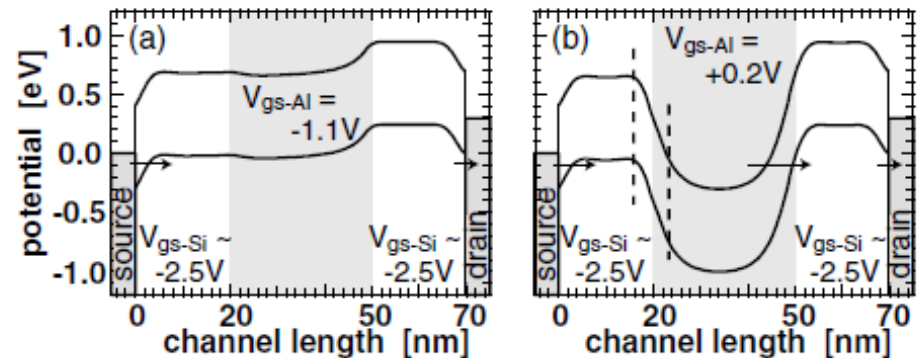
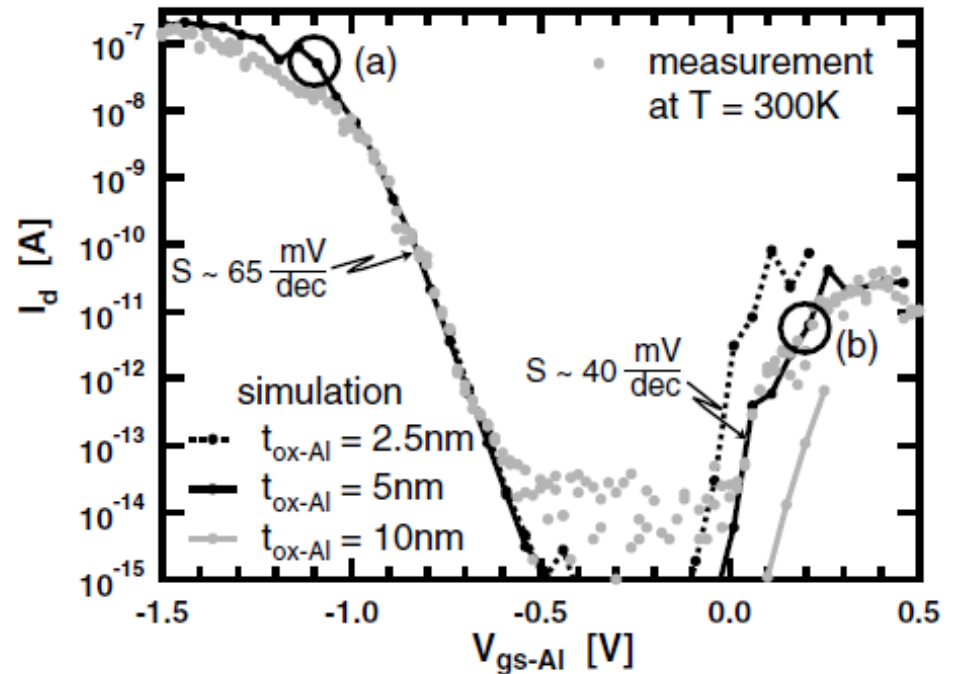
Band-to-band tunneling transistor

- + λ is a few nm in CNT - > sharp band bending
- + Low effective mass
- + Long mfp
- + Same effective mass of electrons and holes
- + Direct band gap



Electrical characteristics

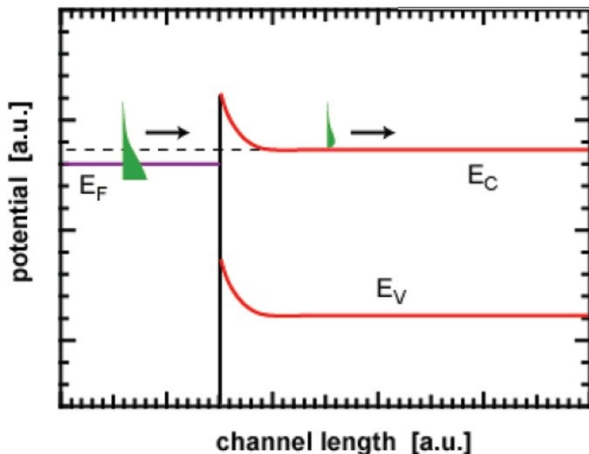
- Back gate to form p-type regions
- Al gate to switch FET
- Ambipolar characteristics
- $SS=40$ mV/dec for the n-branch
- Band-to-band tunneling at the border between the gates



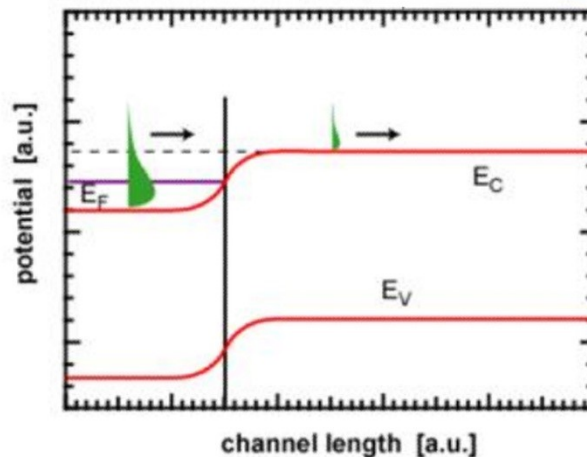
Mechanism of SS reduction

- Only high energy tail of Fermi-Dirac distribution is transferred in thermionic emission or in tunneling through Schottky barrier
- Band-to-band tunneling "filters" the Fermi-Dirac distribution
- For BTB tunneling, small movement of bands give large change in current i.e. small SS

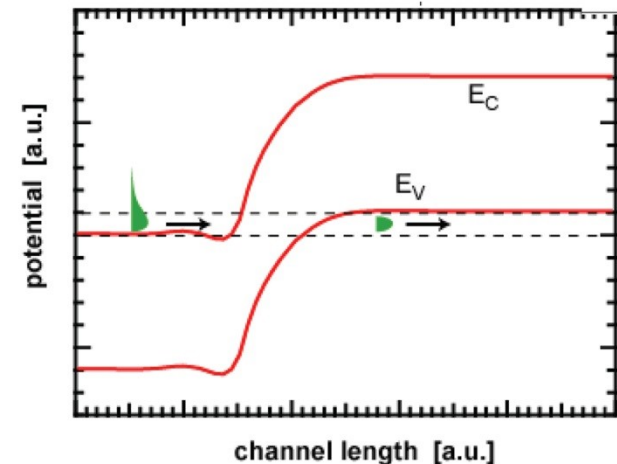
tunneling at Schottky barrier



thermionic emission



band-to-band tunneling



Outline

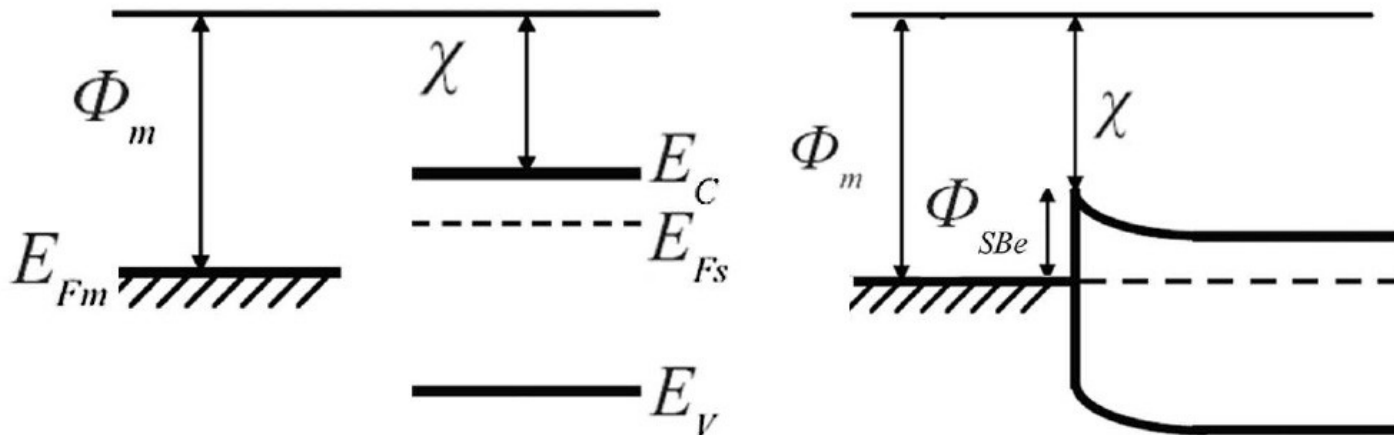
- Basics of graphene and CNTs
 - Structural
 - Electronic
 - Production of CNTs
- Advantages of CNTs for FETs
 - Electrostatics -> length scaling
 - High-k compatibility
 - Band-to-band tunneling
- Challenges of CNT integration
 - Contacts
 - Doping
 - Positioning
 - Chirality control
- Towards integration
 - Flexible electronics
 - High frequency performance

Schottky barrier basics

- Potential barrier between metal and semiconductor
- Gives rectifying behaviour
- Change metal work function \rightarrow change SB height
- Too simple !!!

$$\Phi_{SBe} = \phi_m - \chi$$

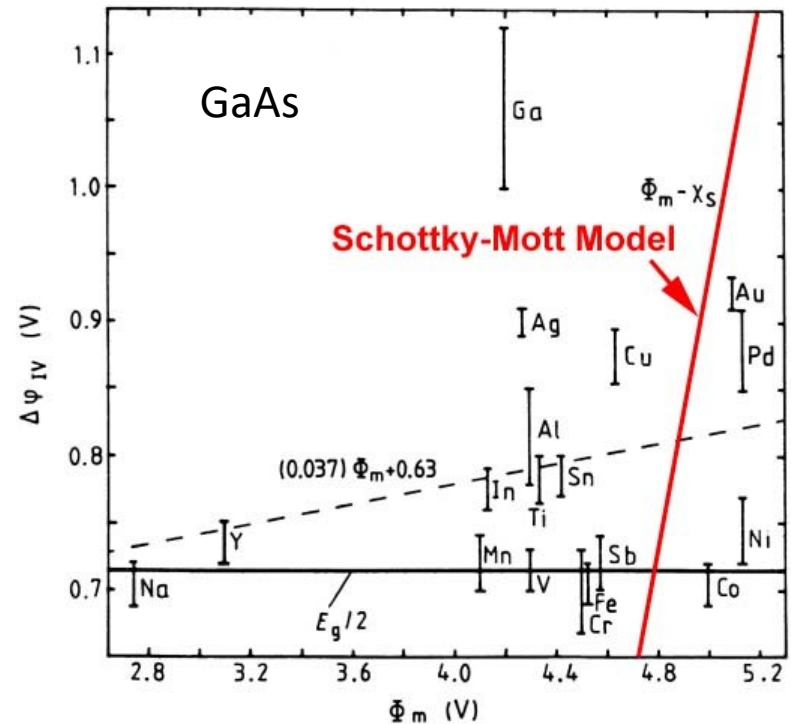
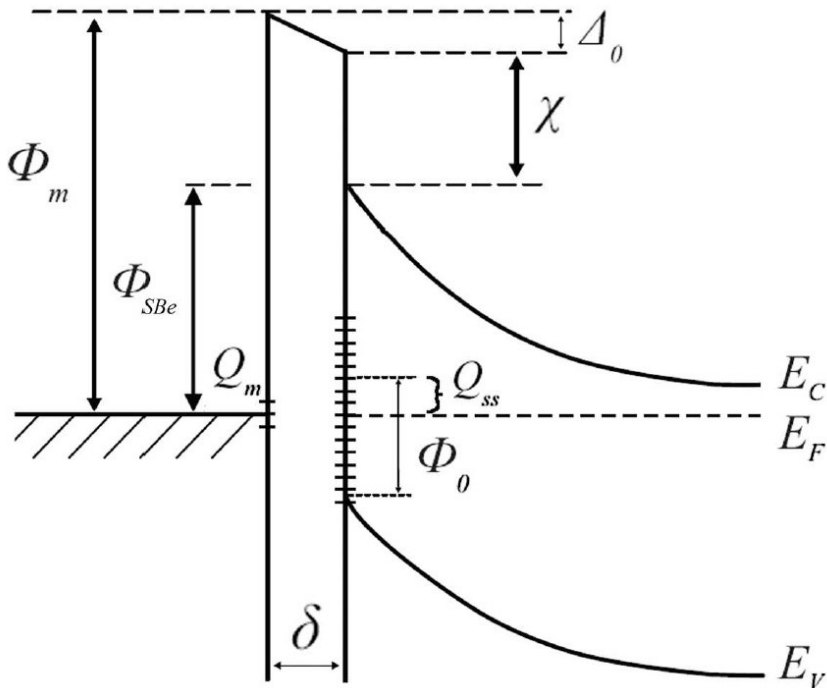
$$\Phi_{SBh} = \chi + E_g - \phi_m = I_s - \Phi_m$$



Fermi level pinning

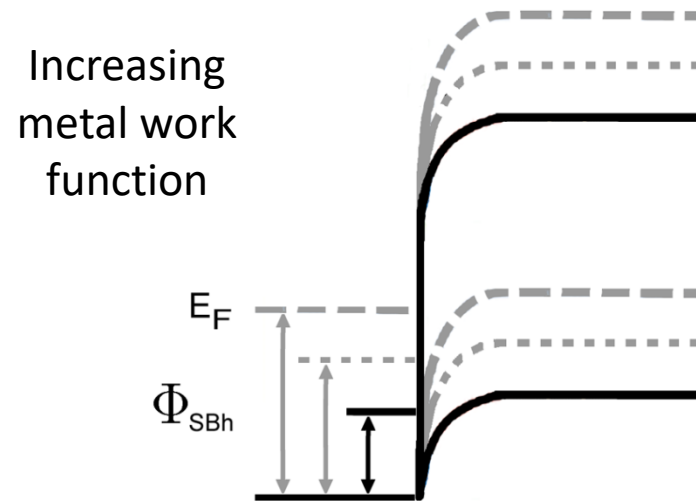
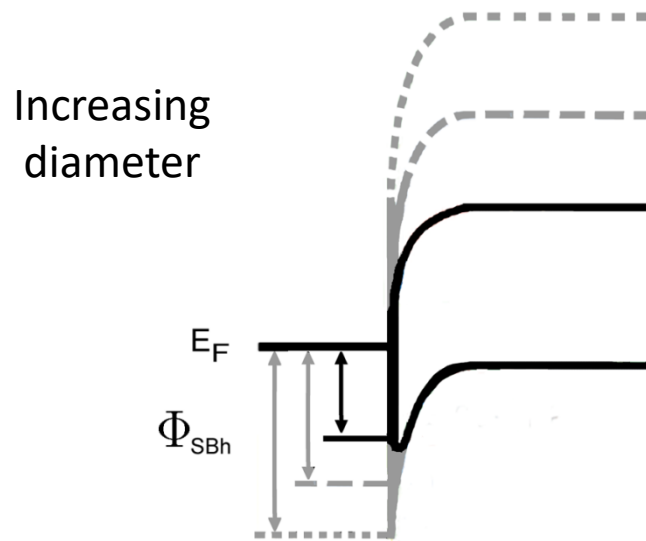
- Interface states form dipoles that shift bands
- SB height often independent on metal work function

$$\Phi_{SBe} = \gamma(\Phi_m - \chi) + (1 - \gamma)(E_g - \Phi_0) \quad \gamma = \frac{1}{1 + \frac{qD_{it}\delta}{\epsilon_i}}$$



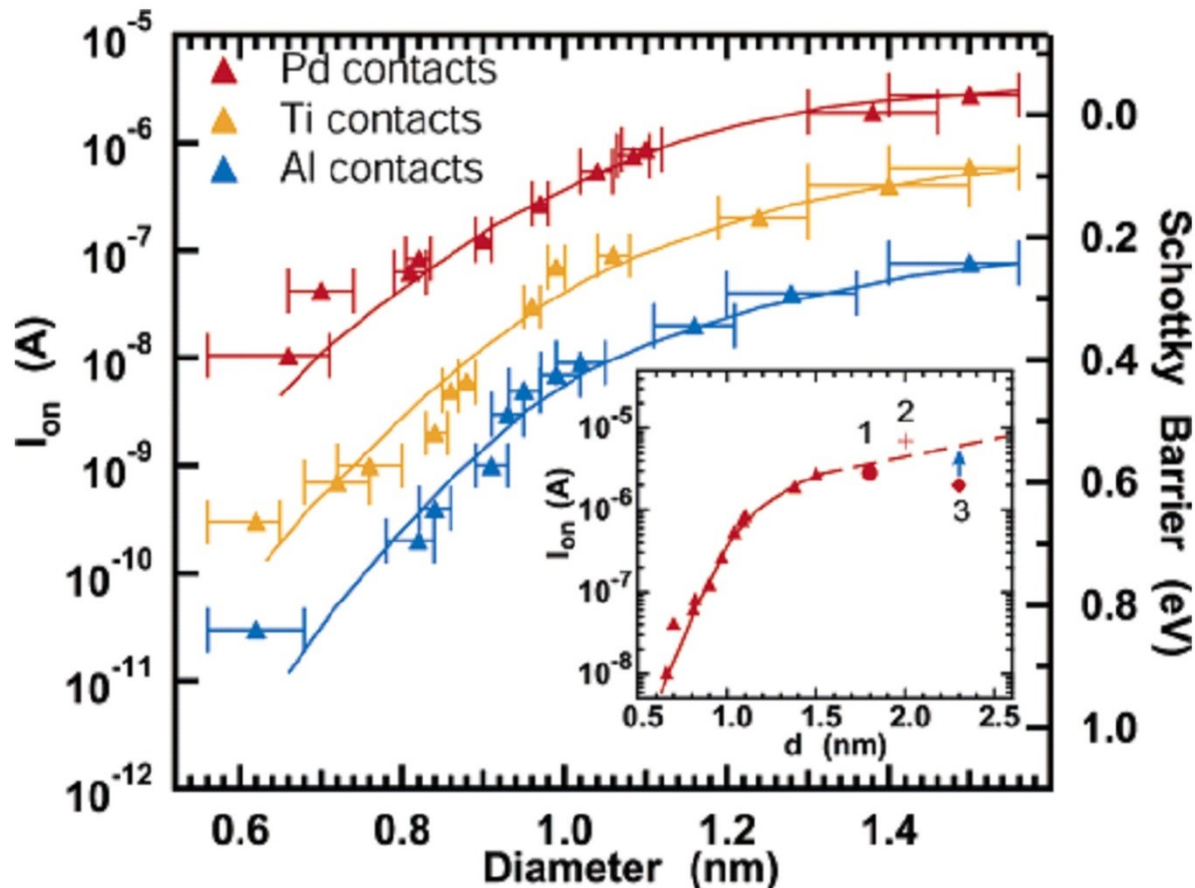
Schottky barrier to CNTs

- Theoretically predicted that interface states have no influence on CNT-metal contacts
- Increasing CNT diameter gives lower barriers
- Increasing metal work function gives lower hole barriers



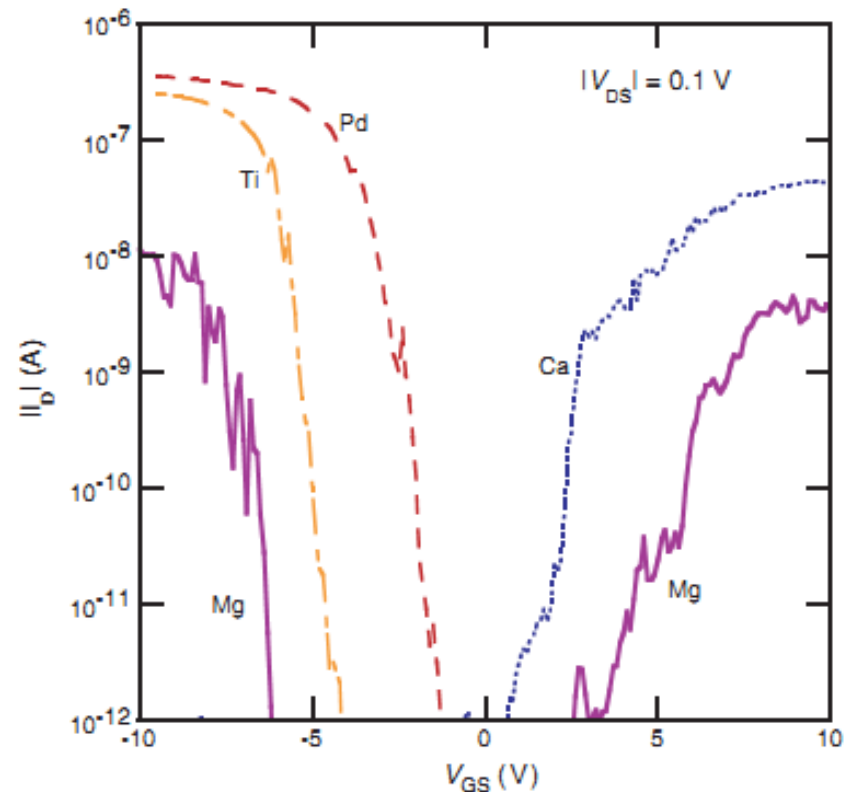
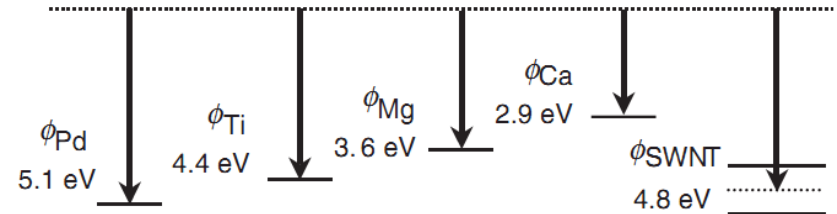
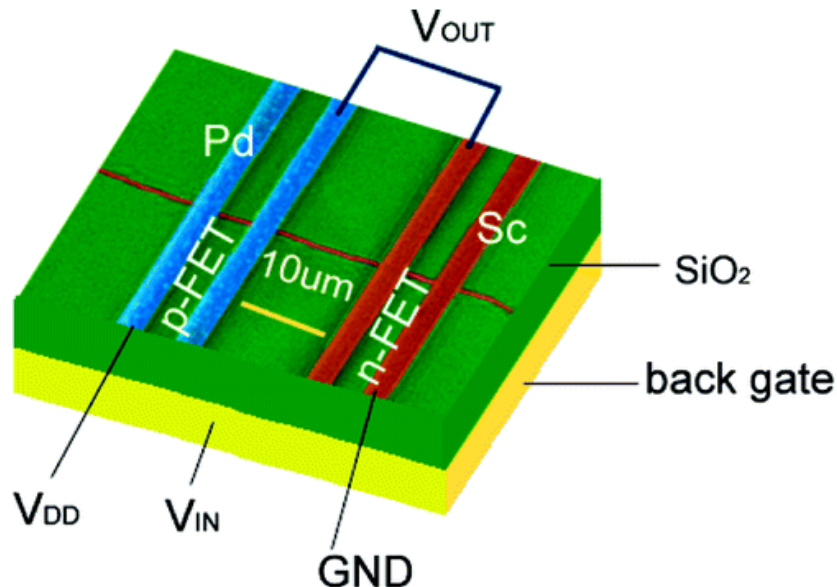
Different contact metals

- Increasing I_{on} with larger CNT diameter
- Increasing I_{on} with higher work function
- No or small effect of Fermi level pinning



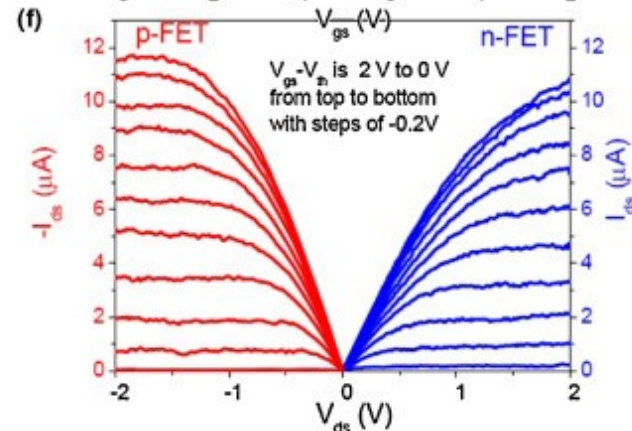
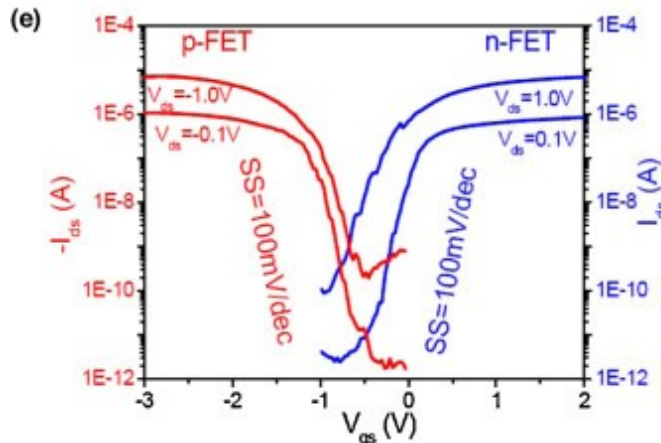
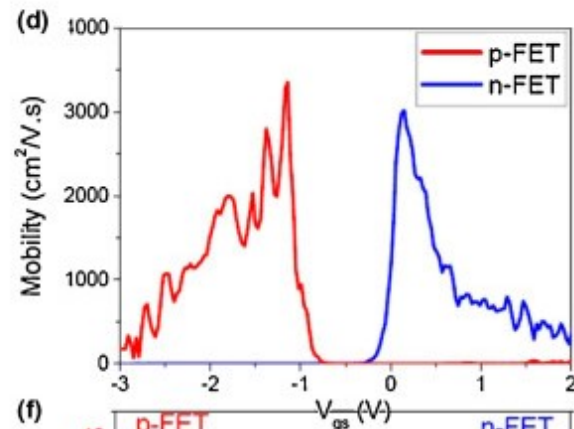
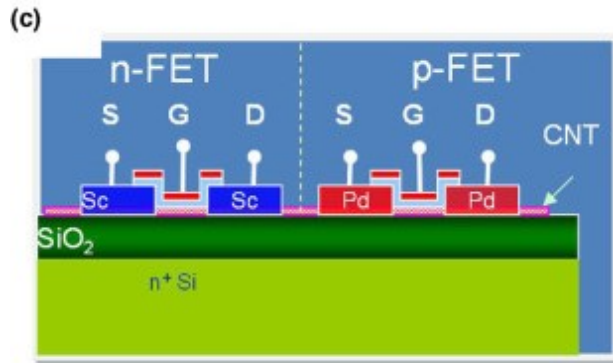
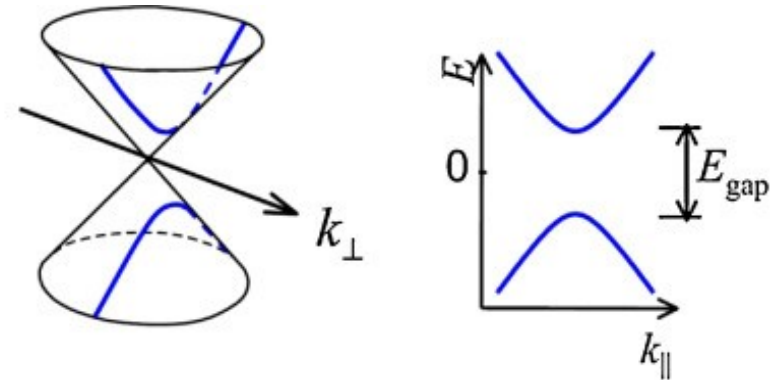
Impact of metal work function

- Can form n or p-type devices using different metals
- Pd best for p-type
- Sc best for n-type



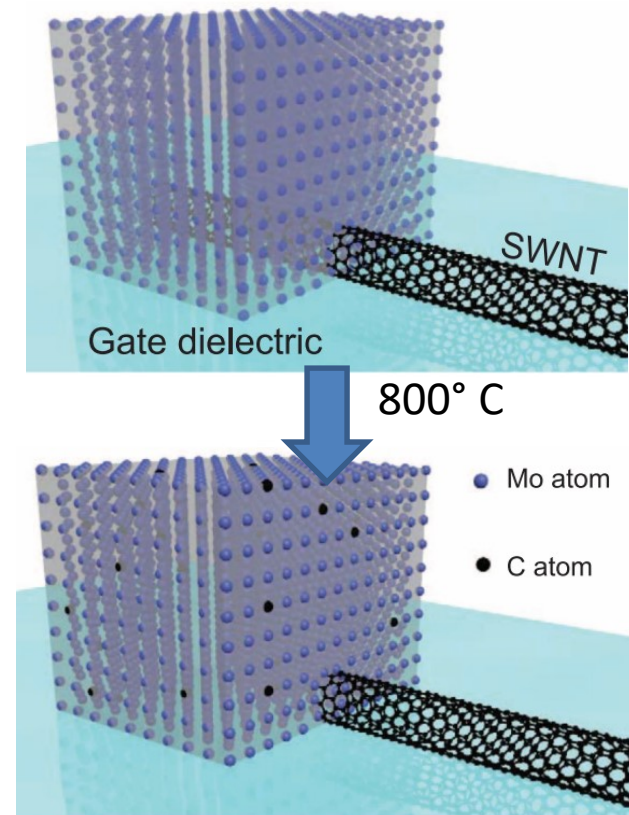
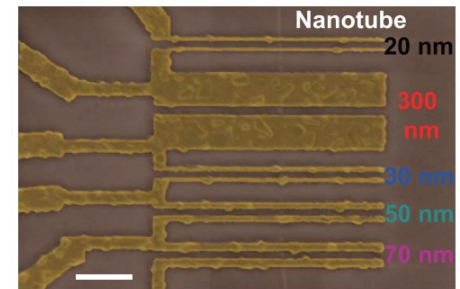
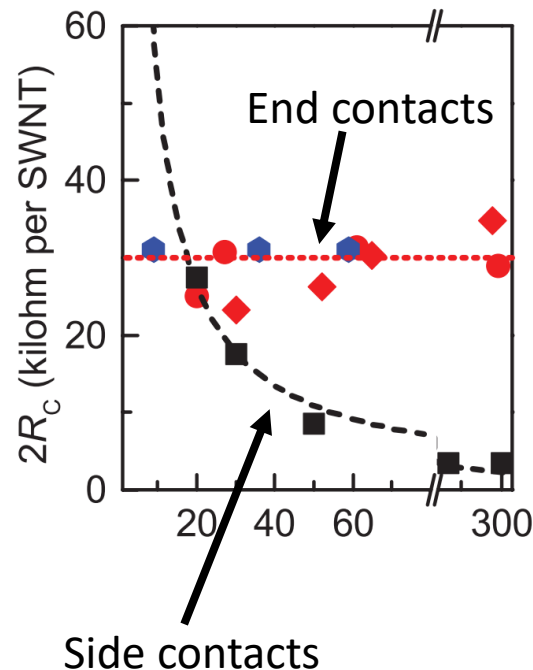
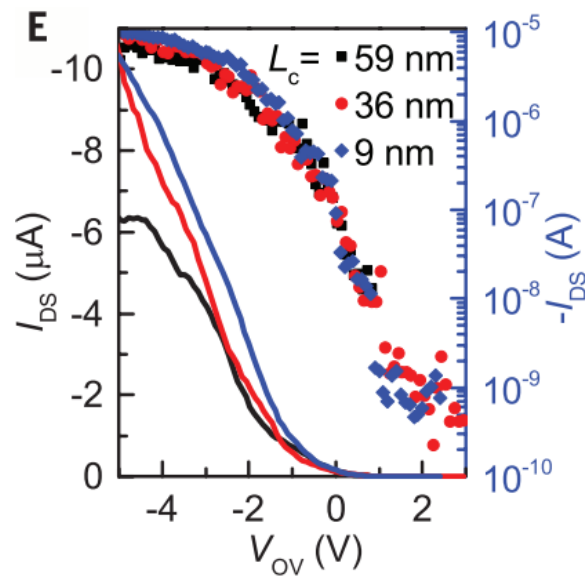
CNTFETs for CMOS

- For most semiconductors $\mu_e > \mu_h$
- Symmetric valence and conduction bands give similar PMOS and NMOS performance for CNTFETs



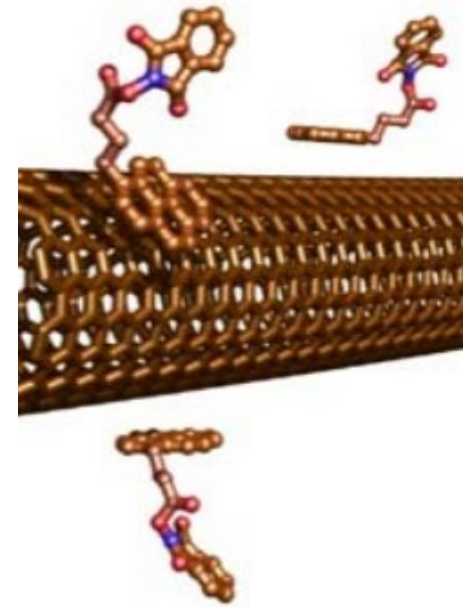
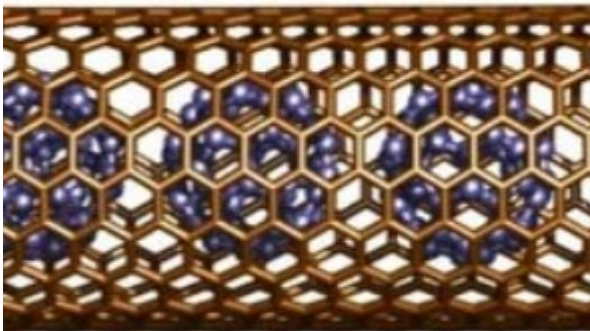
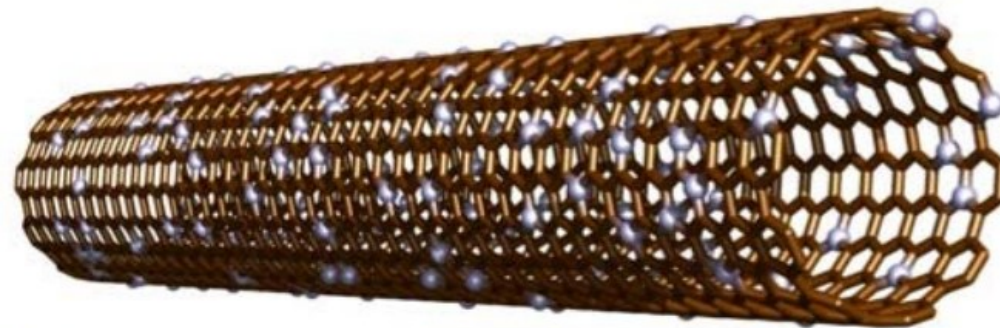
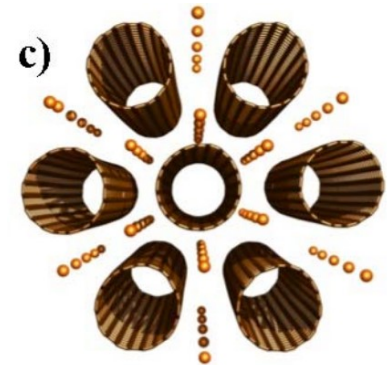
End bonded contacts

- Mo contacts heated to 800°C forms Mo_2C
- Sidecontact transformed to end contact
- Contact only 2 nm²
- Useful for very dense circuits



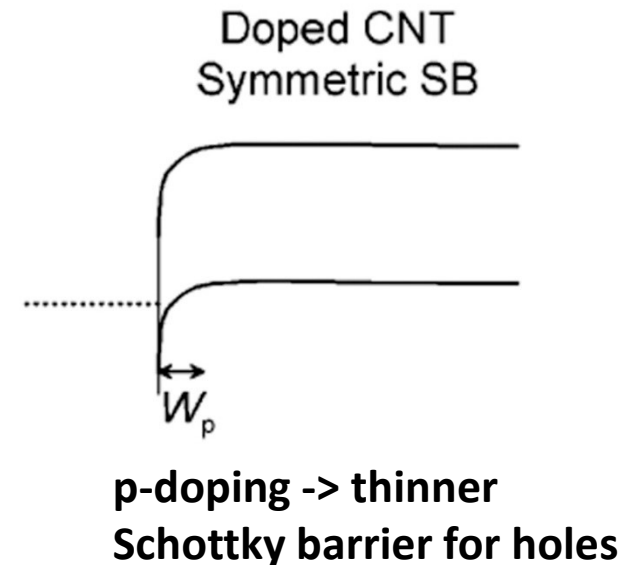
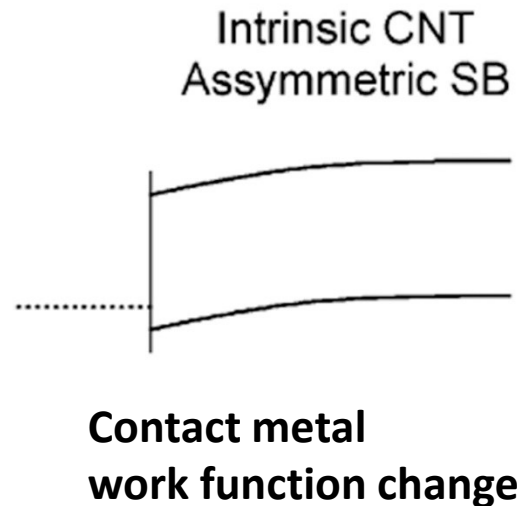
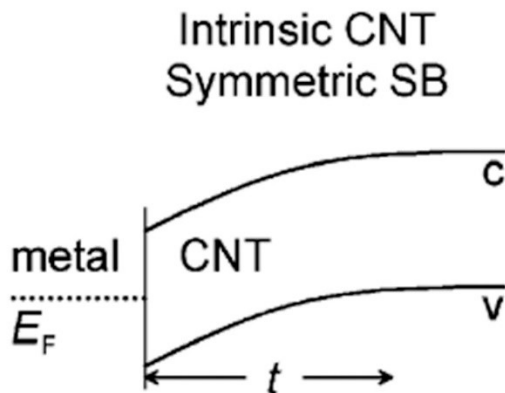
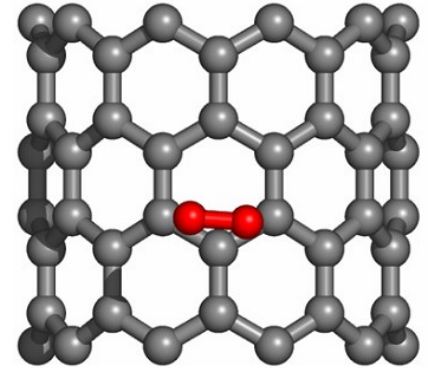
Doping

- Important for CMOS, pn-junctions and good contacts.
- Substitutional doping is difficult without destroying CNTs.



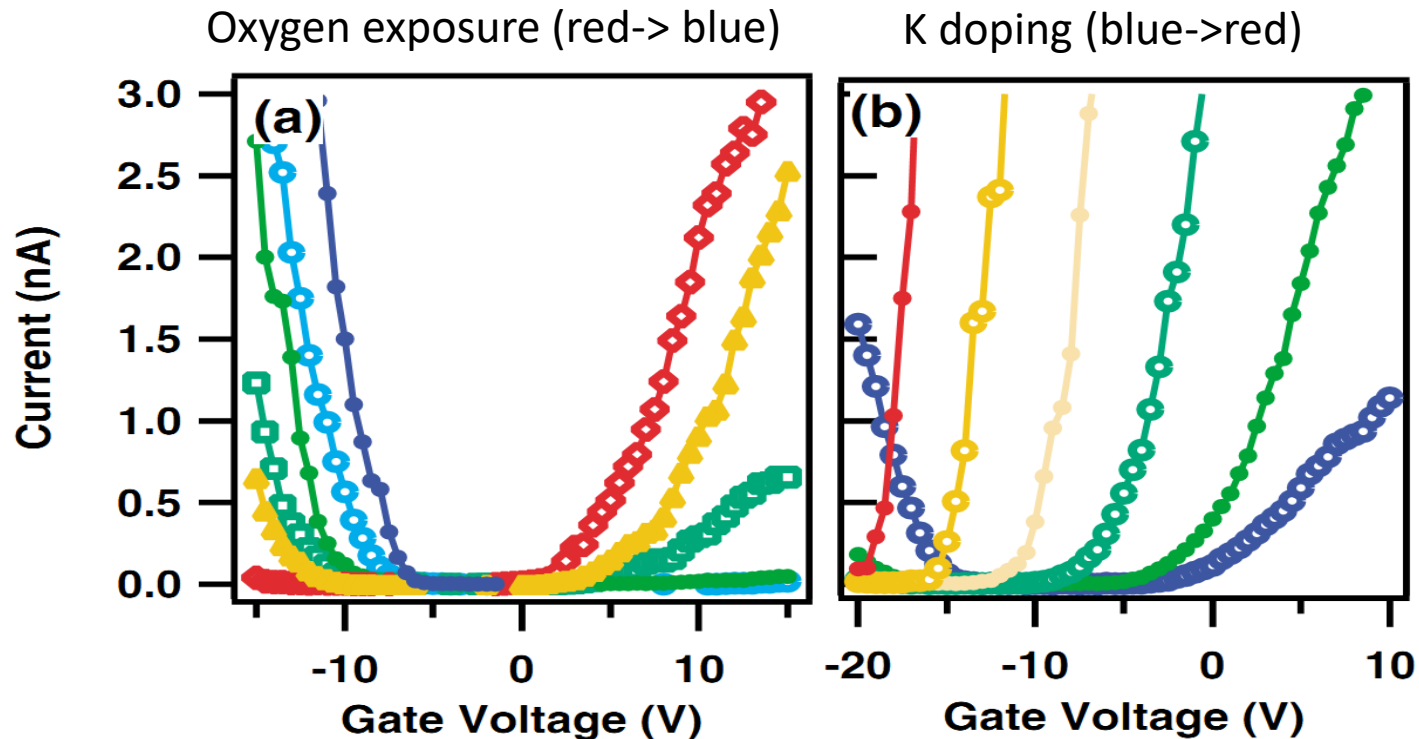
CNTFETs in air

- Physisorbed oxygen p-dopes CNT
OR
- Increases metal work function of contact



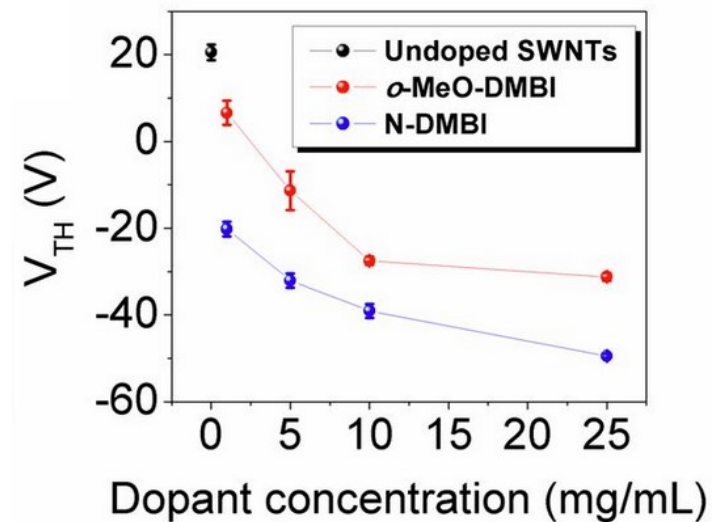
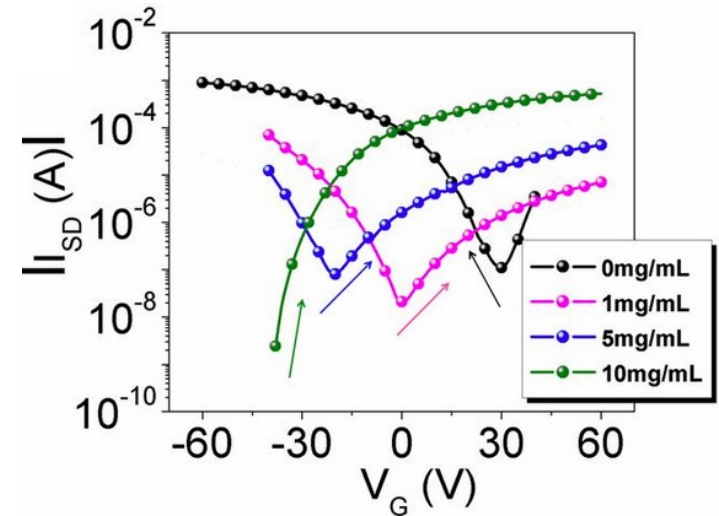
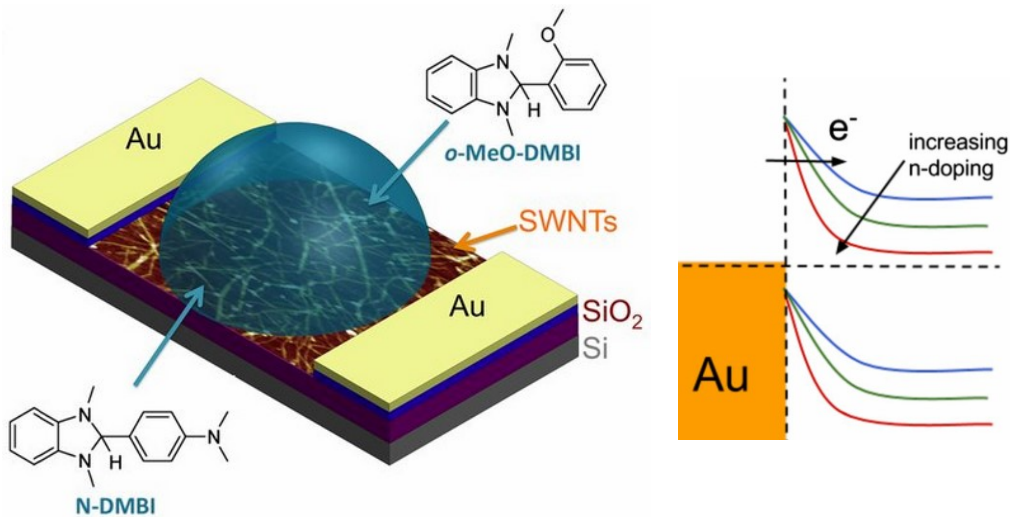
Potassium doping

- O exposure -> p-branch is lowered, n-branch is increased, no V_{th} shift
- K physisorbed on CNT n-dopes by charge transfer -> V_{th} shift
- O: changes work function // K: dopes CNT



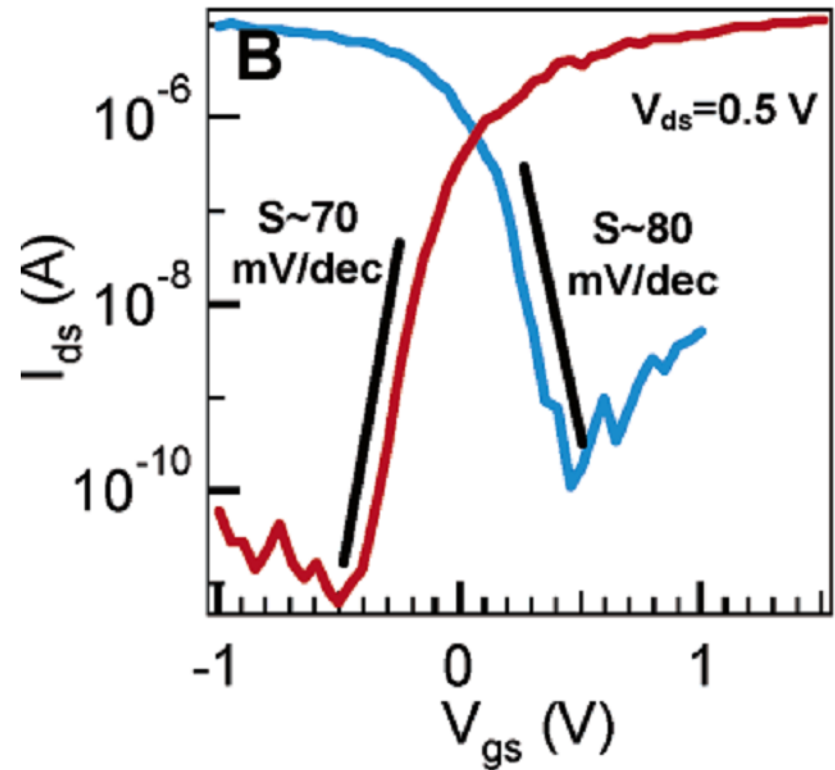
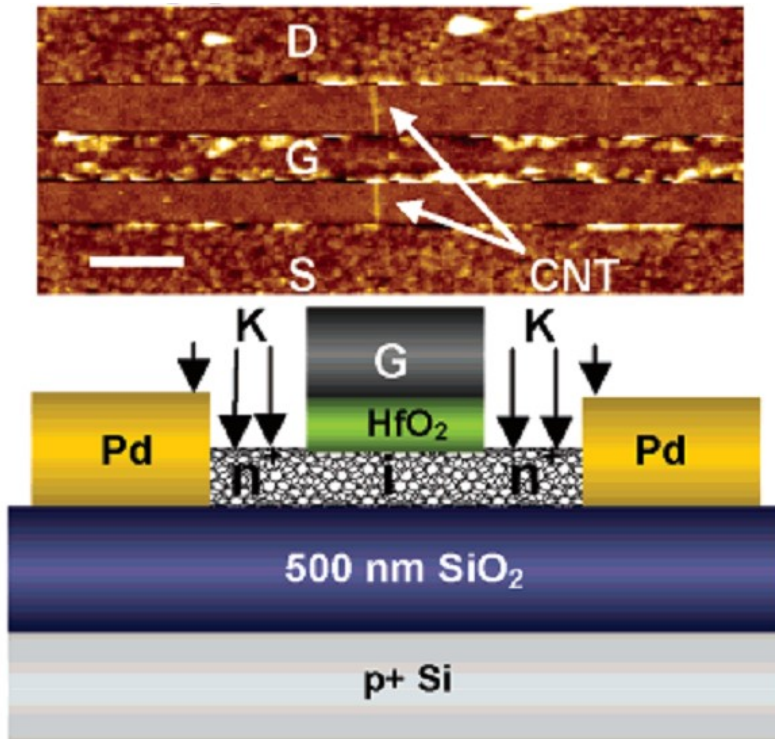
Doping of thin film CNTFETs

- Organic molecules are deposited on CNT network
- n-doping lower Schottky barrier for holes and shifts V_{th}



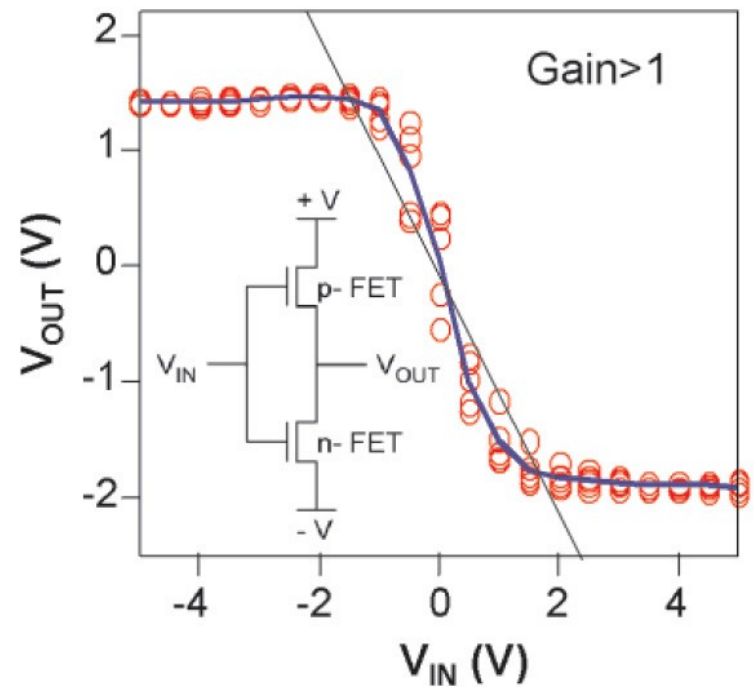
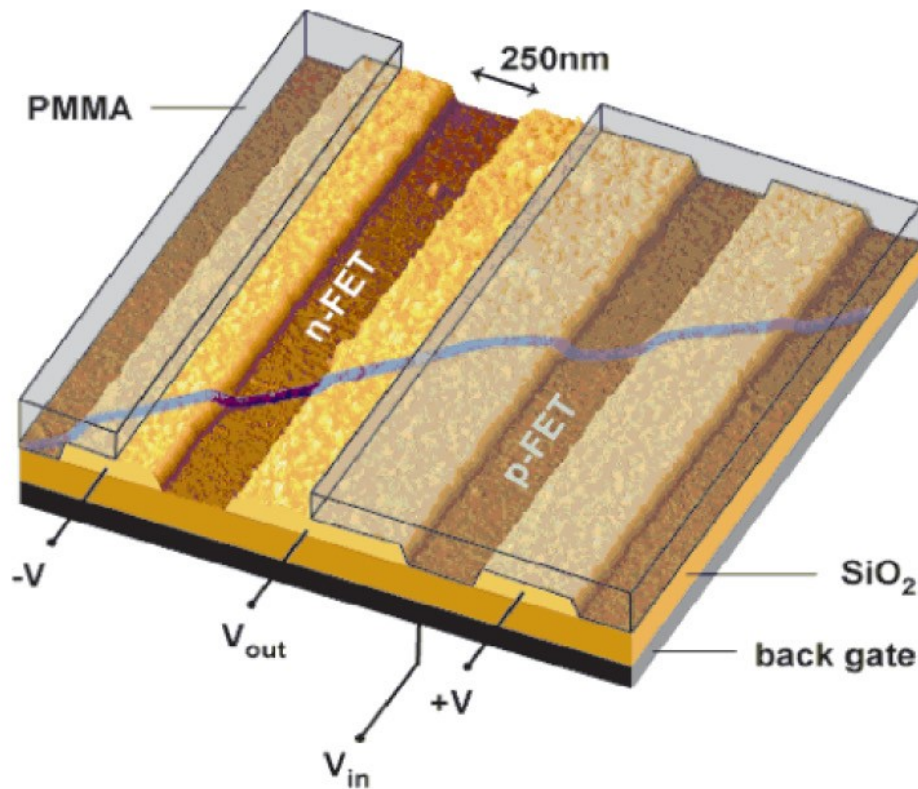
Doped contacts

- n - dope outer CNT segments using K
- Removes influence from Schottky barrier at metal contact



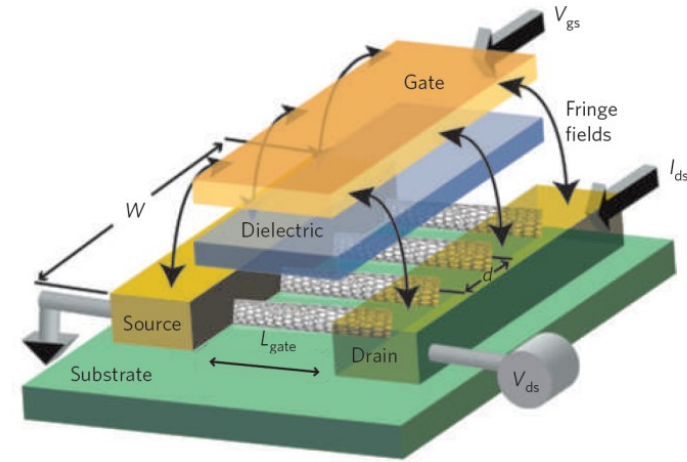
Logic gate on single CNT

- Inverter from p and n CNTFET on the same CNT
- Use K doping or annealing to form n-CNTFET

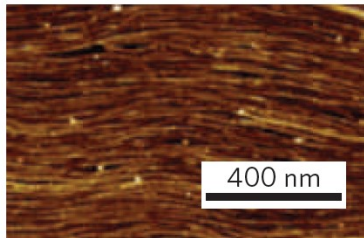


Positioning

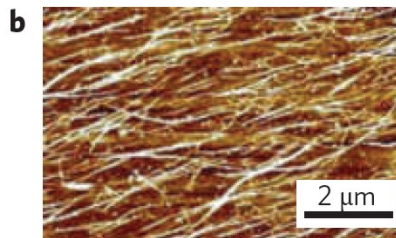
- Multiple parallel CNTs in each FET increases I_{on} , g_m
- Dense packing reduces parasitic capacitances
- Need to control position and orientation of CNTs pre- or postgrowth



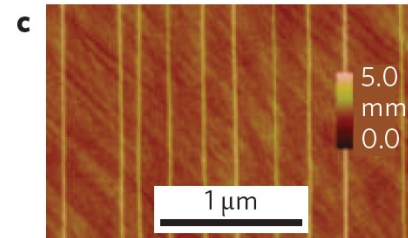
Langmuir-Blodgett



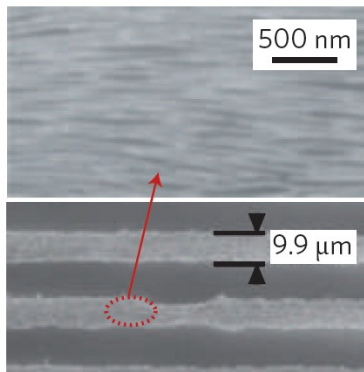
Spin-coating



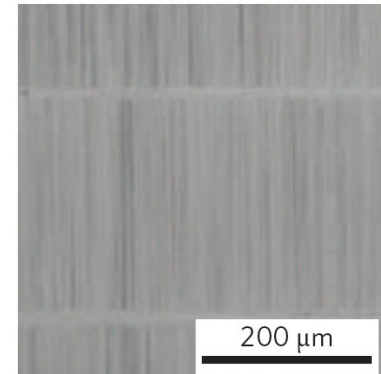
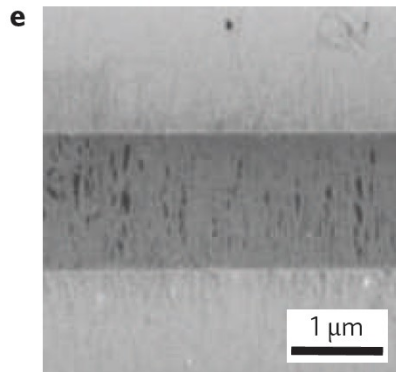
CVD



Droplet

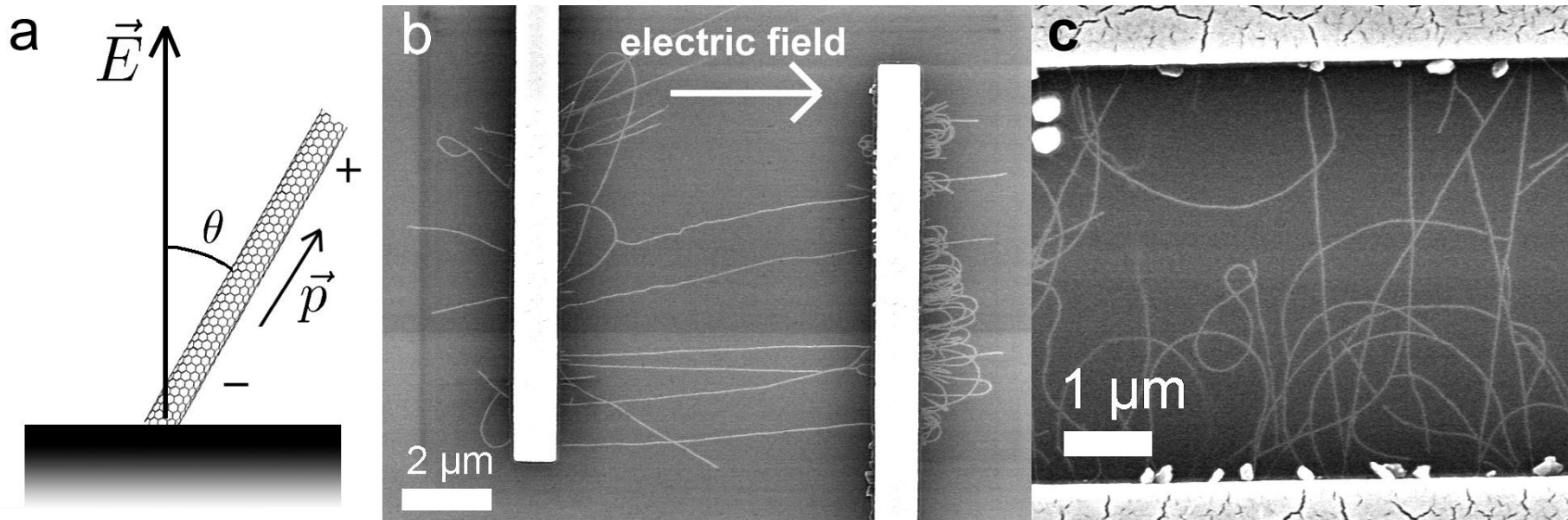


Dielectrophoresis



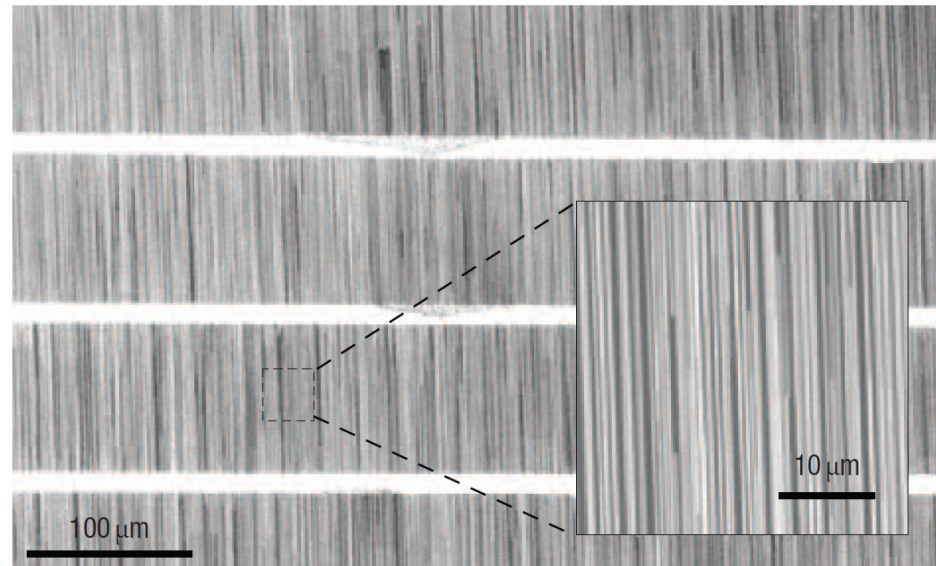
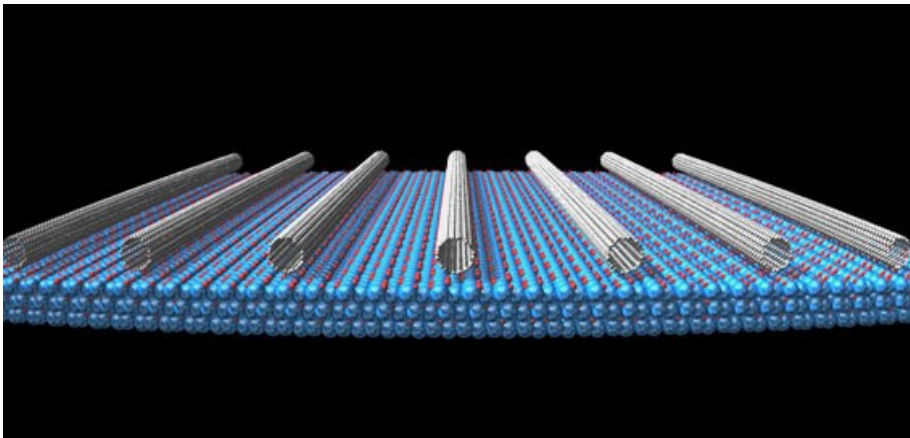
Electric field alignment

- Apply voltage to electrodes during CVD
- Dipole in CNTs align them with field lines
- Difficult to implement for large scale circuits



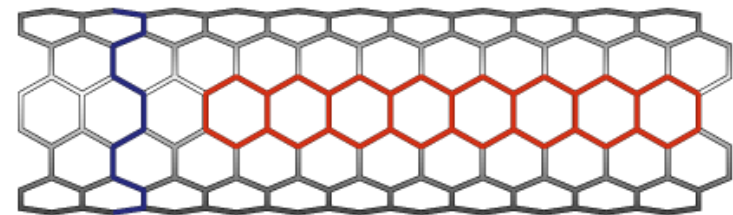
“epitaxial” alignment

- CNTs align in certain crystal orientations of sapphire (Al_2O_3) or quartz substrates
- CNTs align at atomic steps
- Strong attractive interaction between CNTs and Al atoms
- 99.9% are aligned within 0.01°
- 10 CNTs / μm

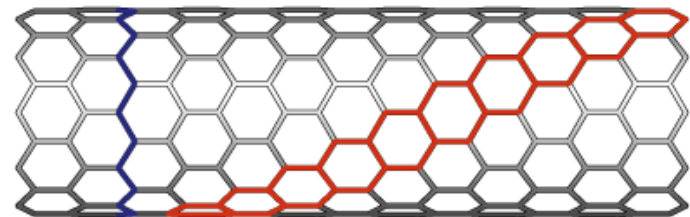


Chirality control

- Metallic CNTs in FETs -> leakage currents - > poor on/off ratio
- Need chirality control or at least control of CNT type
- Need to either:
 - Selectively grow only metallic or semiconducting
 - Separate the two types
 - Selectively destroy one type



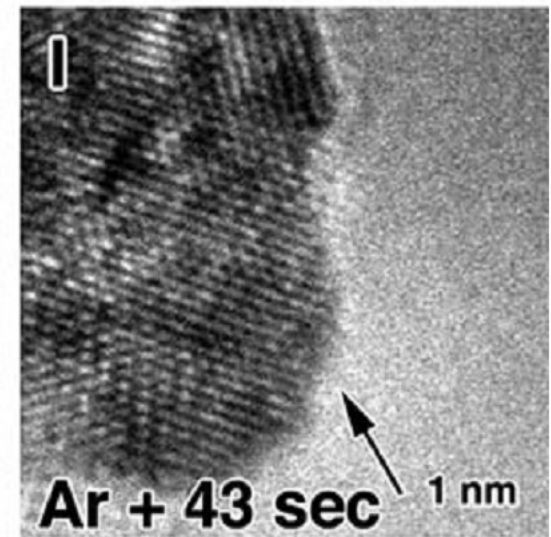
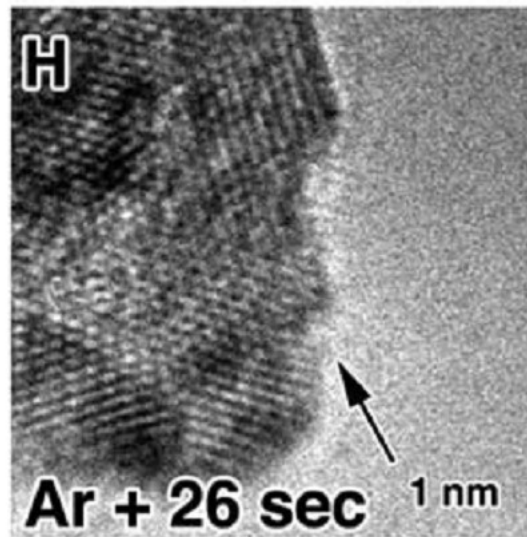
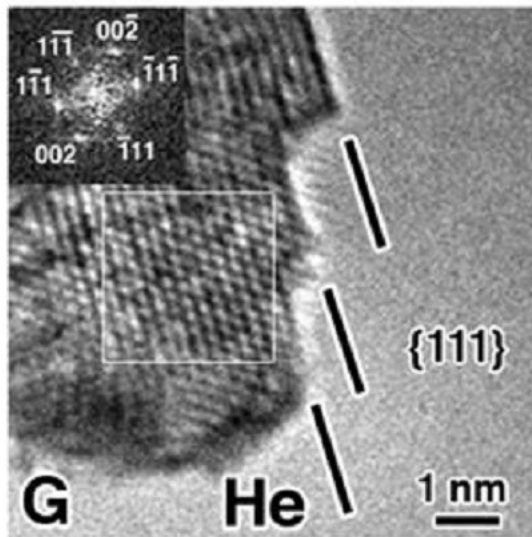
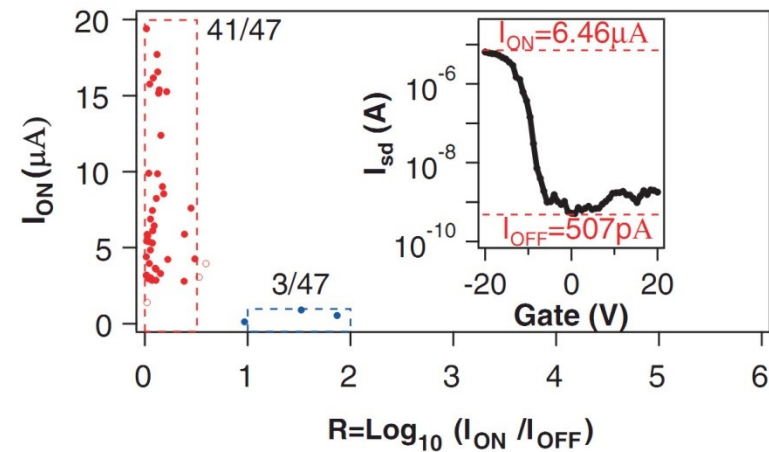
Armchair



Zig-zag

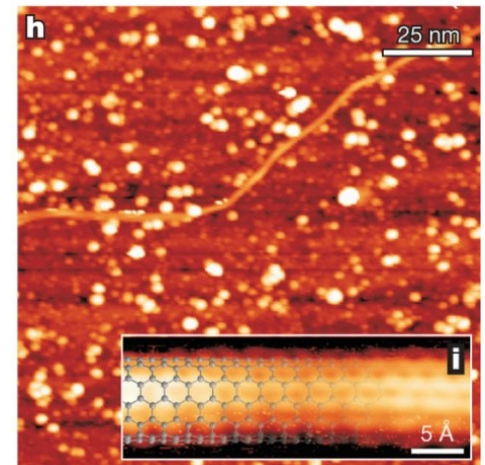
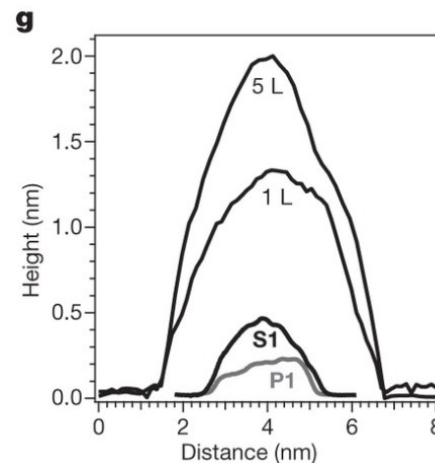
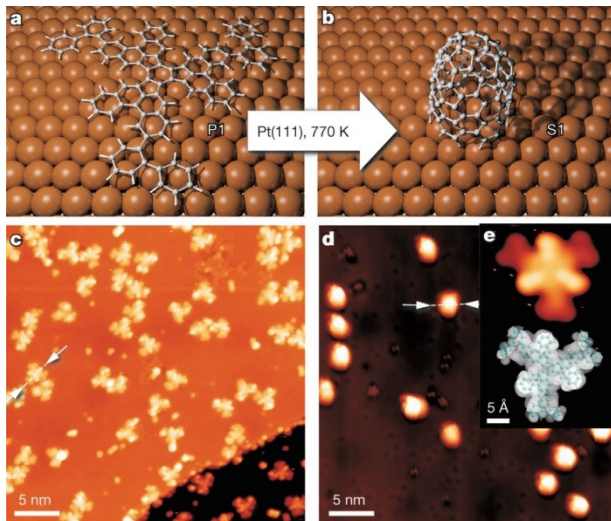
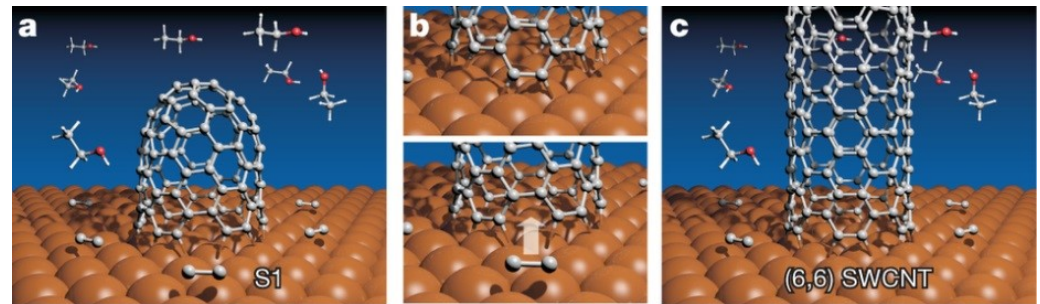
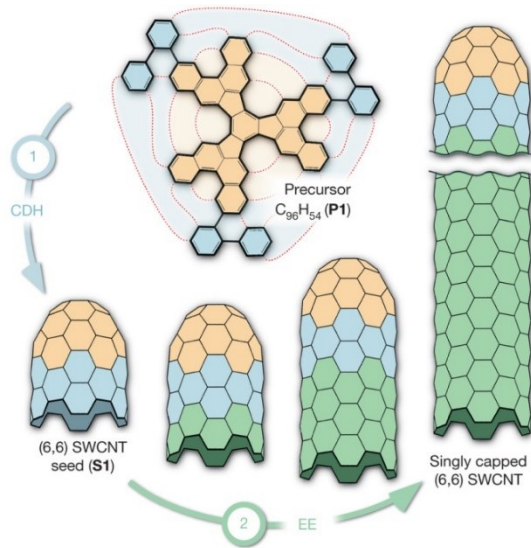
Selective growth

- Anneal metal catalyst in Ar, He or H₂
- Increased metallic CNT part from 33% to 91%
- Strong facets when annealed in He
- Steps in particle important for chirality control?
- Not well understood!



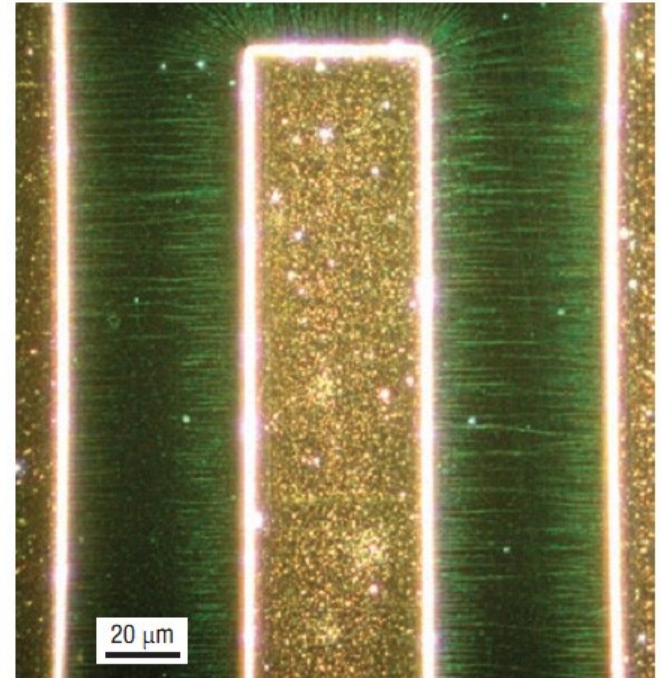
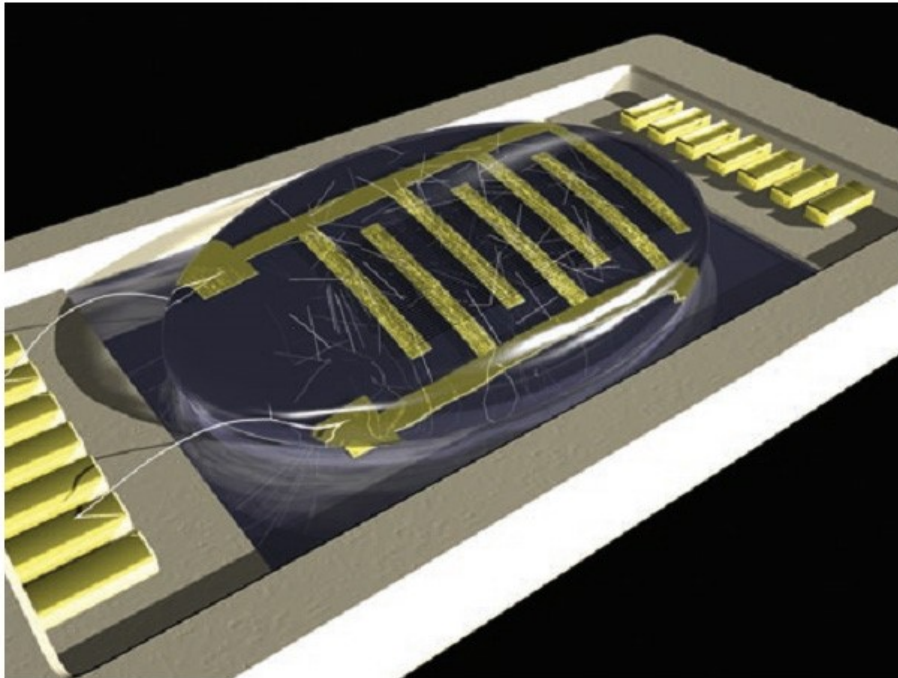
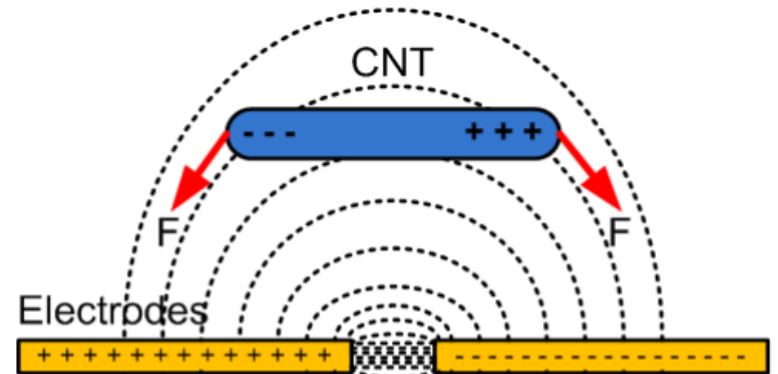
Templated growth

- Molecule defines cap
- Only (6,6) CNTs i.e. "real" metallic



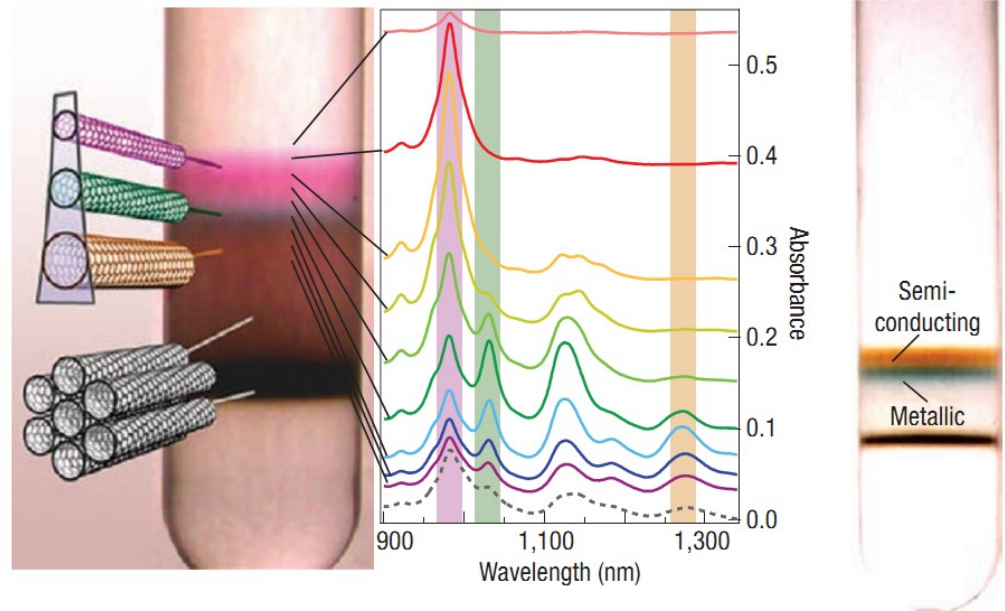
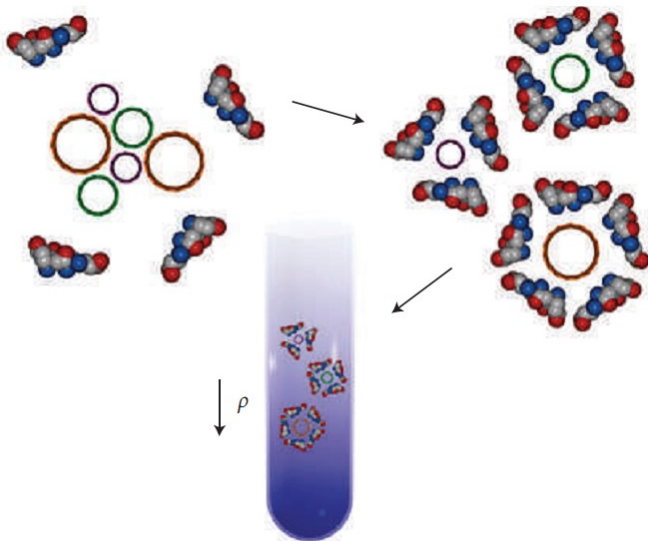
Separation by dielectrophoresis

- AC voltage between electrodes
- Metallic CNTs attracted to electrodes and removed from suspension
- Only small scale (nanograms)



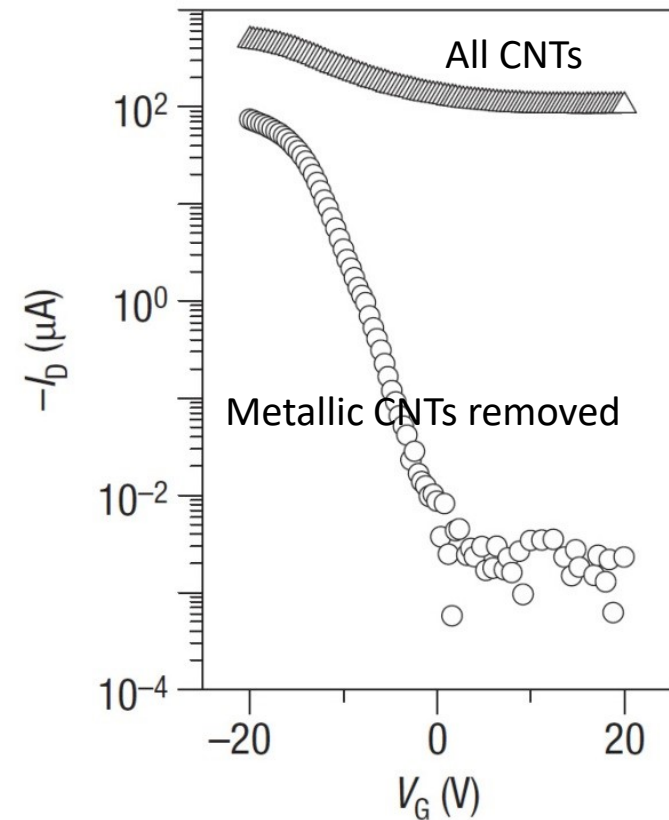
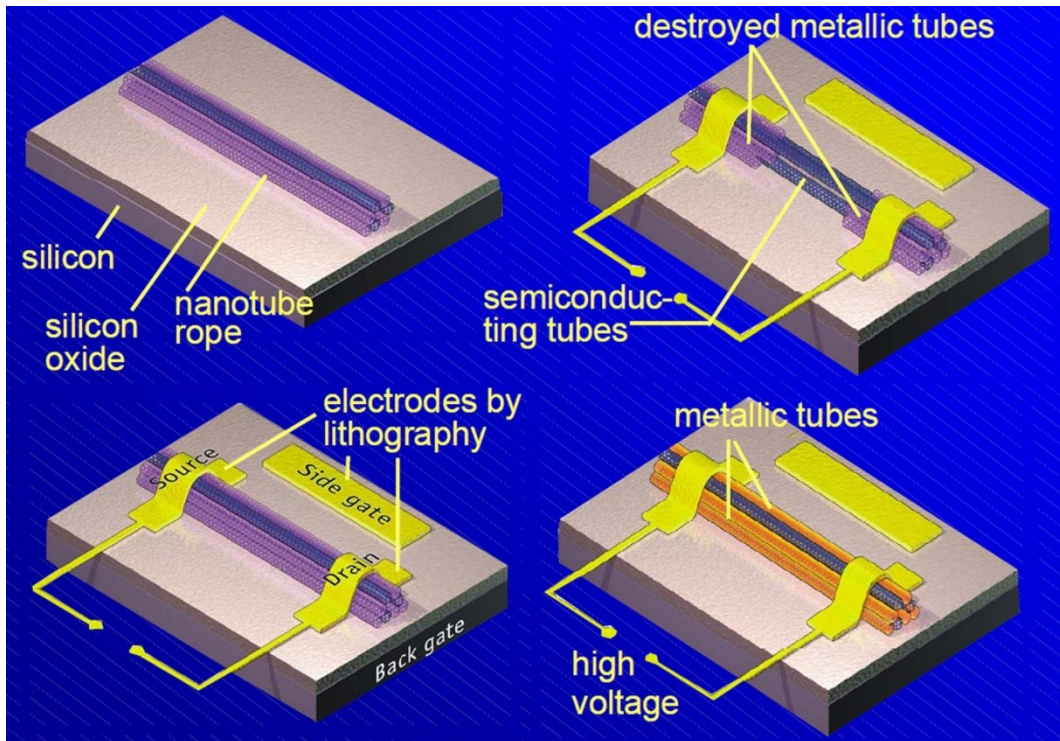
Separation by centrifugation

- Centrifuge CNT suspension at 64000 rpm \rightarrow 200000 g
- CNTs are sorted according to density
- Pick up some part of vial and repeat
- 97% of CNTs are within 0.2 Å of mean diameter



Selective destruction

- Apply gate voltage to switch off semiconducting CNTs
- Apply high S/D voltage
- Metallic CNTs are heated and destroyed
- Difficult for large scale circuits
- May destroy nearby CNTs

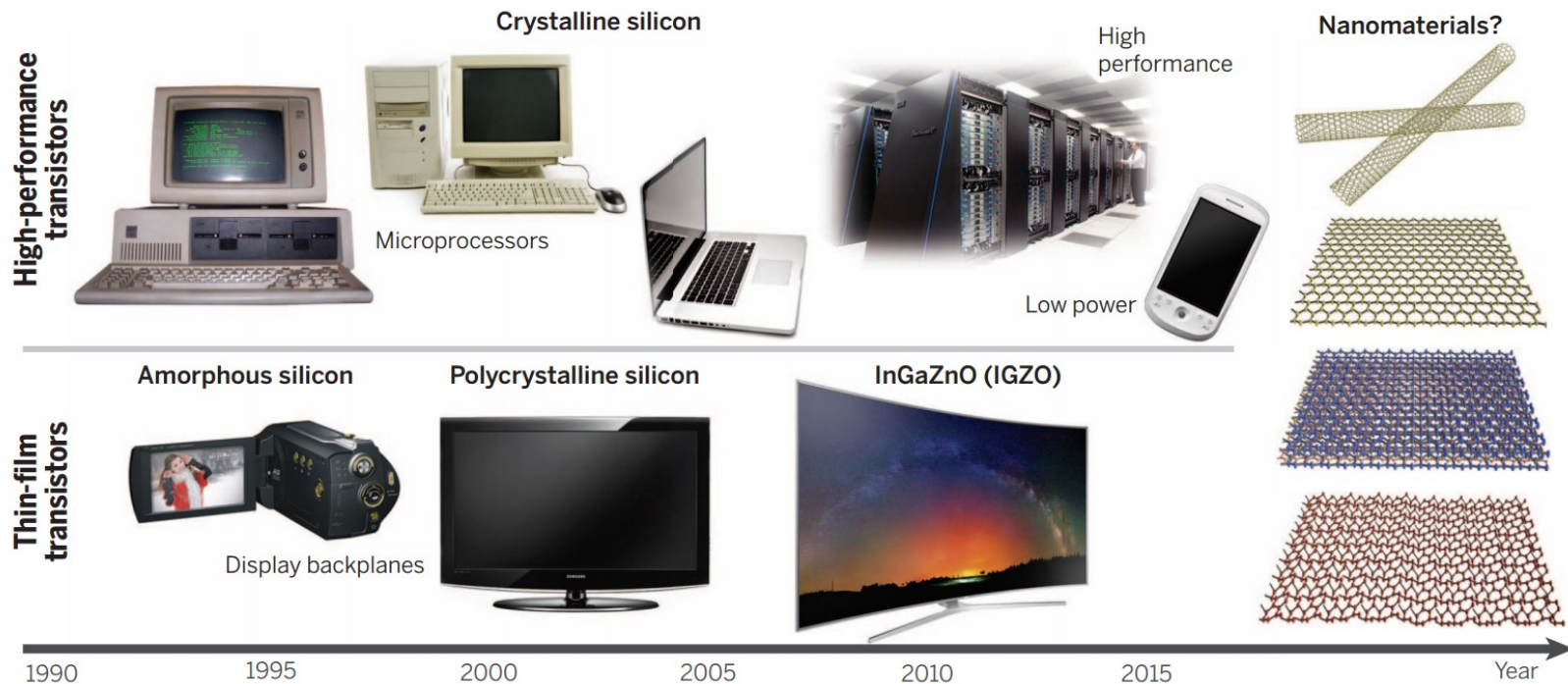


Outline

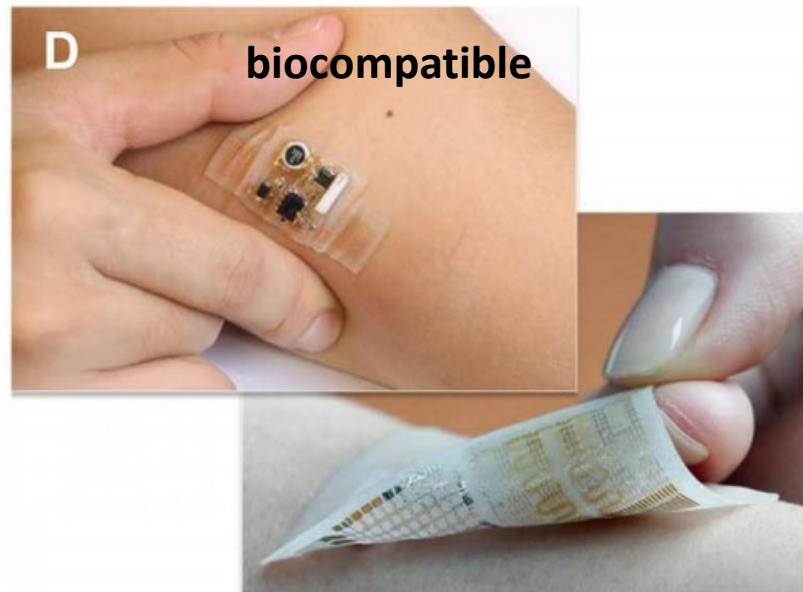
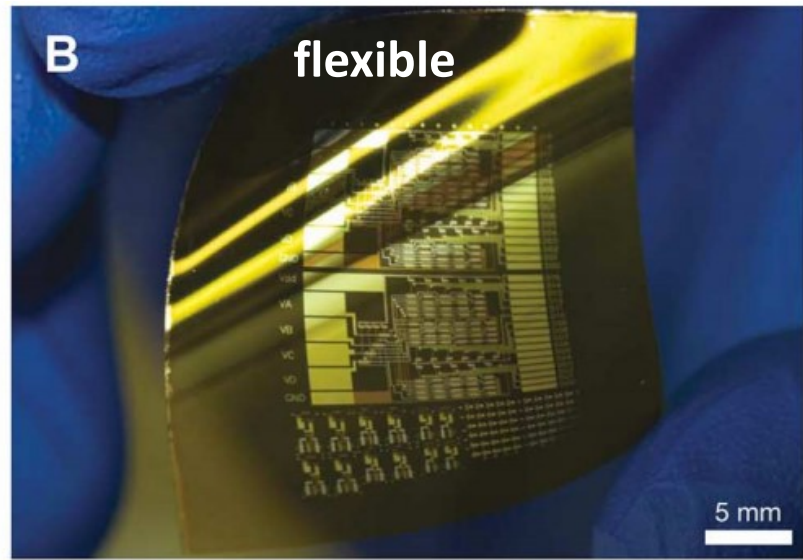
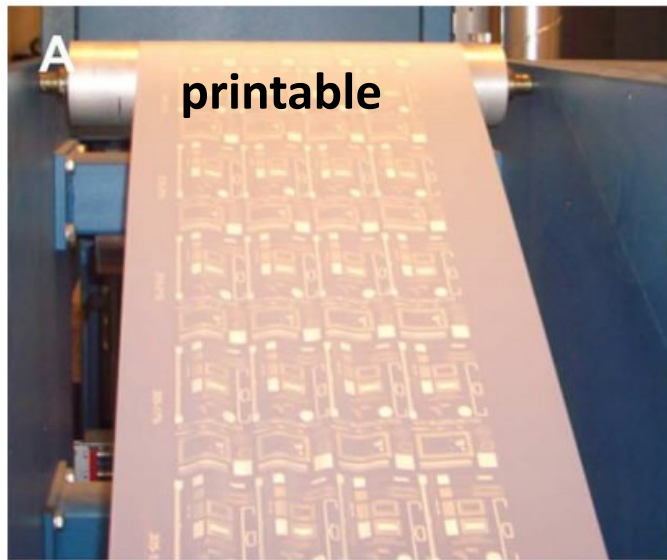
- Basics of graphene and CNTs
 - Structural
 - Electronic
 - Production of CNTs
- Advantages of CNTs for FETs
 - Electrostatics -> length scaling
 - High-k compatibility
 - Band-to-band tunneling
- Challenges of CNT integration
 - Contacts
 - Doping
 - Positioning
 - Chirality control
- Towards integration
 - Flexible electronics
 - High frequency performance

Thin film transistors

- Printed / flexible / transparent / biomedical electronics
- Lower requirements on size and speed
- More sensitive to cost and fabrication complexity
- Amorphous-Si, Poly-Si, InGaZnO, organic molecules

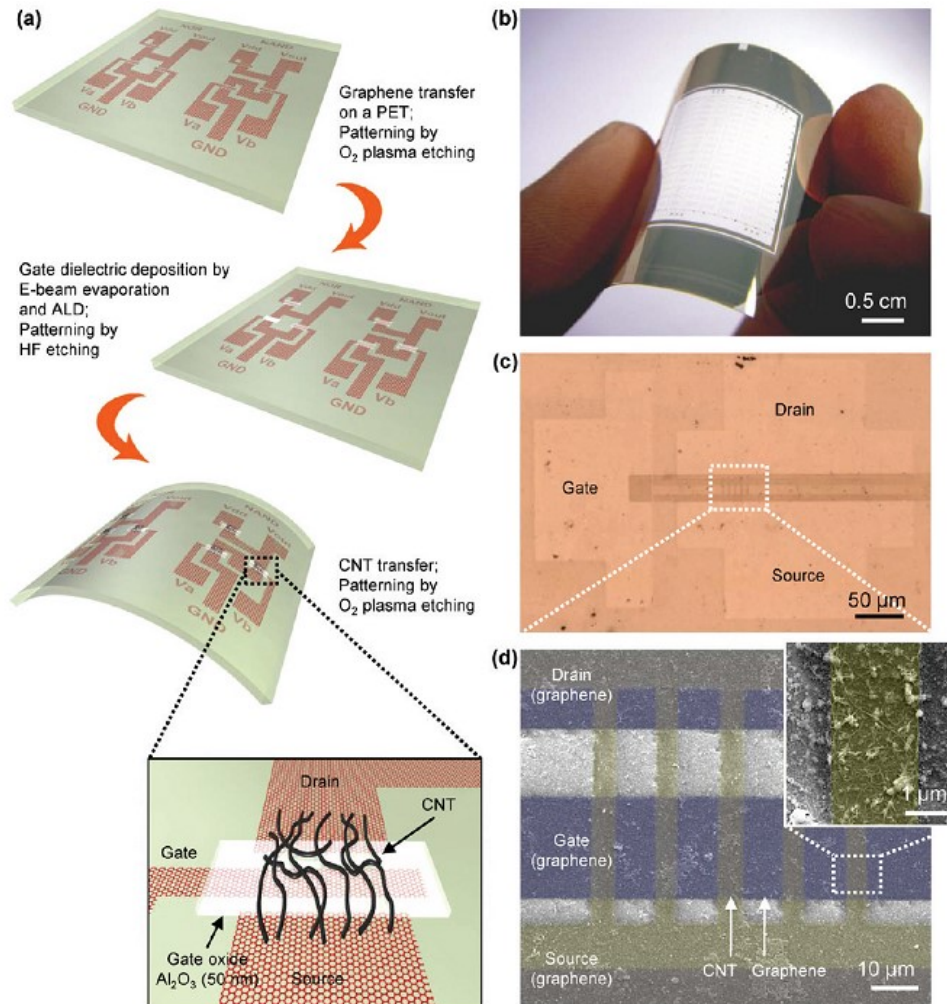
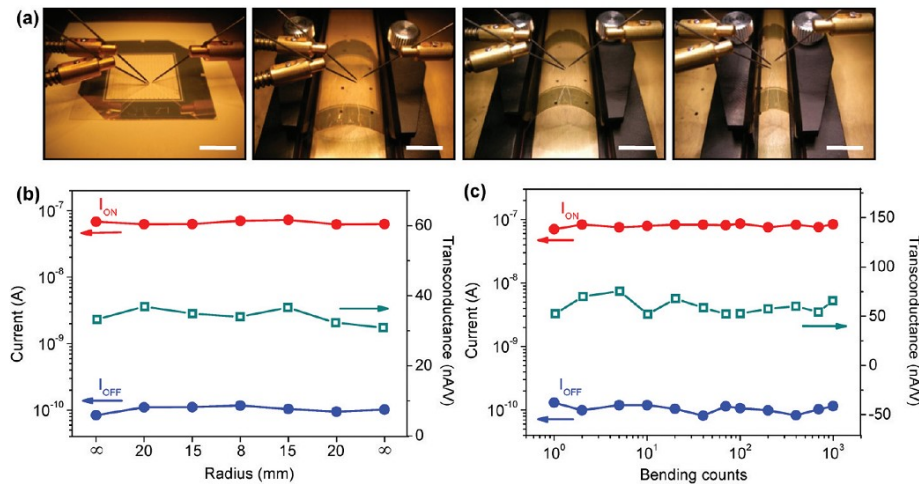


Thin film transistors

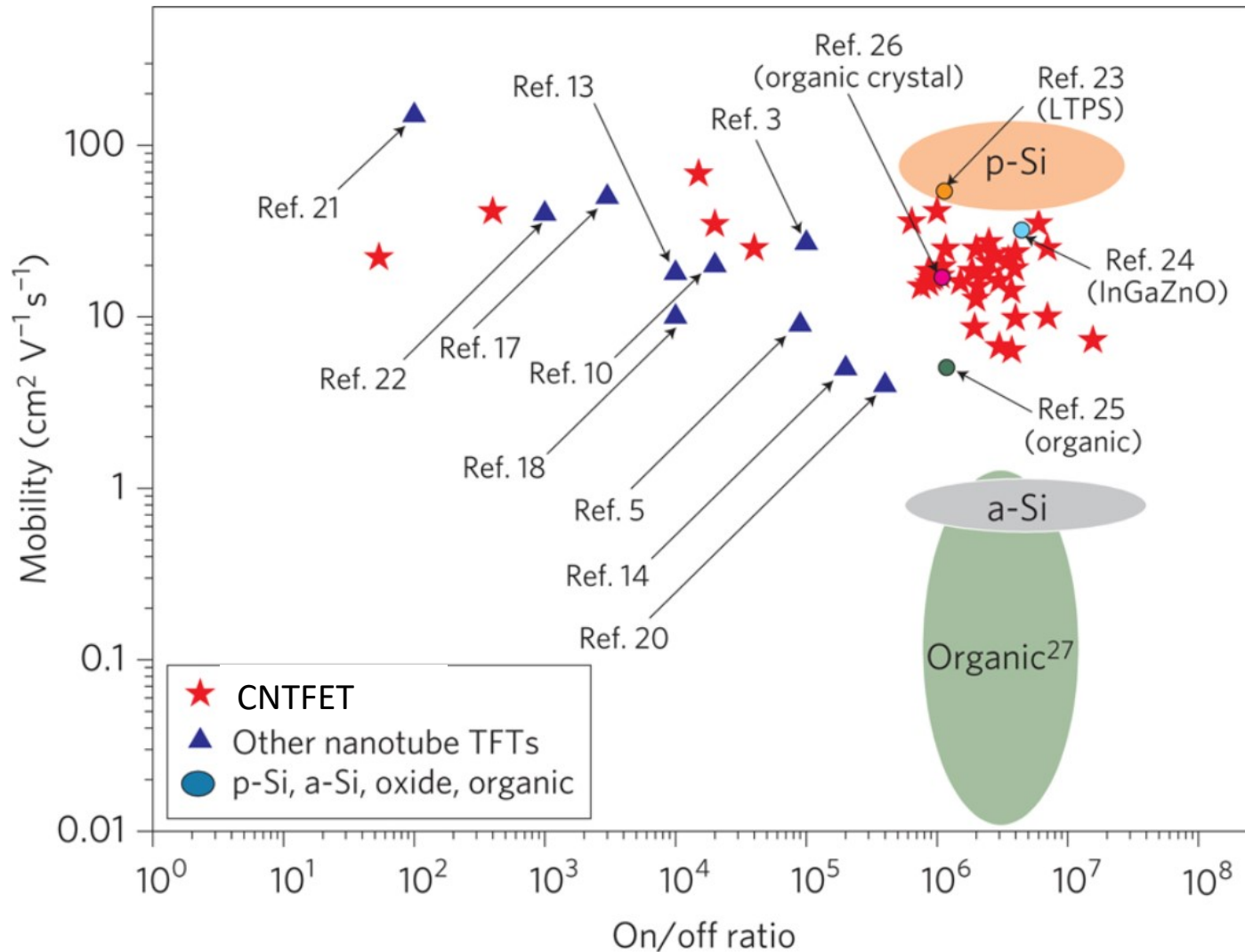


Flexible electronics

- Graphene for electrodes
- CNTs for channel
- No degradation when bent



Thin film transistors comparison



Requirements for RF applications

- Need high g_m and low $g_d \rightarrow$ only semiconducting CNTs
- Minimize parasitic capacitance / CNT \rightarrow dense array of CNTs

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{gs} + C_{p,gs} + C_{p,gd})((R_{p,s} + R_{p,d})g_d + 1) + C_{p,gd}g_m(R_{p,s} + R_{p,d})}$$

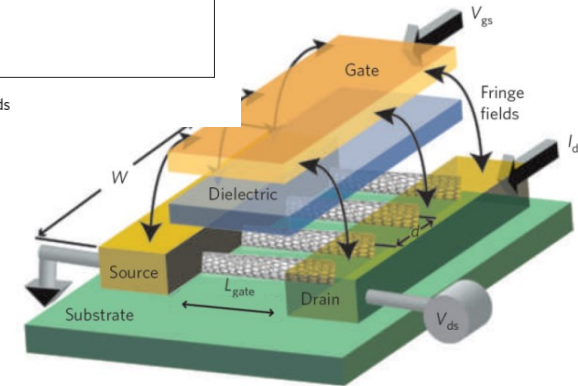
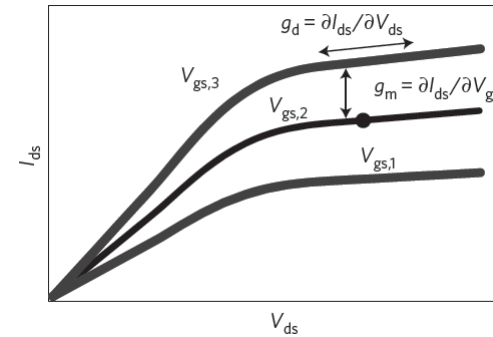
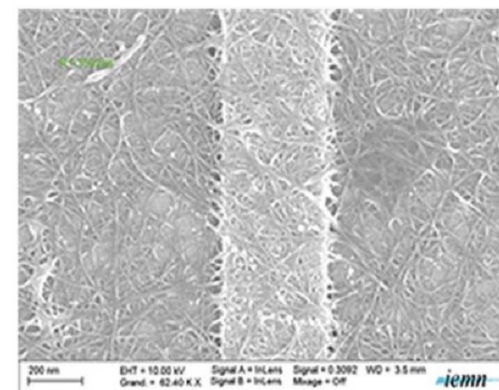
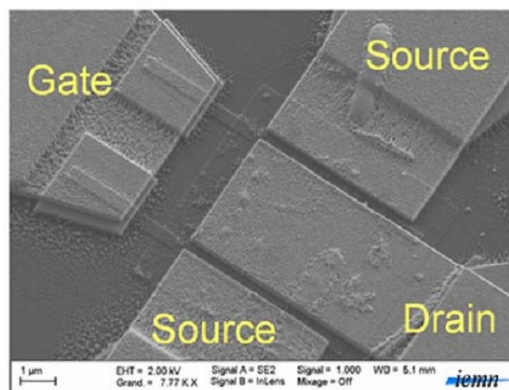
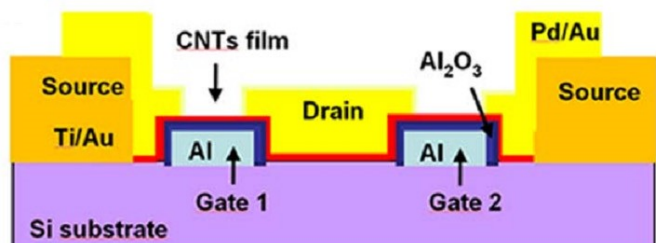
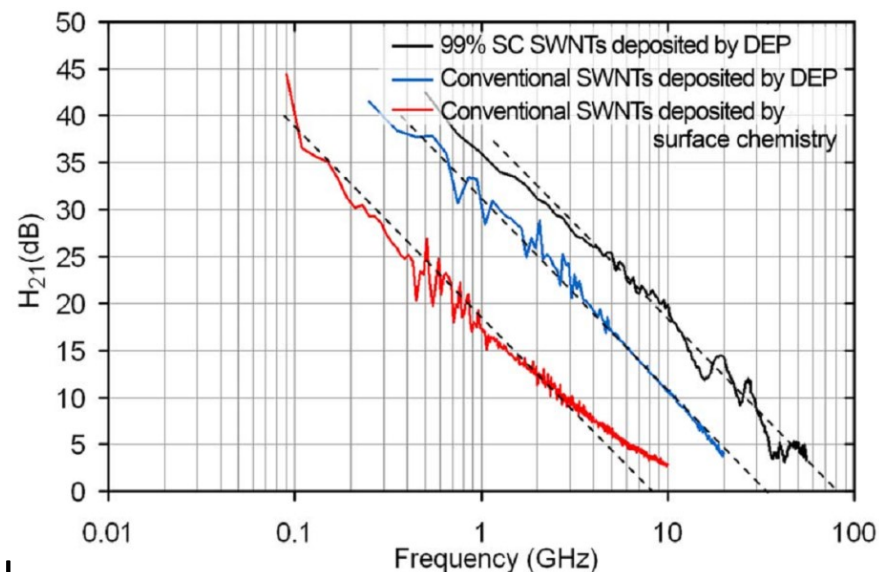


Table 1 | Ideal parameter values for making a high-frequency field-effect transistor from single-walled nanotubes.

Property/parameter	Target value or range	Justification
Diameter	1.5–2.0 nm	Current is largest in this range ^{54–55} .
Chirality	Semiconducting and same (n,m)	To obtain identical transport properties.
Purity	>99% semiconducting nanotubes	No metallic nanotubes for high gain and high f_{max} .
Length	>1 μm	Nanotube length must be longer than the intended channel length.
Density	>10 nanotubes μm^{-1}	Reduces the parasitic capacitance per nanotube; increases current carrying capacity; improves impedance matching.
Alignment	All parallel	Results in higher transconductance and denser nanotube packing.
Uniformity	Wafer scale	Essential for large-scale processing.

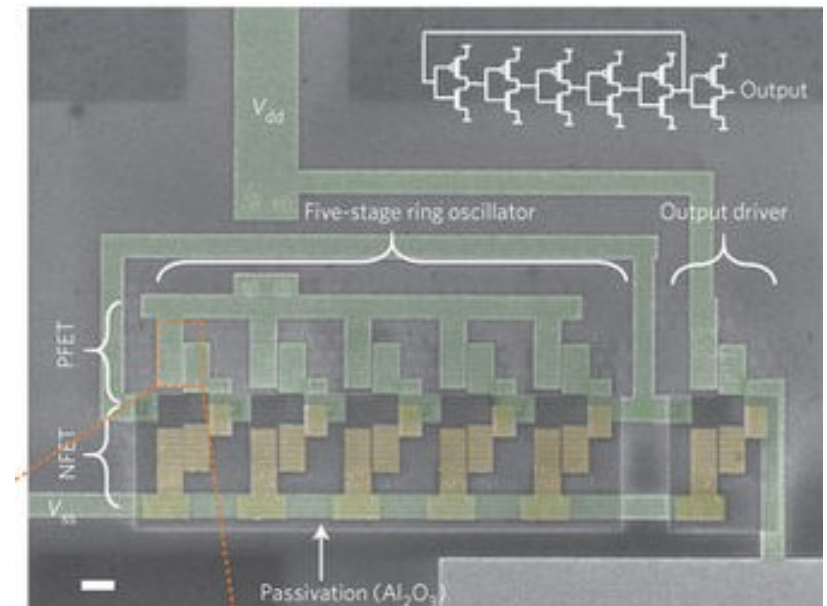
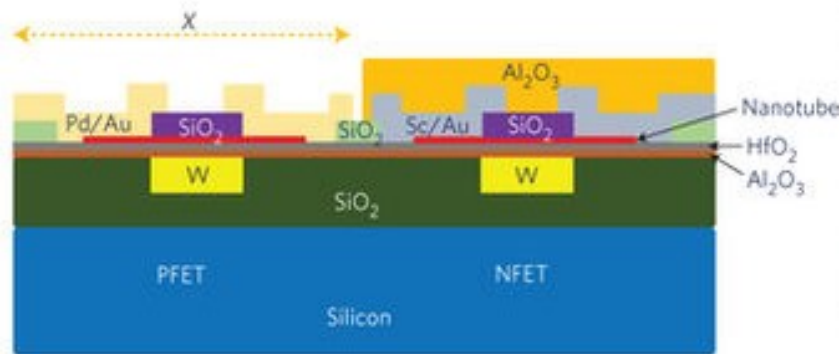
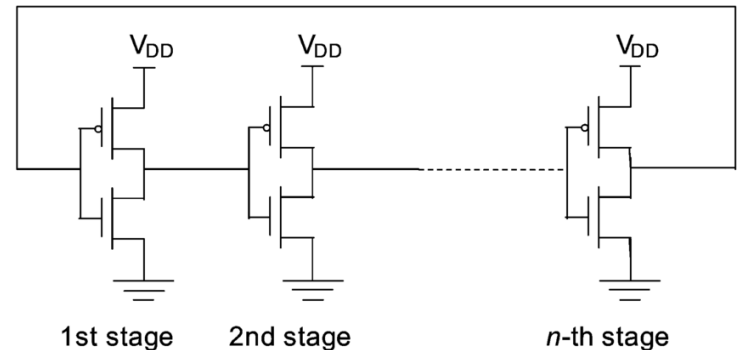
RF performance

- Can not use single CNT due large parasitic capacitance (and impedance mismatch)
- Use semiconducting CNTs separated using centrifugation
- $f_T = 80$ GHz
- Much better than unseparated CNT material



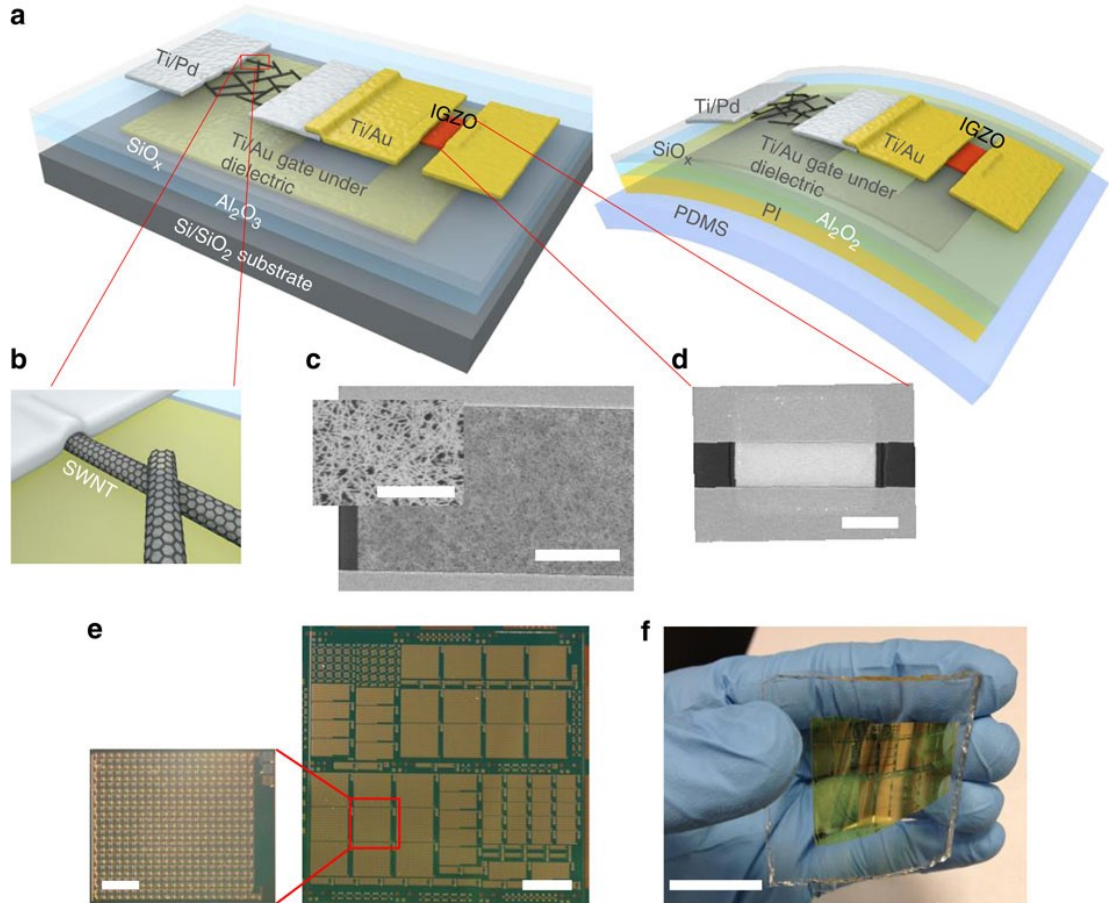
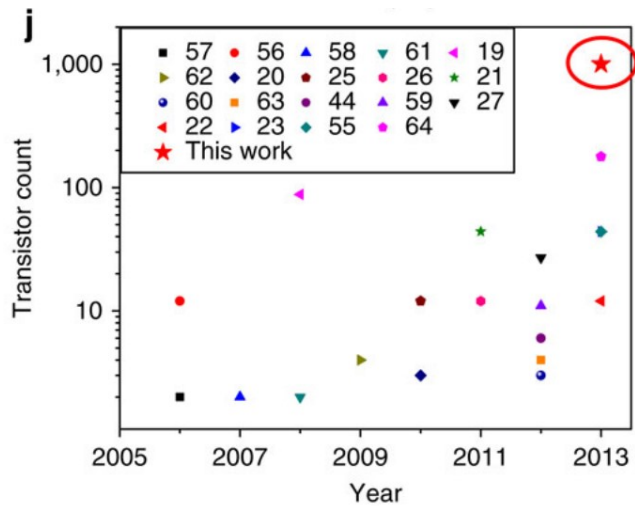
Ring Oscillator

- Odd number of inverters in series, output connected to input.
- Used to measure speed of digital technologies.
- Centrifuged NWs = 99.9% semiconducting
- Switching time = 355 ps /stage (2.8 Ghz)



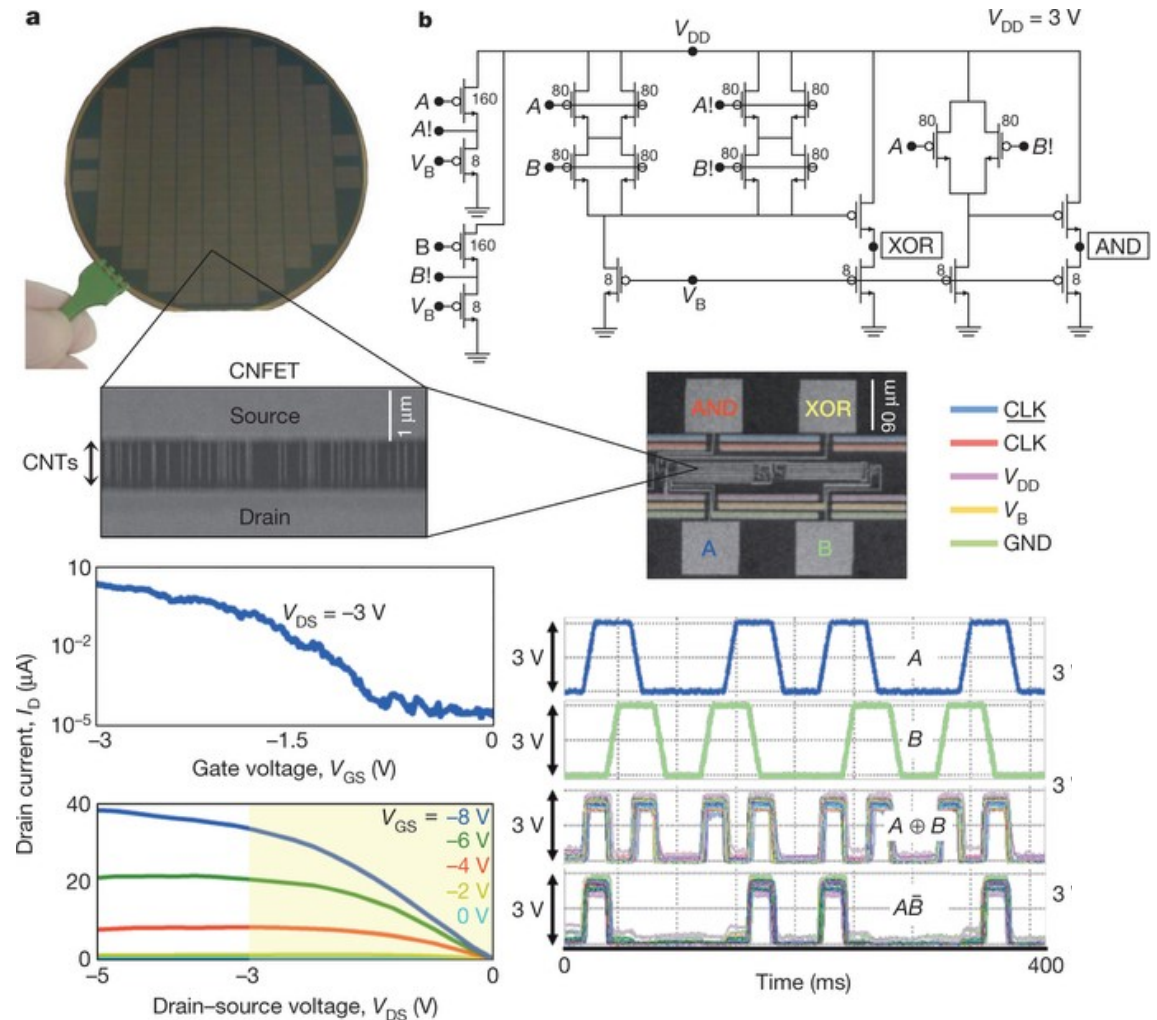
Large scale integration

- p-type CNTFETs (from centrifuged CNTs)
- n-type InGaZnO (sputtered)
- Flexible substrate
- 501 stage ring oscillators
- >1000 transistors



CNT computer

- 178 p-type CNTFETs.
Aligned growth -> transfer
-> burn-off
- Not CMOS, only p-type.
- Counting and number sorting.
- 1980's level.



Summary

- **Individual CNTs have great electronic properties**
 - High mobility
 - Coaxial gate + thin gives good electrostatics -> scaling
 - Compatible with high-k dielectrics
 - No surface scattering
- **CNTs are difficult to integrate in large scale circuits**
 - Schottky barriers at contacts
 - Unstable doping
 - Poor position control
 - Semiconducting / metallic mix

