Integration of III-V semiconductors with Si

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On the agenda

NANO ELECTRONICS GROUP

Part 1:

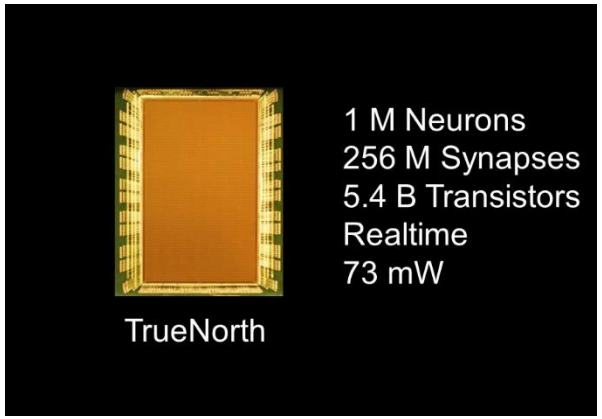
- Why go for III-Vs?
- Challenges of integration
- Integration techniques
  - Buffer layer epitaxy
  - ELO

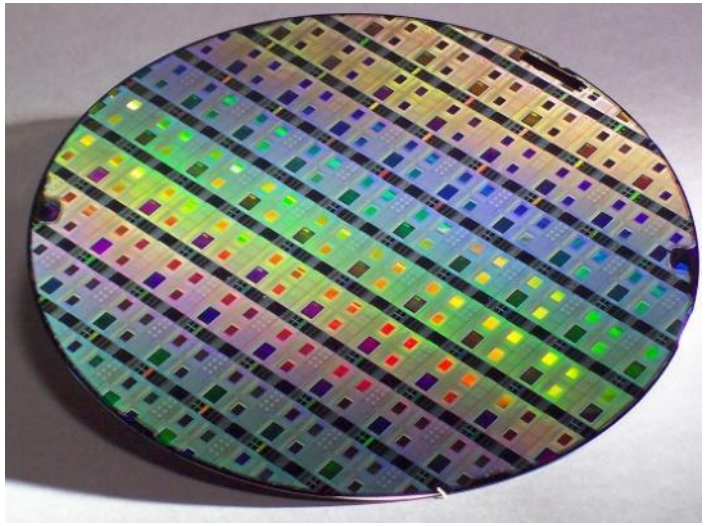
Part 2:

- ART
- Nanowire epitaxy
- TASE
- RME

Si integrated circuits

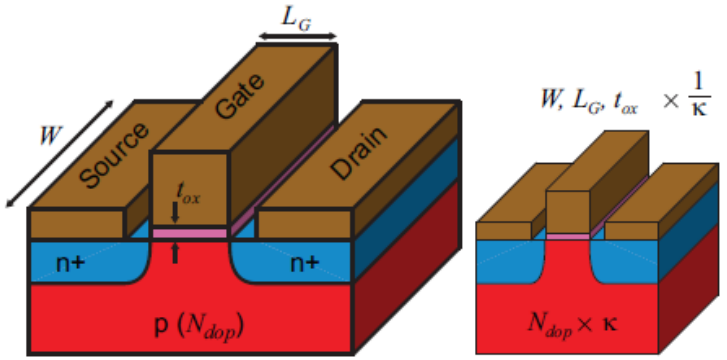
- Si electronics for 50+ years!
  → Established, inexpensive, versatile
- Billions of transistors/chip (all ”identical”!)
- Si CMOS → Greatest engineering feat of mankind

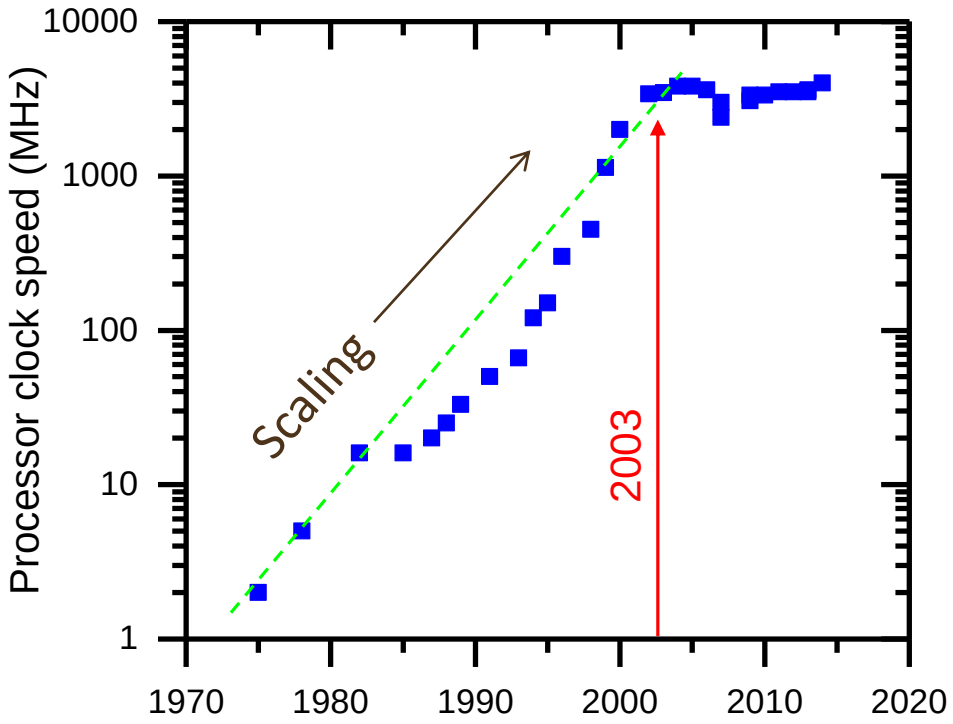


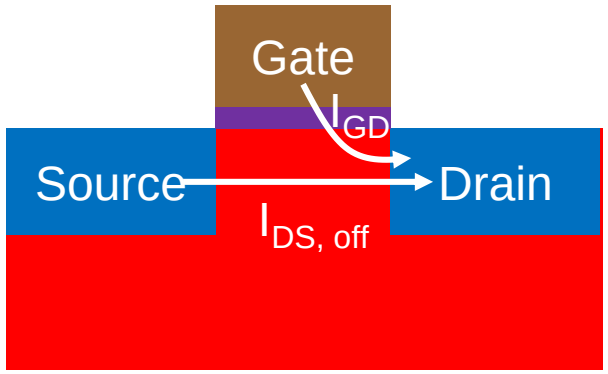


End of the Si roadmap

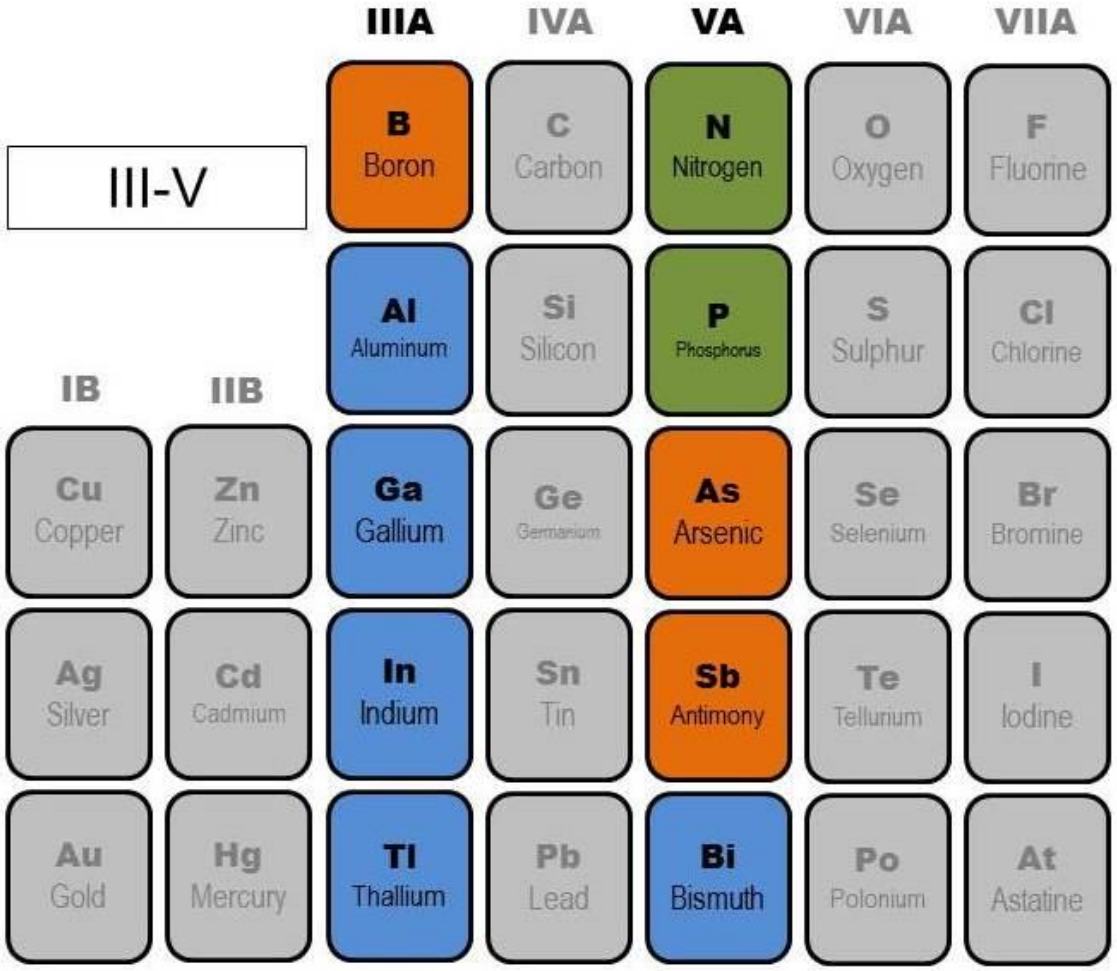
- Power leakage is the problem
  - Leakage through gate dielectric, I_{GD} (dynamic)
  - Leakage in off-state, $I_{DS,off}$ (static)
  - Core clock speed increase stalls







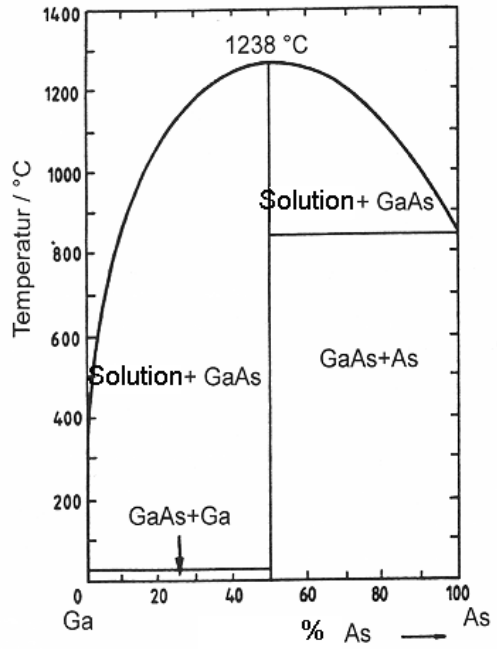
III-V semiconductors



Larger band gap

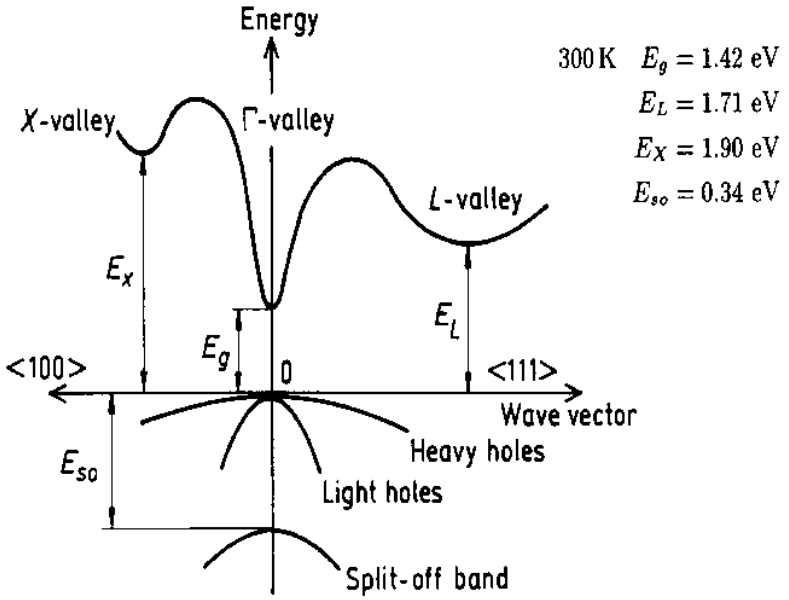
BN	(BP)	(BAs)	(BSb)	(BBi)
AlN	AlP	AlAs	AlSb	(AlBi)
GaN	GaP	GaAs	GaSb	(GaBi)
InN	InP	InAs	InSb	(InBi)
(TlN)	(TlP)	(TlAs)	(TlSb)	(TlBi)

Larger band gap ⟷ Smaller m*

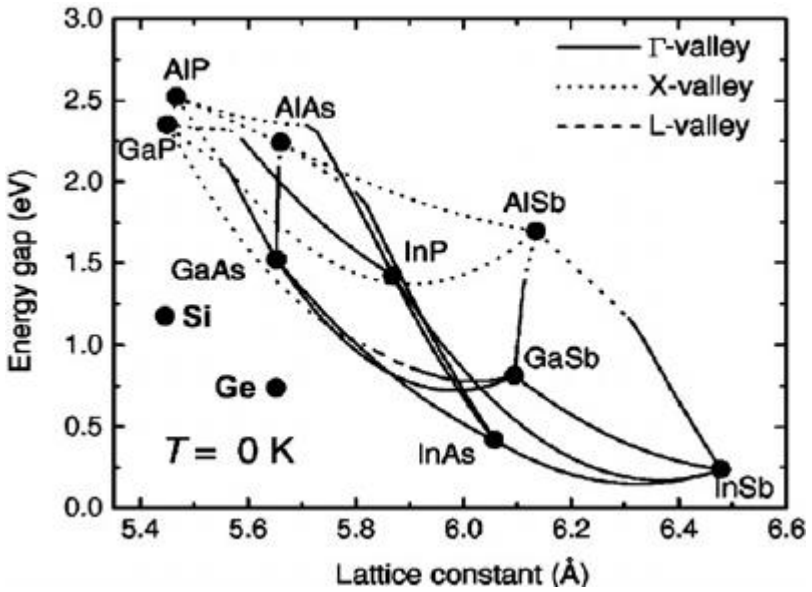


Exact binary composition!

So why III-V's?

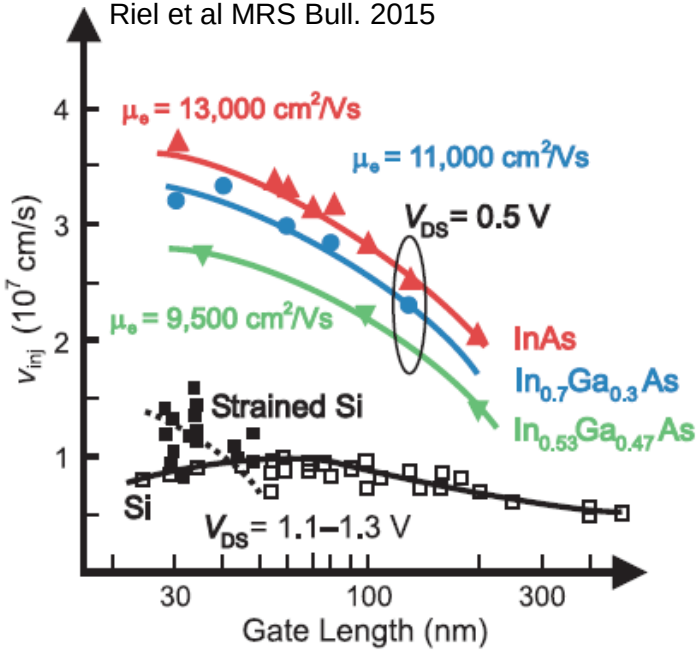


Direct band gaps



Ternary compounds

Riel et al MRS Bull. 2015



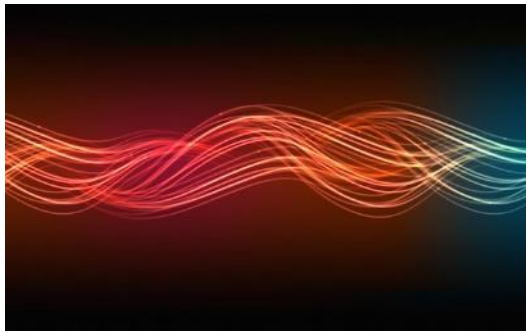
High electron mobility

So why III-V's?

- Can extend application space
- But for feasibility ($$) needs integration with Si

Optoelectronics

- LEDs
- Lasers
- IR Photodetectors



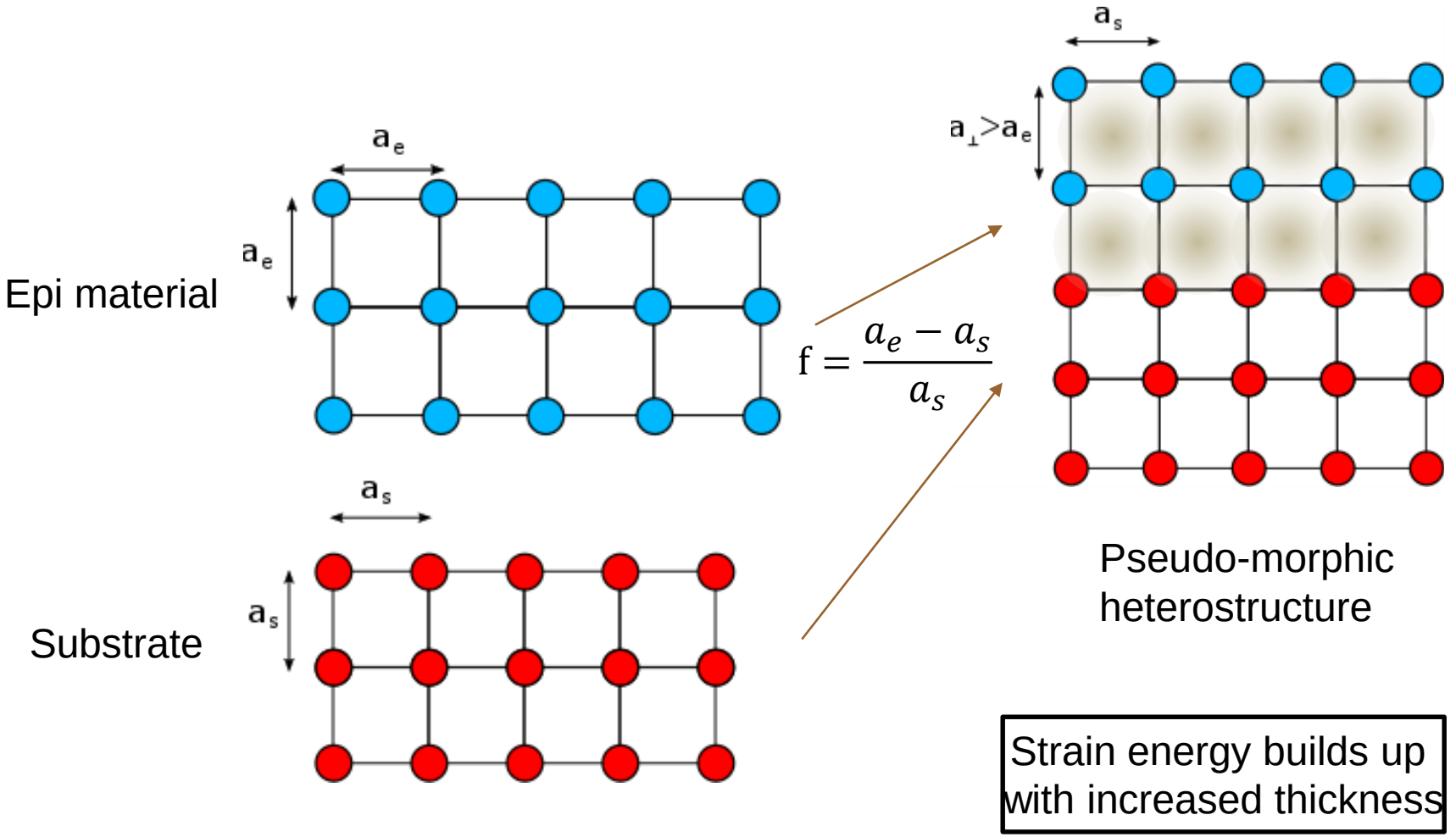
Communication and Power

- mmWave devices (> 60 GHz)
- RF Power amplifiers
- Power switches

Quantum computing

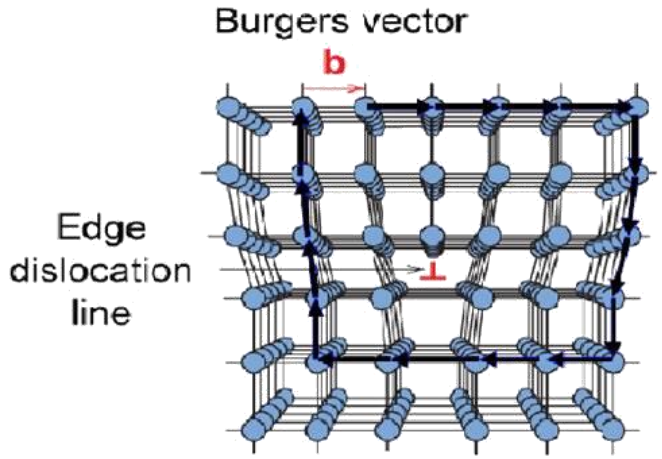
- Majorana fermions
- Topological interfaces

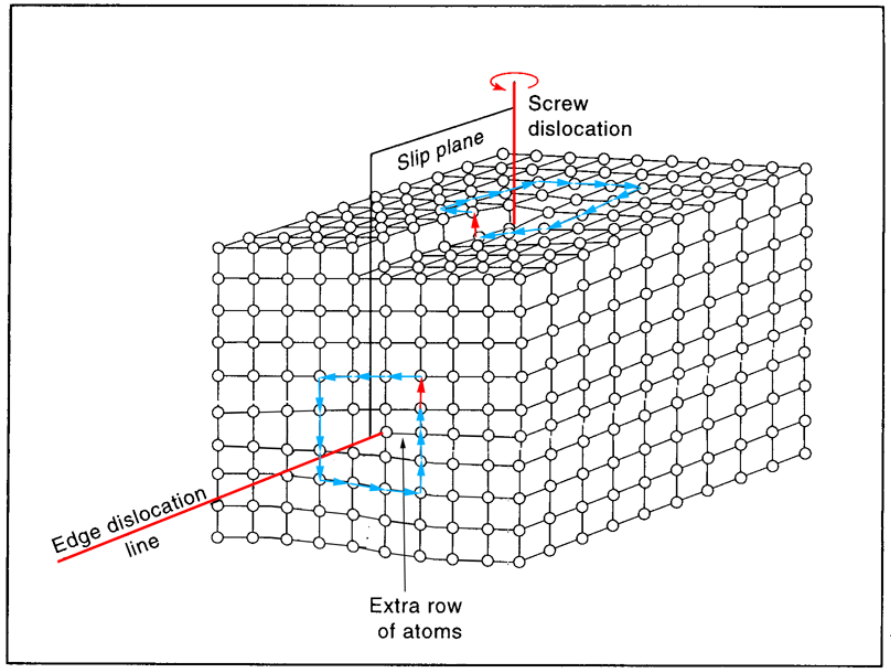
Challenges of integration - *Lattice-mismatch*



Two types of line dislocations

- Burgers vector direction tells type of defect:
- Edge dislocations
  - Extra/missing row of atoms parallel to the dislocation
  - Burgers vector perpendicular to line
- Screw dislocation
  - Atomic planes is screwed around the dislocation
  - Burgers vector parallel to line





How thick can you grow?

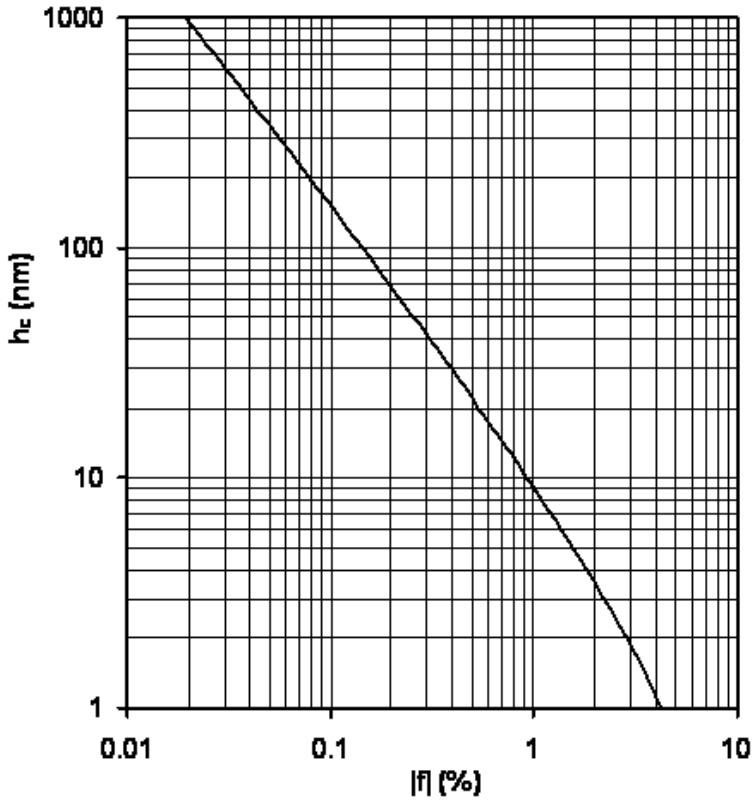
$h = layer\ thickness$

- $E_{strain} \propto h$
- Not stable when E_{strain} > critical thickness, h_c

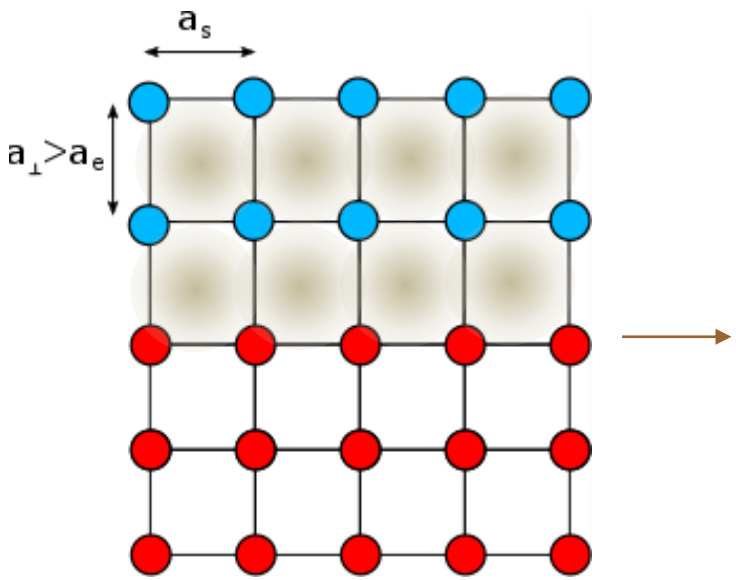
$$h_c \simeq \left(\frac{1-\nu}{1+\nu}\right)\left(\frac{1}{16\pi\sqrt{2}}\right)\left(\frac{b^2}{a(x)}\right)\left(\frac{1}{\epsilon_0^2}\right)\ln\left(\frac{h_c}{b}\right)$$

Matthews-Blakeslee model

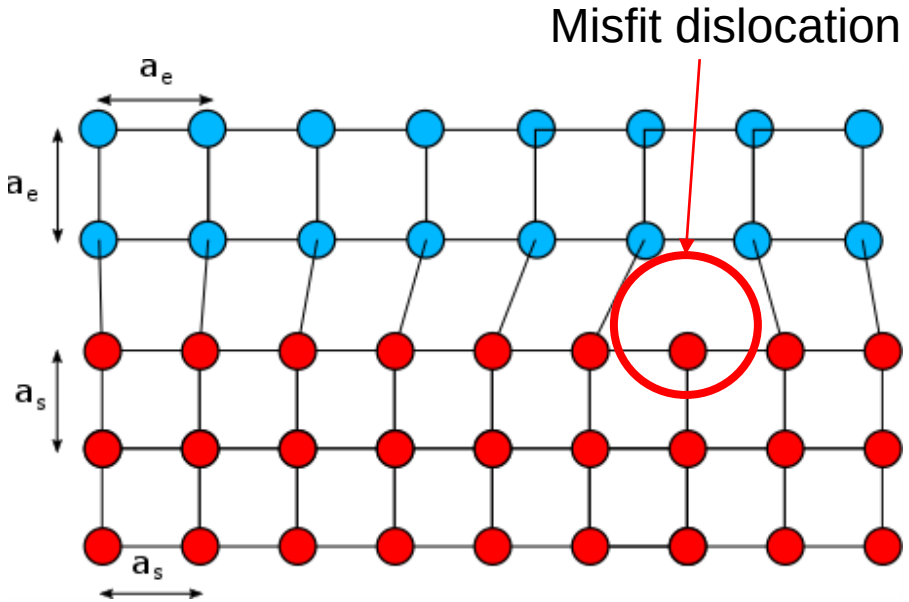
v = Poisson ratio
ϵ_0 = lattice mismatch
b = slip distance (Burgers vector)
a = bulk lattice constant of film



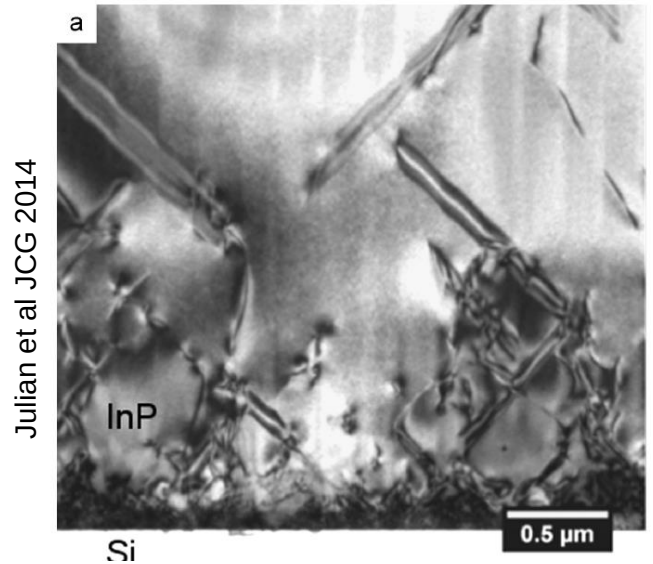
Strain relaxation

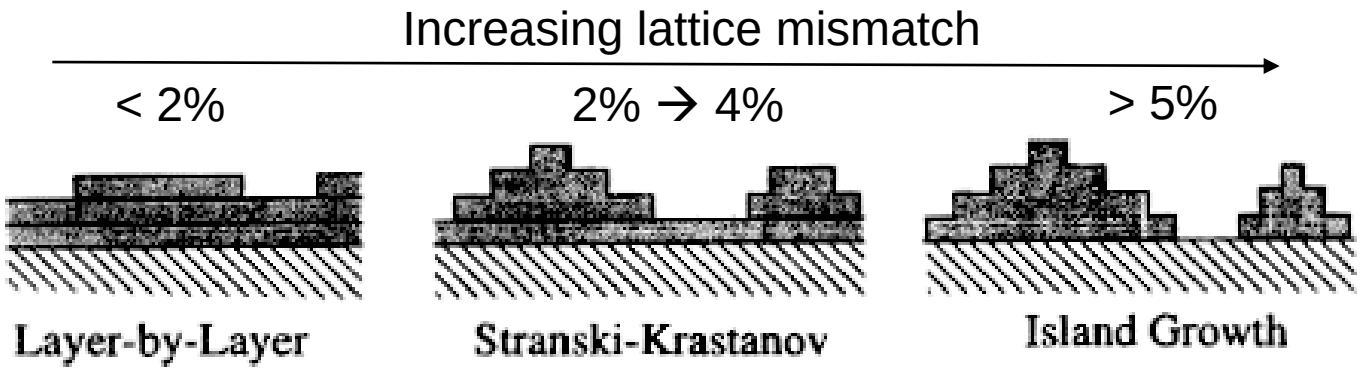


Pseudo-morphic heterostructure

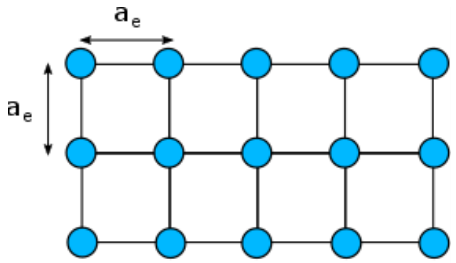


Relaxed heterostructre

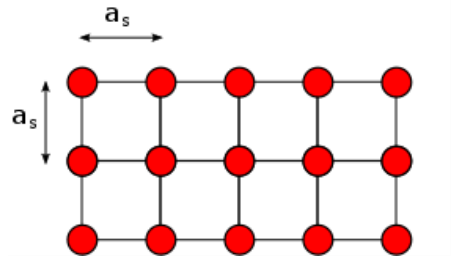




Example – InAs on Si



InAs
a_e = 6.058 Å



Si
a_s = 5.431 Å

$$f = \frac{a_e - a_s}{a_s}$$

1. How large is the lattice mismatch (f)?
2. What is the critical thickness?
3. What growth mode to expect?

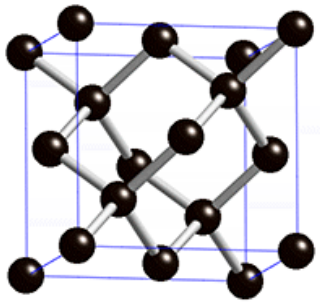
Answers:

1. **11.5%**
2. **Basically zero**
3. **Island growth**

→ InAs integration on Si seems quite hopeless

Challenges of integration - *Crystal structure*

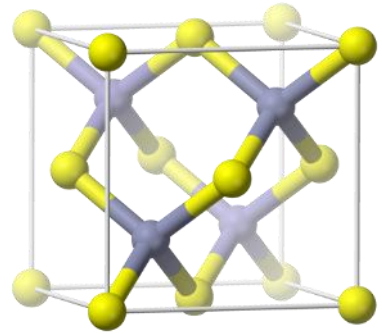
Si



Diamond structure

Two interlaced face-centered cubic (fcc) lattices
The second lattice is translated a/4*(1,1,1)

III-V

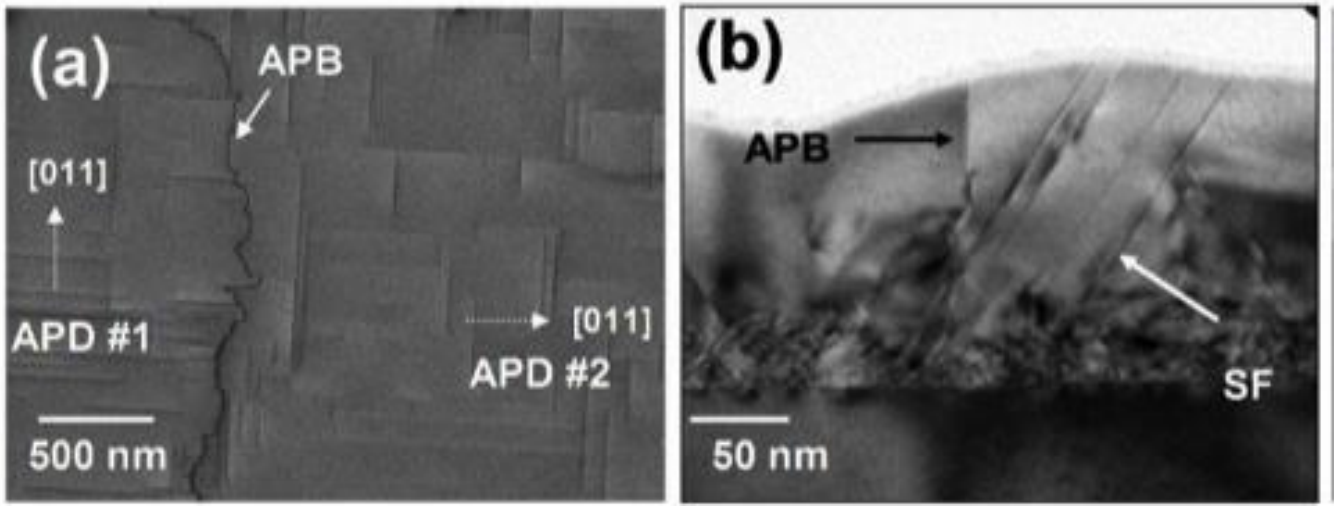


Zinc-blende structure

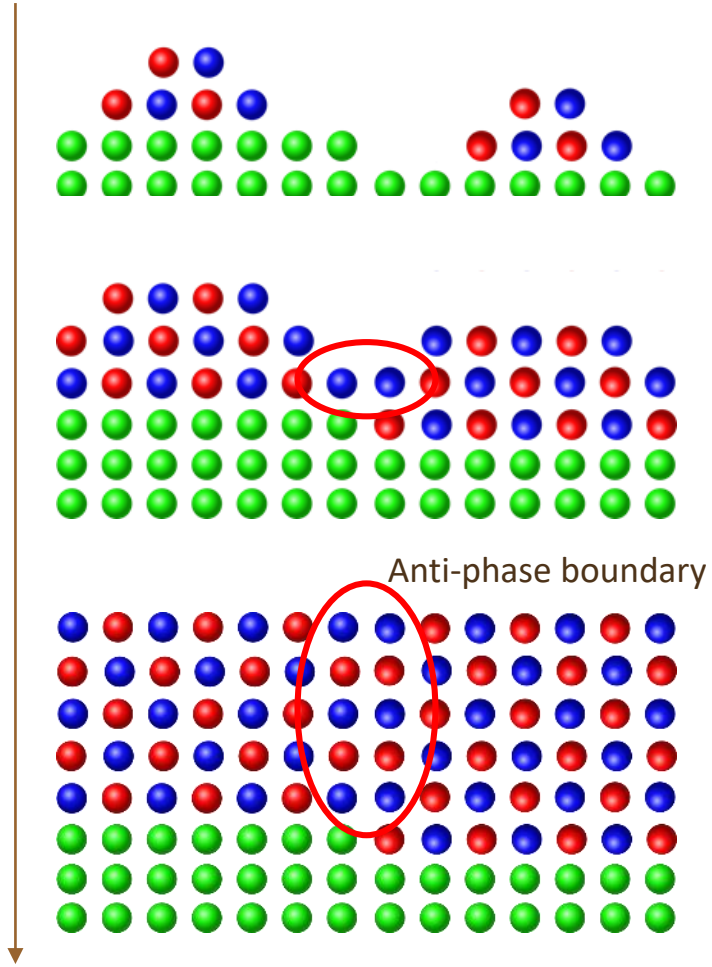
Same structure as diamond
but **one fcc lattice has group III**
and **the second one has group V species**

Anti-phase boundary defects

- Very detrimental defect due to highly polarised defect states.



Michaud, Portail, Alquier ”Advanced Silicon Carbide Devices and Processing”, Chapter 2 (2015)

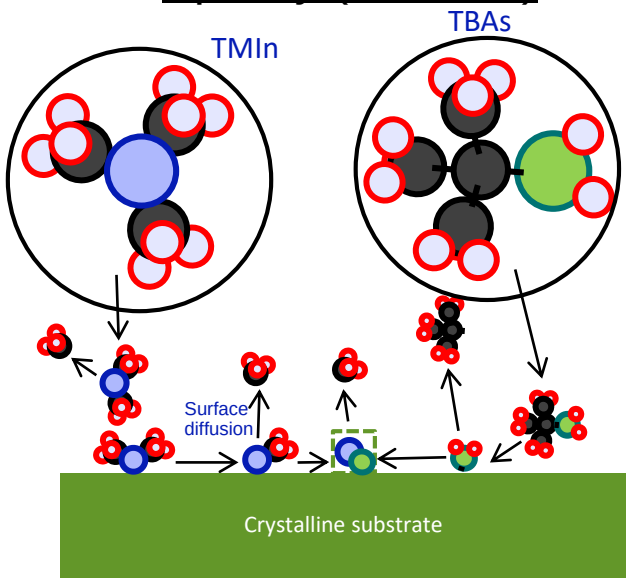


Integration strategies

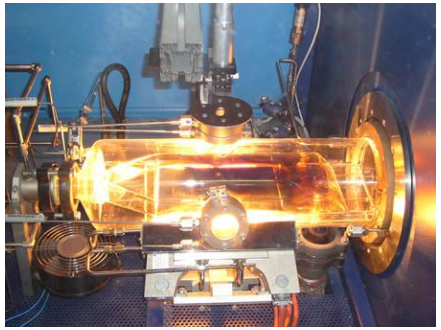
Goal:

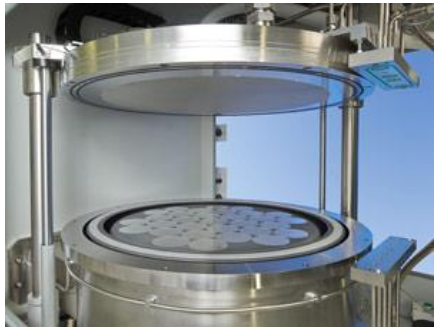
- Maximize quality
- Minimize cost

Epitaxy (MOVPE)

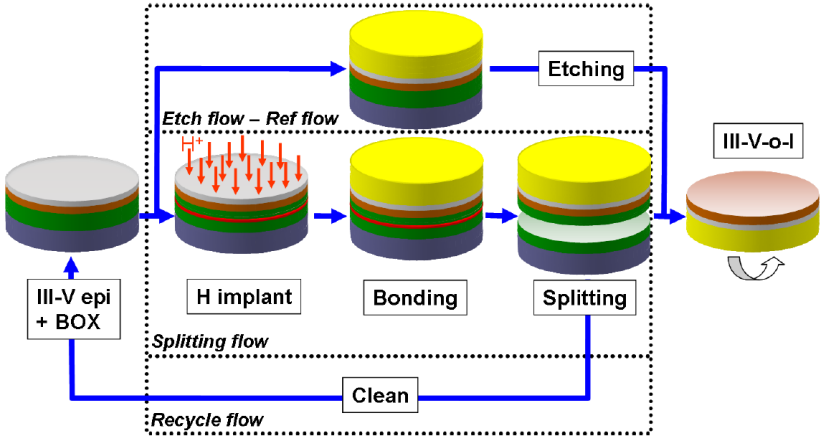


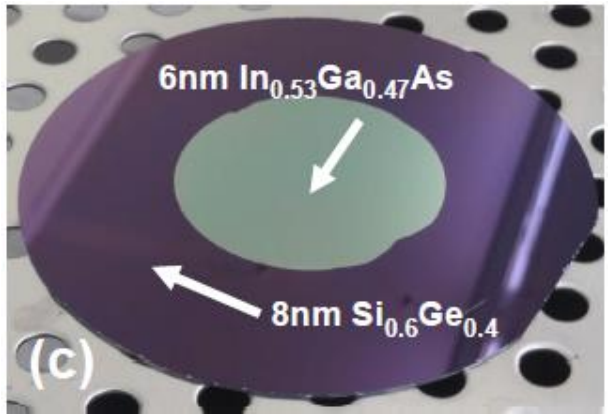
Typical Temperature: 500-800ºC





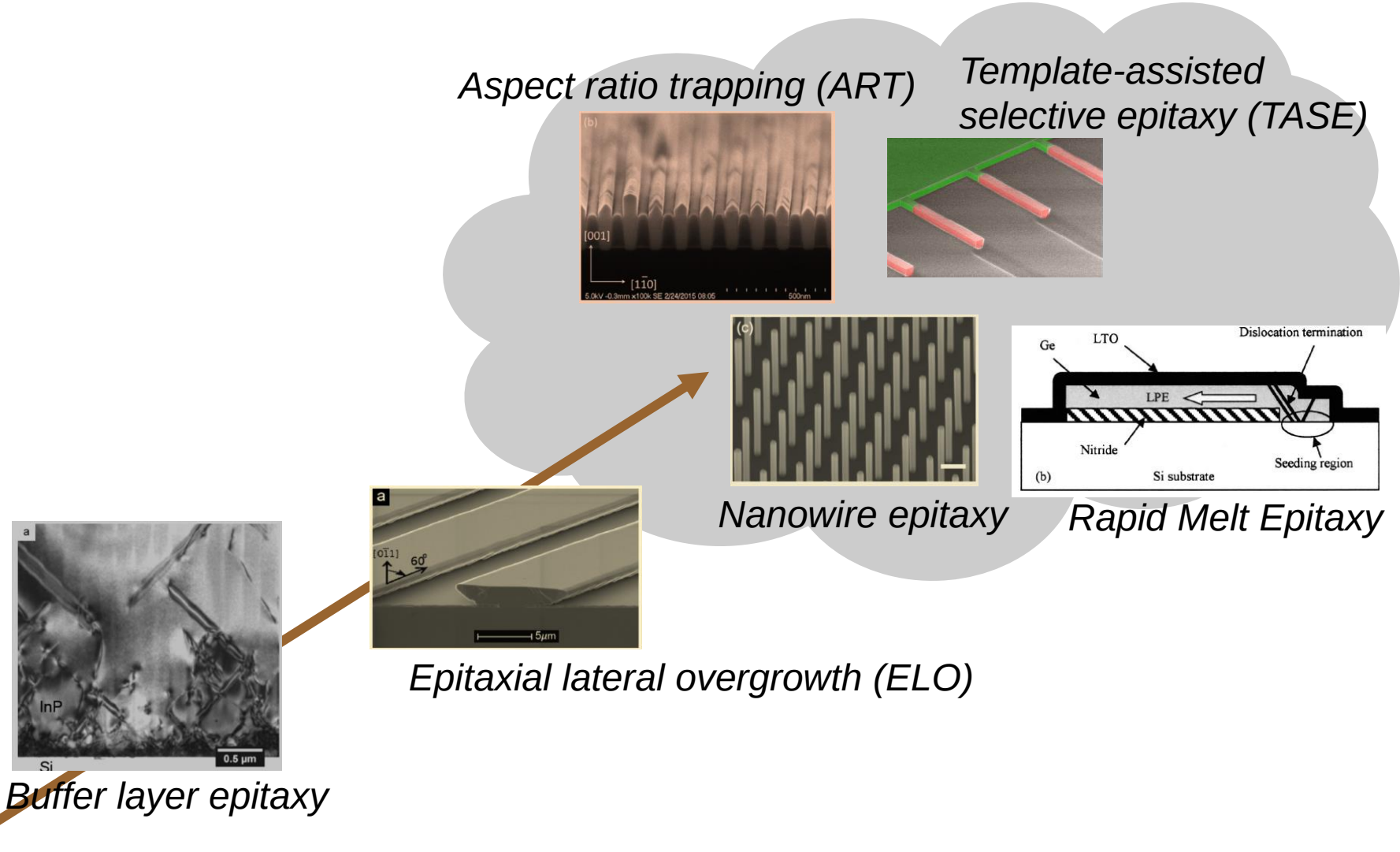
Wafer bonding





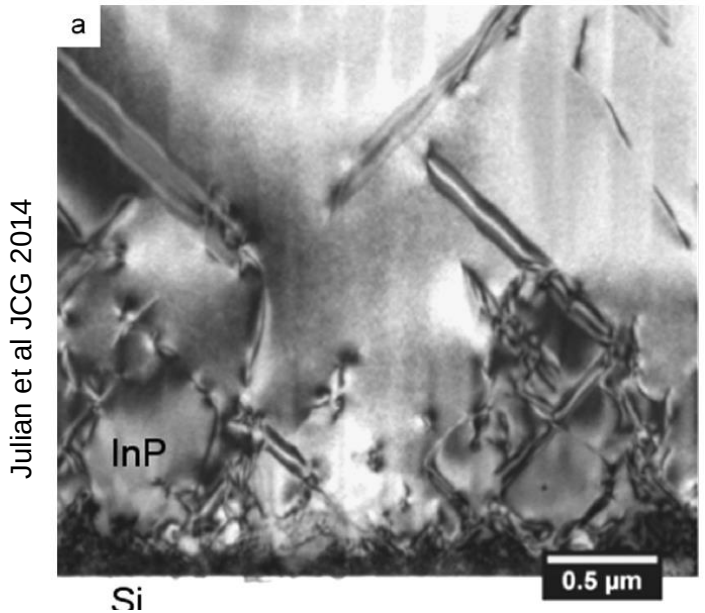
Czornomaz et al. IEDM 201

Epitaxial integration methods

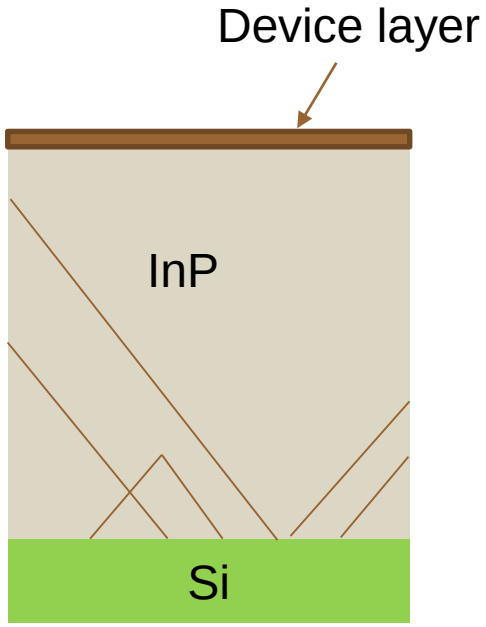


Buffer layer epitaxy

- Idea: Reduction of defects in top layer by containing defects in a thick ”buffer” layer.
- Why? Dislocations can terminate when merging



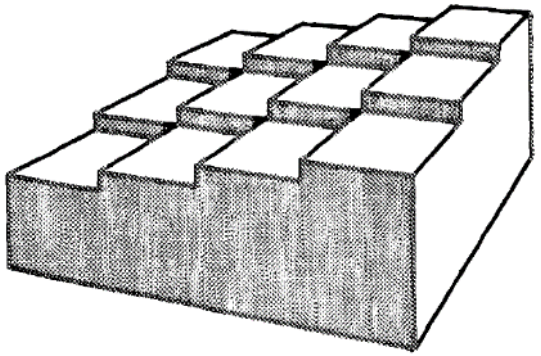
Julian et al JCG 2014



Strategies to limit defect propagation

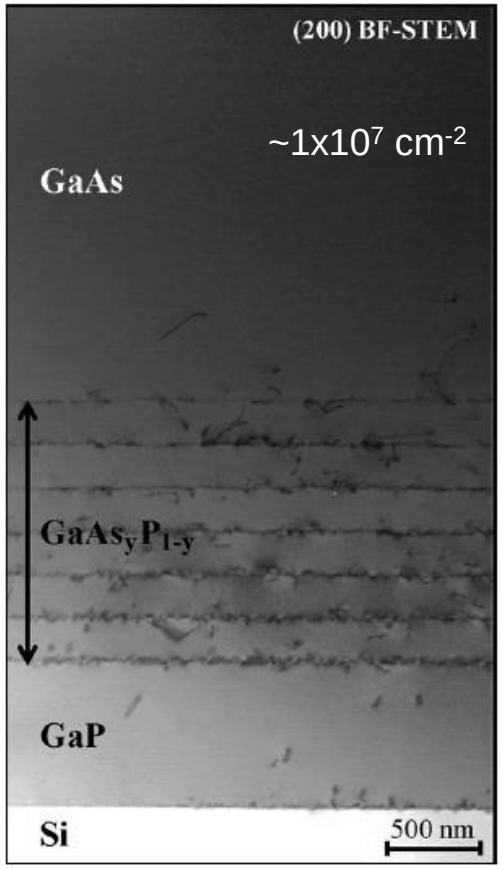
Off-cut substrates

Maximizes nucleation density



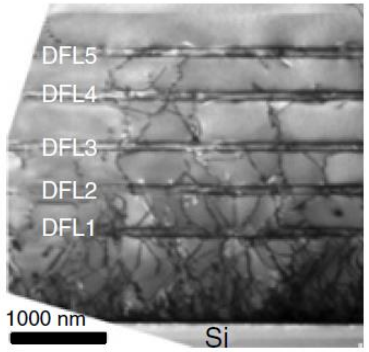
Fischer et al. JAP 1986

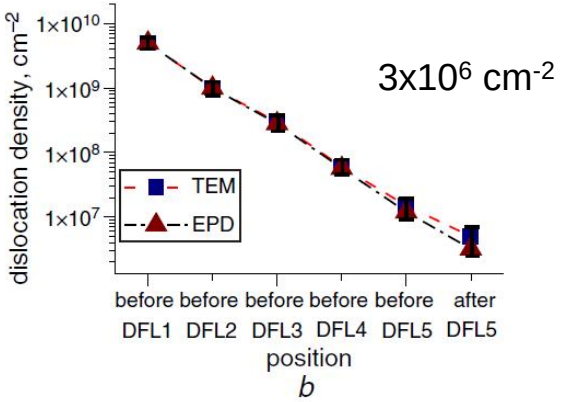
Graded buffers

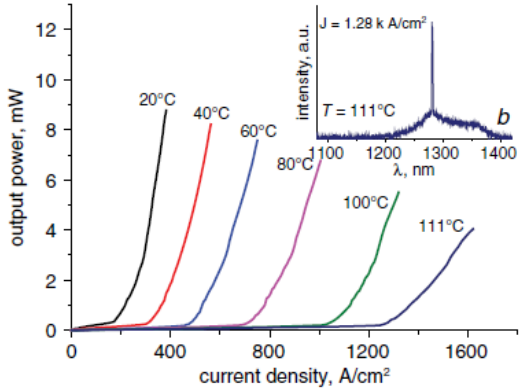


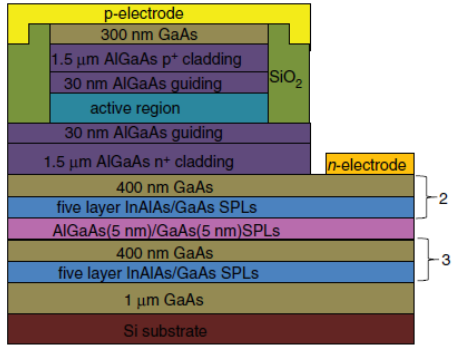
Grassman et al. TED 2010

Superlattices





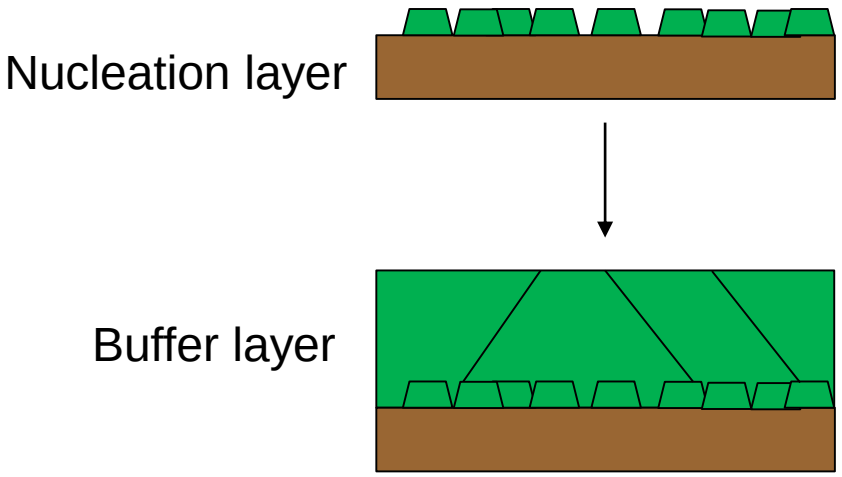




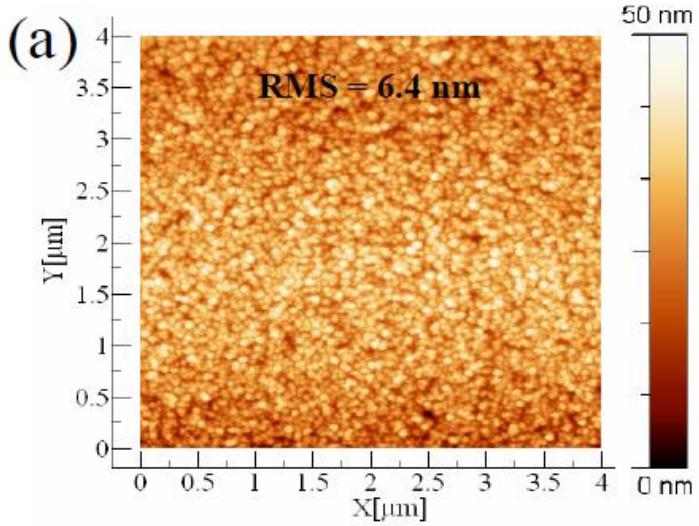
Chen et al. IEEE Electron Lett. 2004

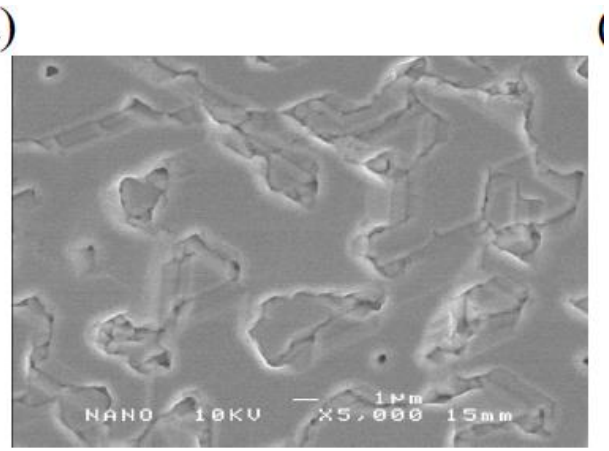
Two-step buffer

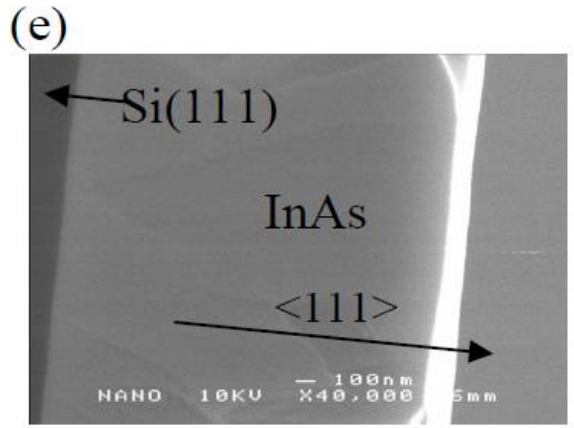
- **Nucleation step:** low temperature, high growth rate
  → Creates dense network of dislocated islands
- **Buffer step:** standard growth conditions to merge film



InAs on Si(111), nucleation @ 350 °C

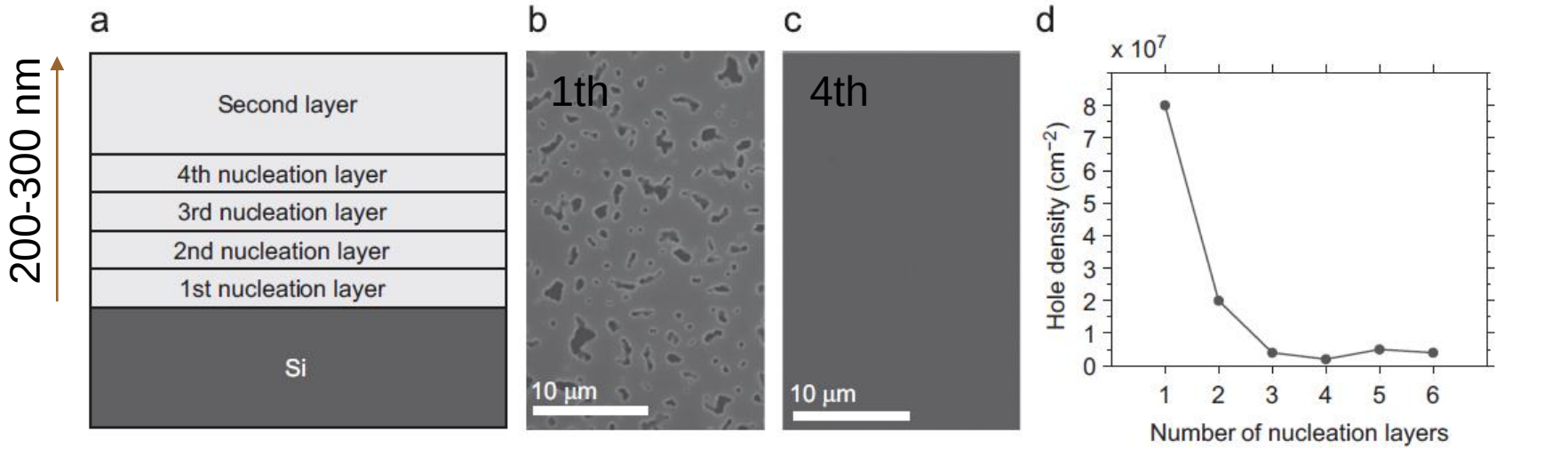


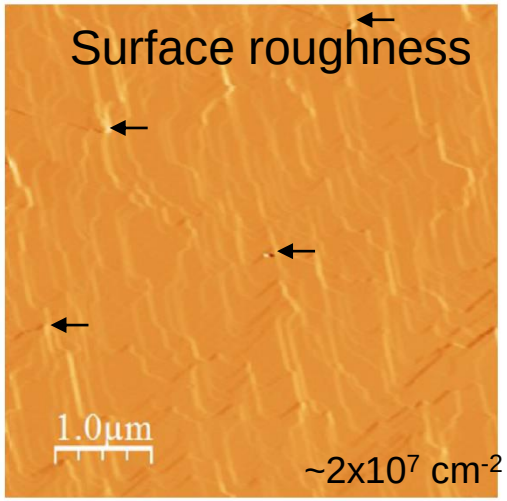




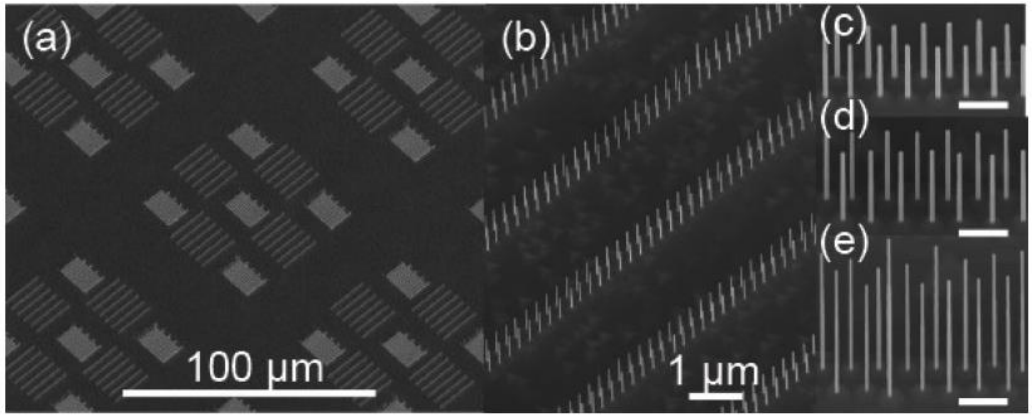
Multiple nucleation steps

Ghalamestani et al. JCG 2011



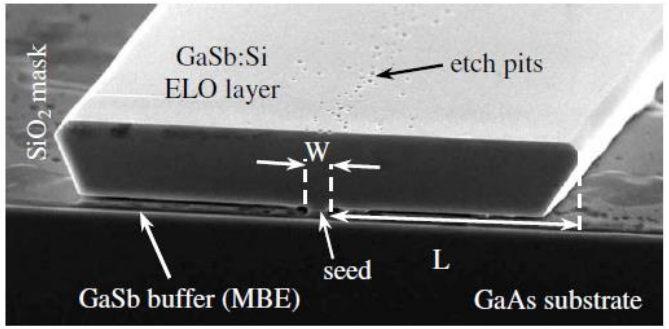


InAs nanowires grown on the InAs buffer

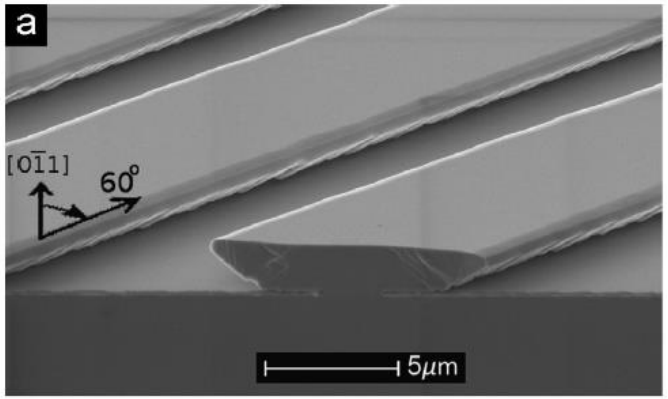


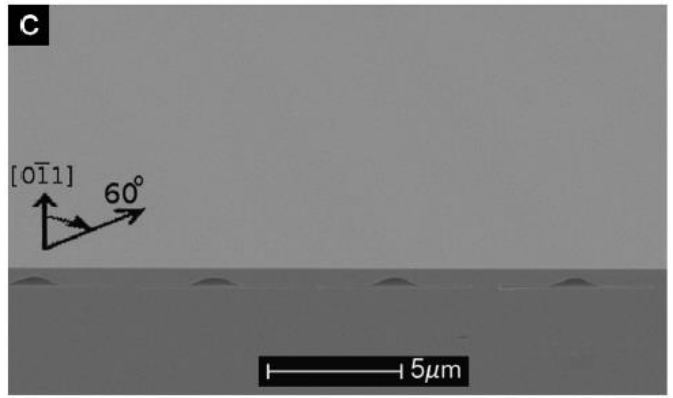
Epitaxial Lateral Overgrowth

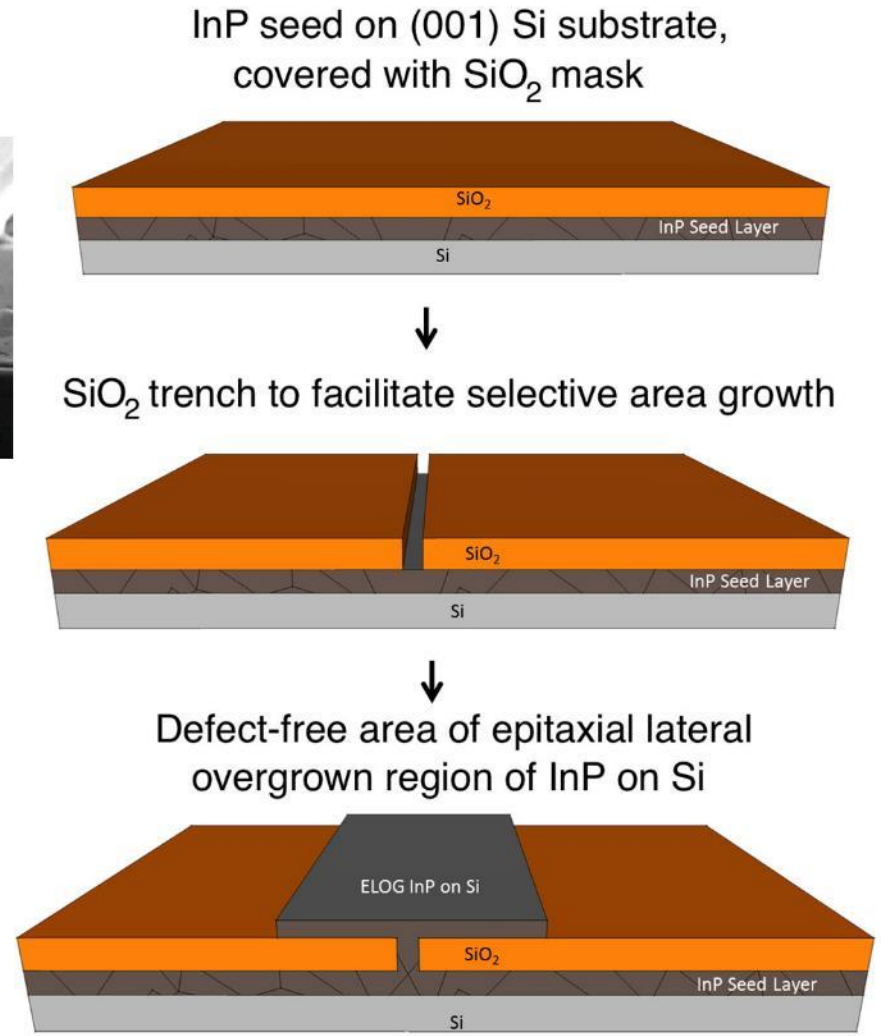
- Growth through small trench
- Filters out defects
- Layer on top of mask is high-quality
- Problem with void formation upon merging stripes
- Still high defect density above openings



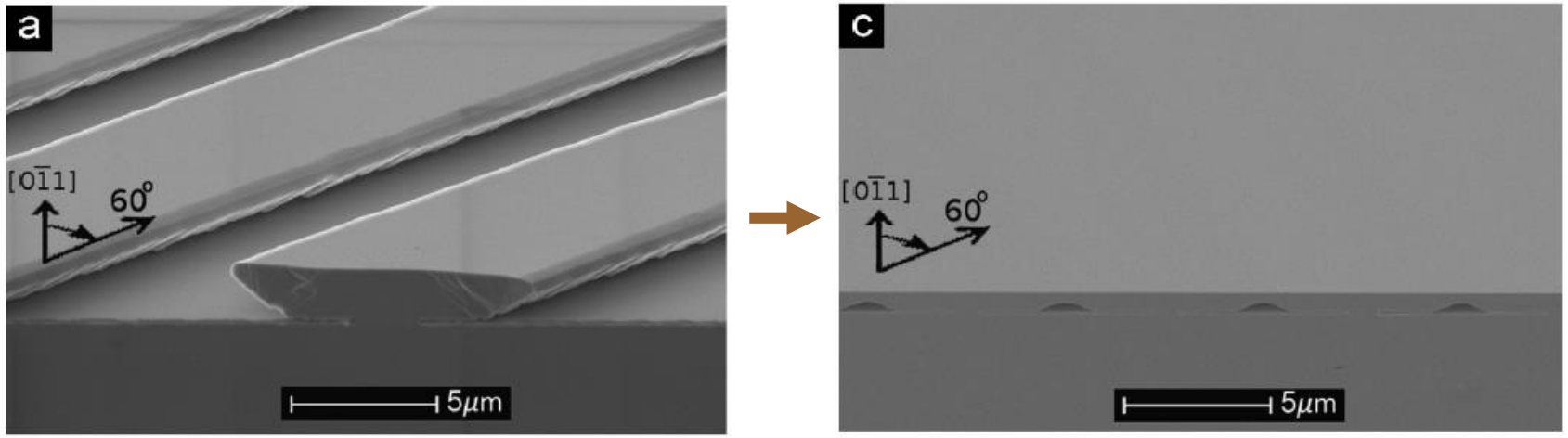
Wierzbicka et al. JAP 2009

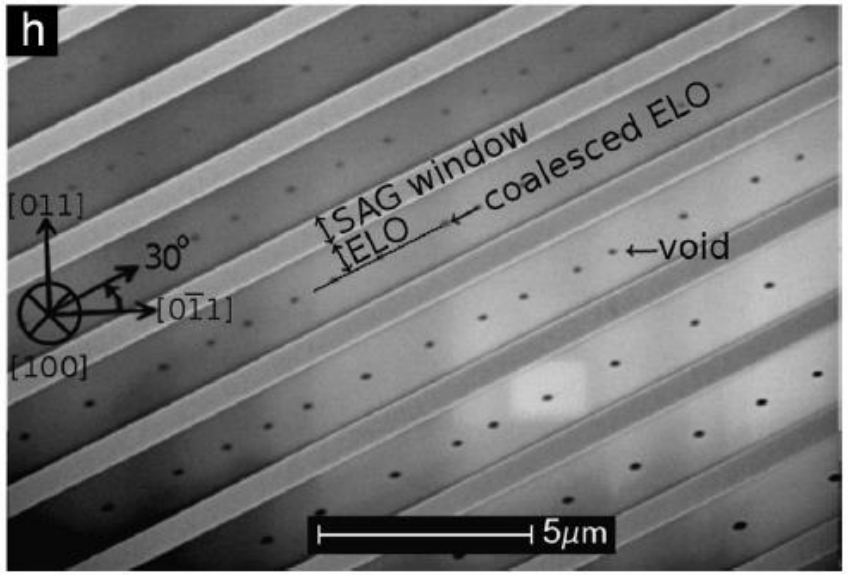




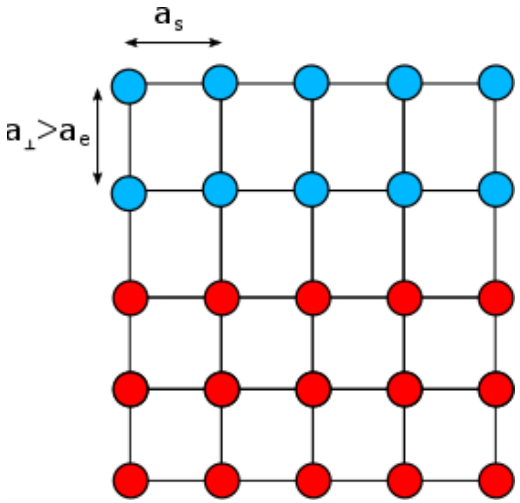


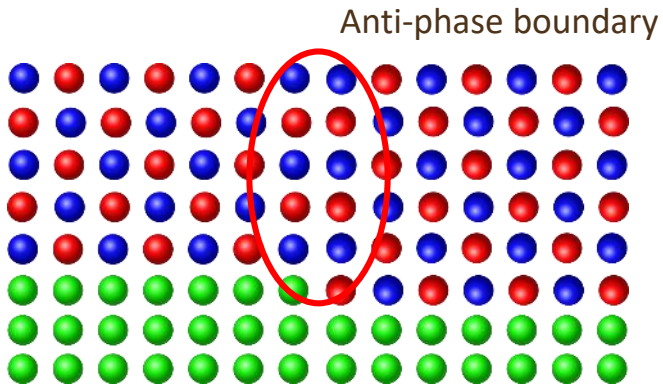
Problem of merging growth fronts



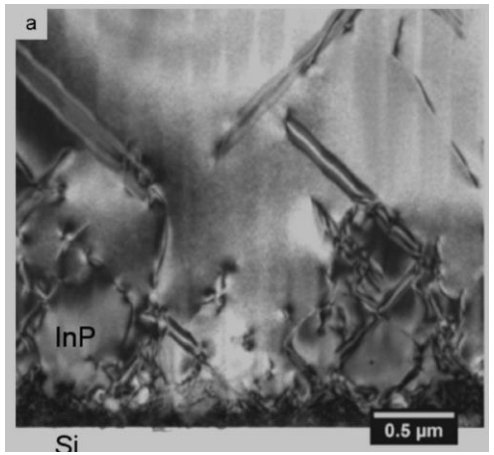


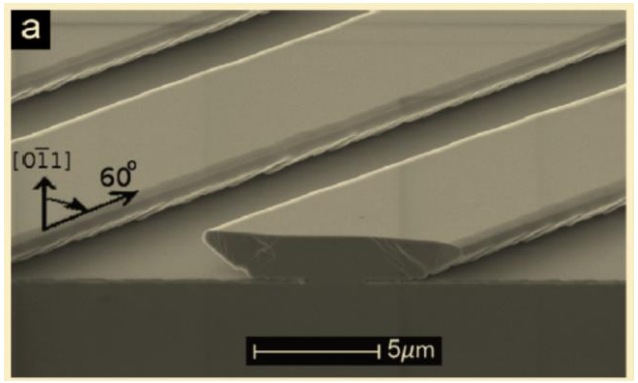
- Faceting can cause voids
- Crystal misalignment can cause defects



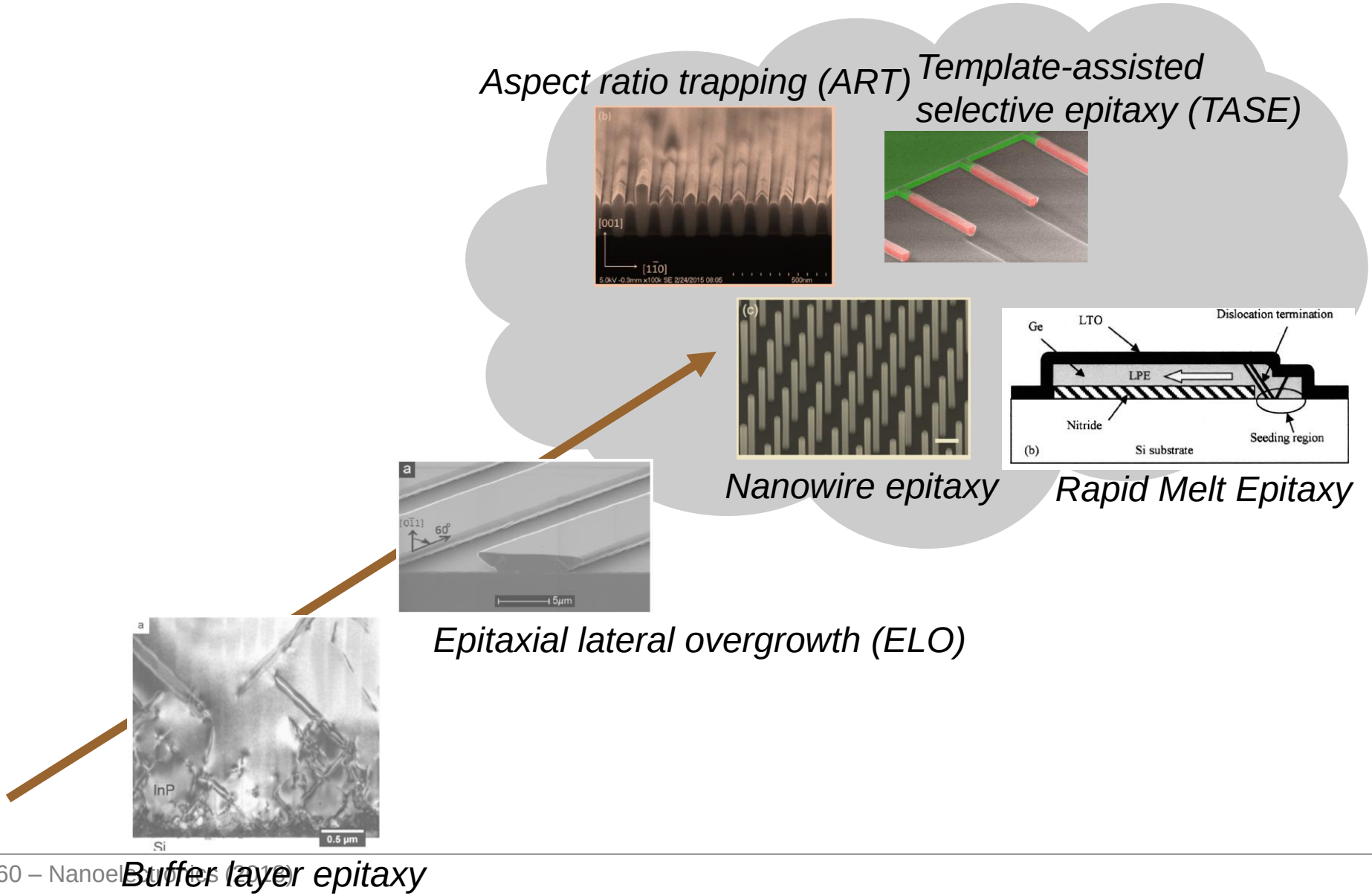


Break





Epitaxial integration methods

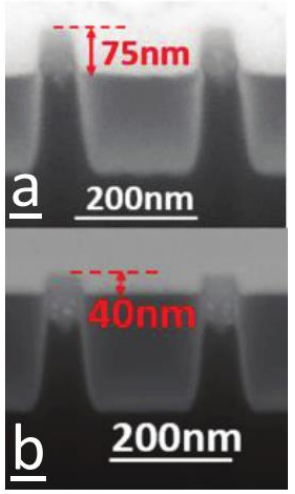


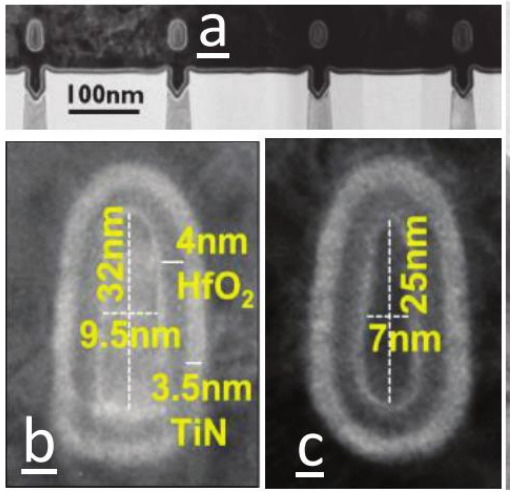
Aspect ratio trapping (ART)

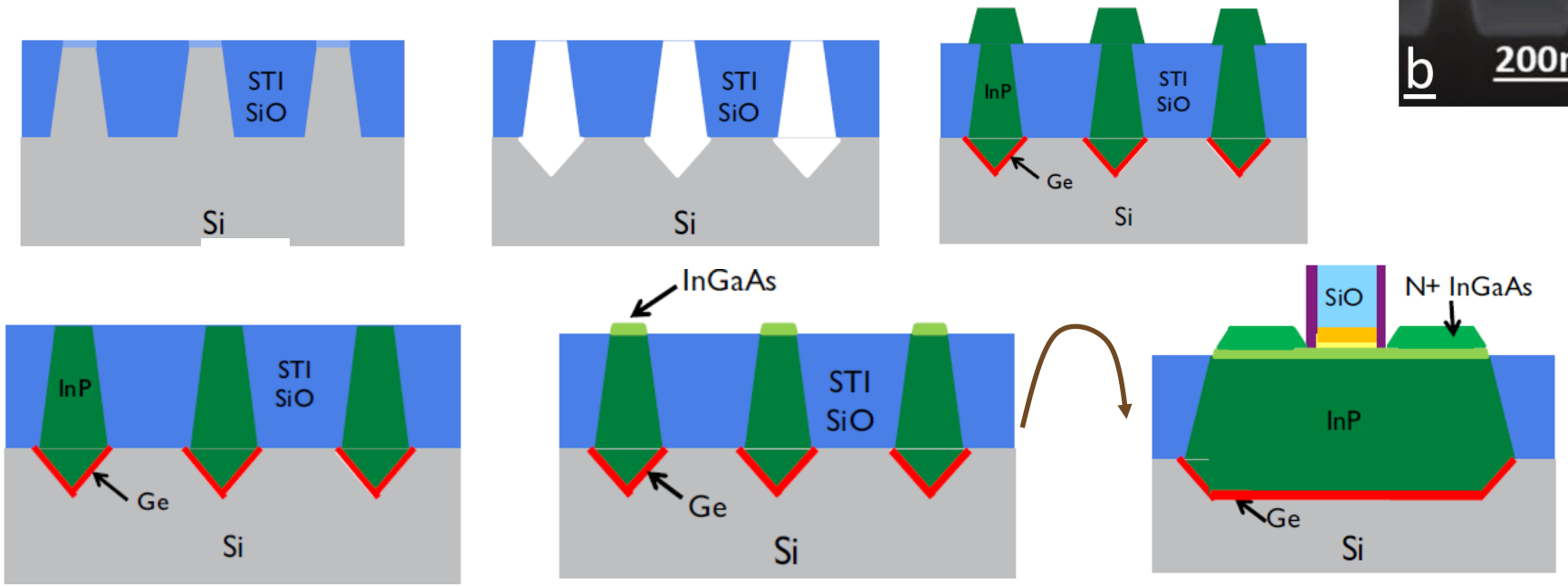
NANO ELECTRONICS GROUP

IMEC VLSI 2016

- Idea:
  - Based on ELO concept but no merging
  - High aspect ratio windows (trenches) to catch all defects
- Progress lead by IMEC, Sematech
- Completely compatible with Si CMOS fin processes (replacement fin)



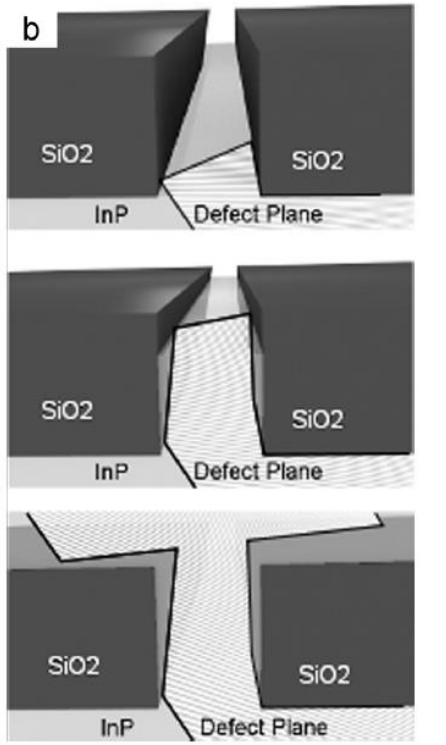


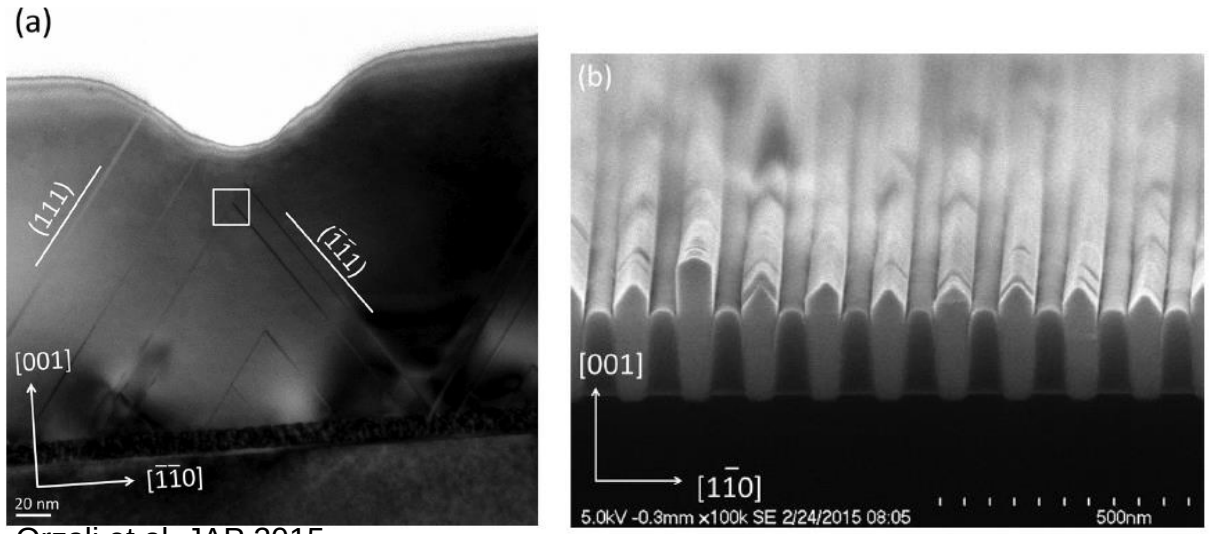


Defect ”trapping” in ART

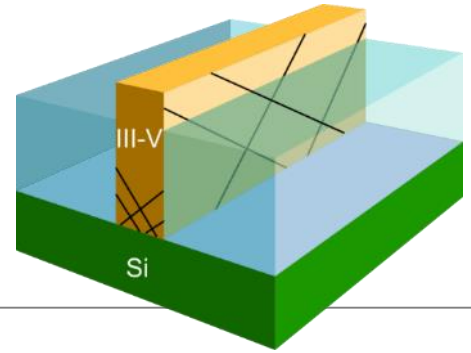
- Defects (dislocation threading, twins, stacking faults) occur on (111) planes
- Defects across the trenches terminate on oxide
- Defects along the trench may not be trapped
- Two-step growth improves this → Maximize nucleation density to prevent threading

Julian et al JCG 2014



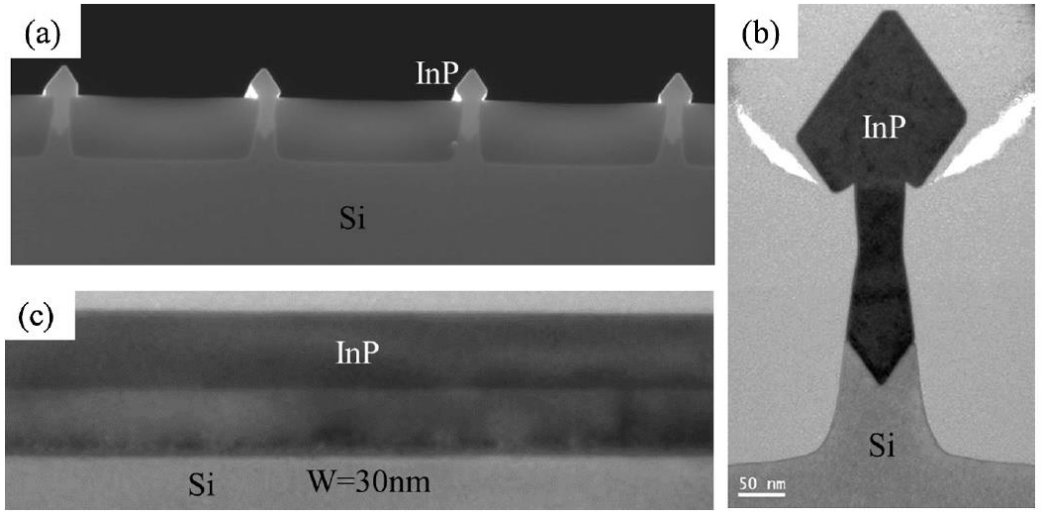


Orzali et al. JAP 2015

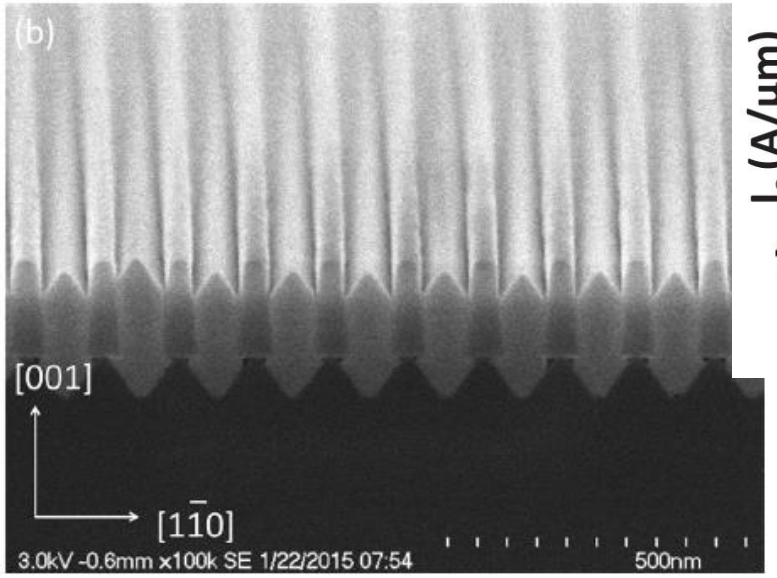


Latest status

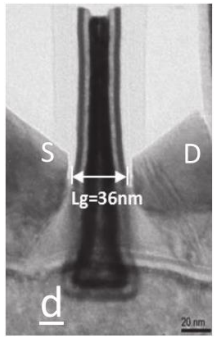
- V-groove at bottom deemed crucial
- IMEC:
  - **Two-step growth** to create a dense twin network
  - Mg Counterdoping to increase resistivity in InP



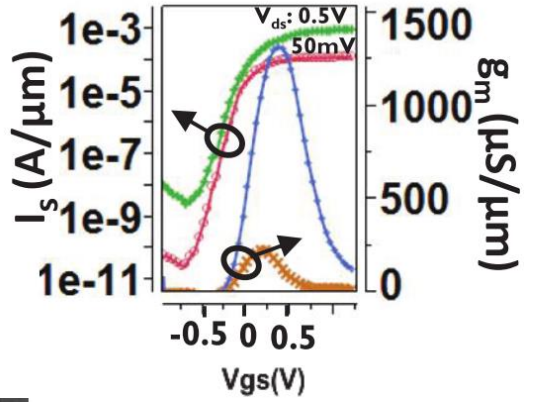
Waldron et al. SSE 2016 (IMEC)



Orzali et al. JAP 2015 (SEMATECH)



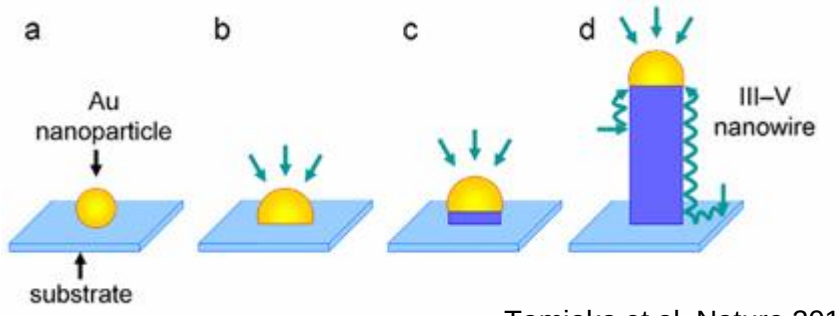
- I_{on} = 200 µA/µm (V_{DS}=0.5V)
- g_m = 1.3 mS/µm (V_{DS}=0.5V)
- μ_{FE} ~ 1200 cm^2/Vs
- SS = 82 mV/dec



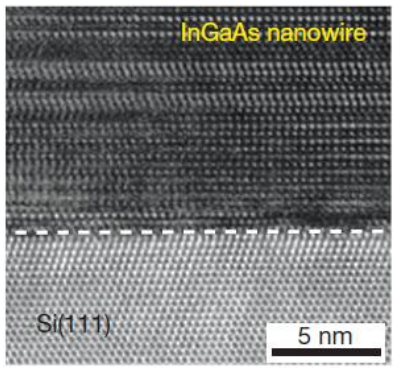
IMEC VLSI 2016

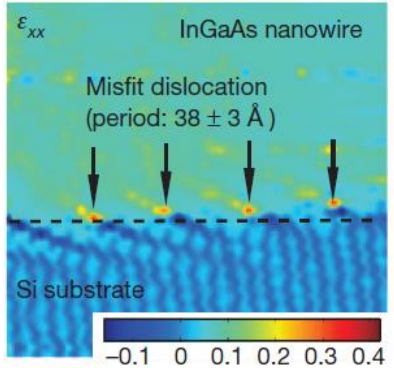
Nanowire epitaxy - VLS

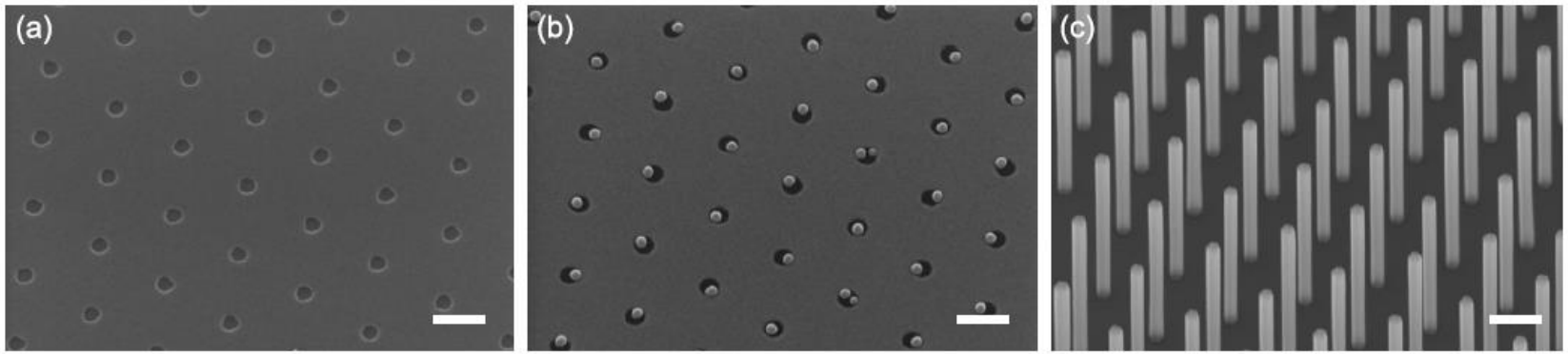
- VLS – Vapour Liquid Solid
- Selective growth seeded by liquid particle
  - Extrinsic particle (Au, Ag, Al, Sn, ...)
  - Self-assisted (Ga → GaAs, In → InAs)
- Gives nanowire structures along [111]B (usually)
- Strain relaxation by
  - elastic relaxation at small dimensions (some claim)
  - Point contact to Si → Contained misfit dislocation network at heterojunction (observed)



Tomioka et al. Nature 2012



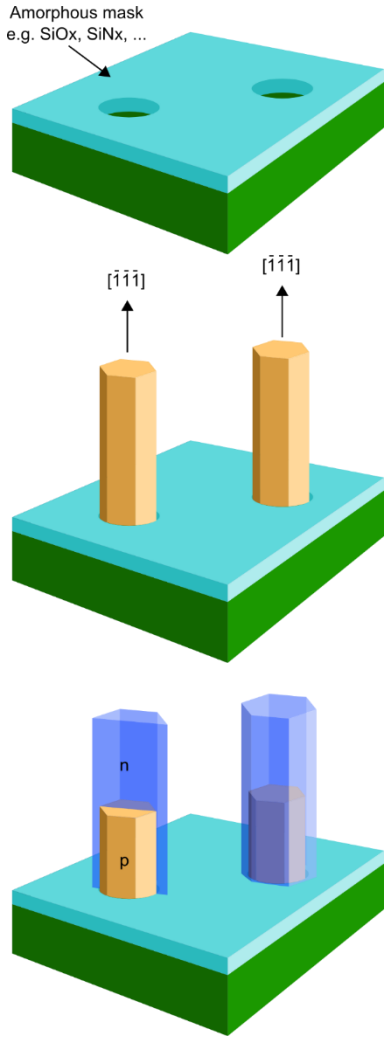




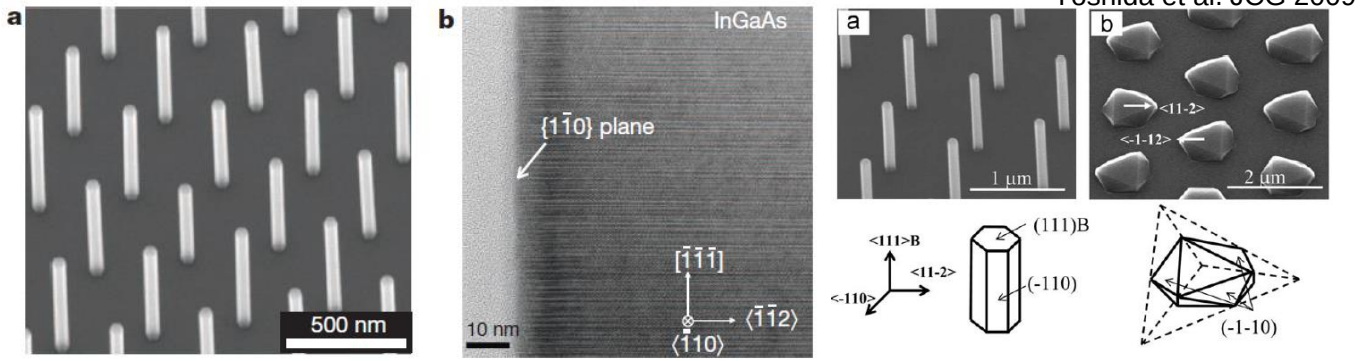
Plissard et al. Nanotechn. 2011

Nanowire epitaxy – Selective area

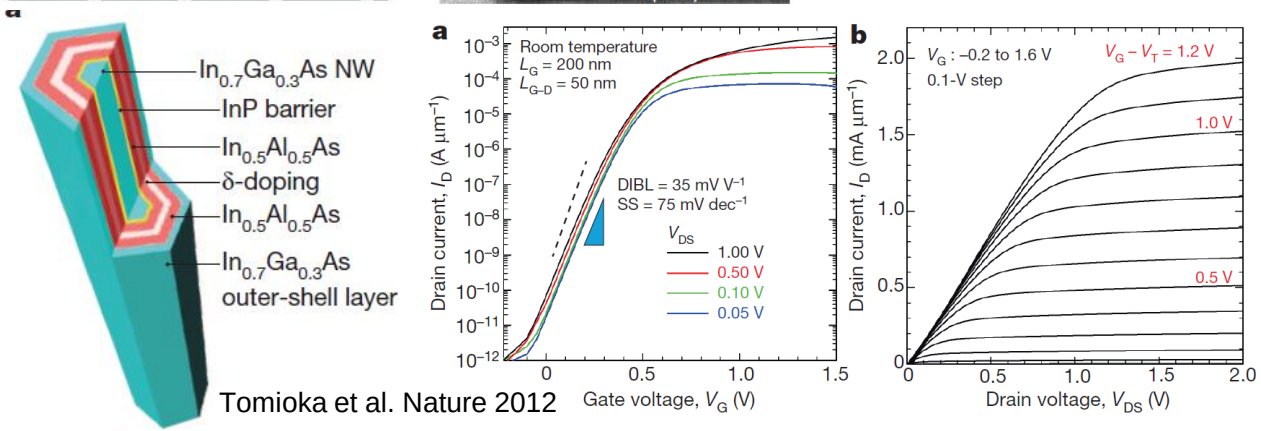
- No seed → abrupt junctions, CMOS compatible
- **Twin defects are necessary**!! → Prismatic crystal shape
  - (111)B top and {110} side facets
- Aspect rato given by growth rate anisotropy
- Excellent devices demonstrated by Hokkaido group



Yoshida et al. JCG 2009

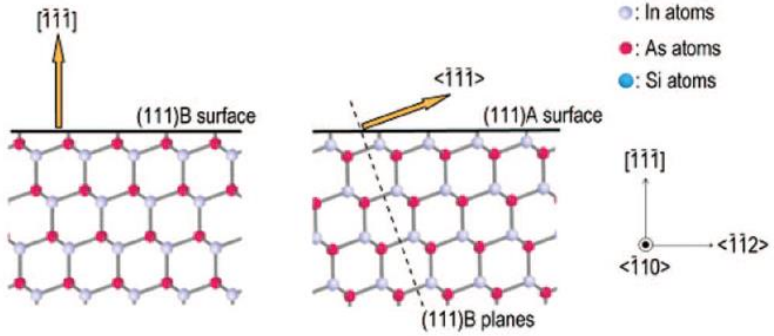


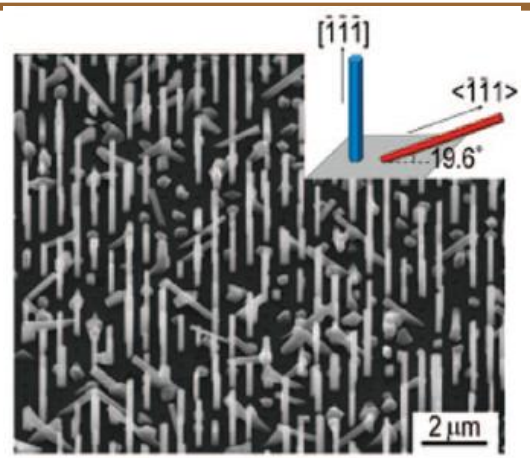
Tomioka et al. Nature 2012



Limitations of nanowire epitaxy

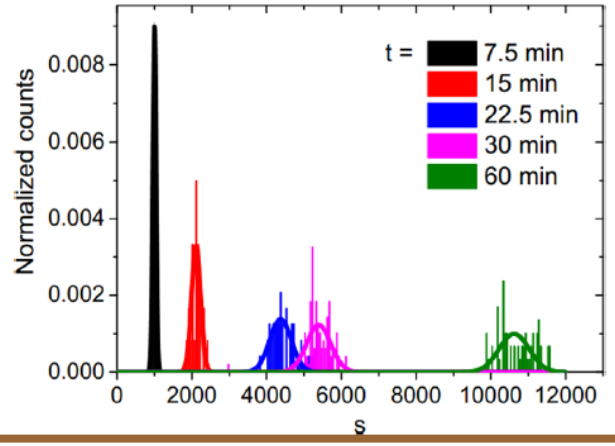
- Non-polarity of Si
  → Equiv. nucleation dir.
- Vertical or inclined nanowire growth

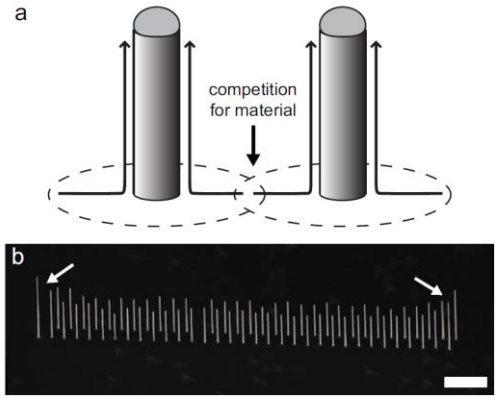




Tomioka et al. Nano Lett. 2008

Dubrovskii et al. CGD 2016





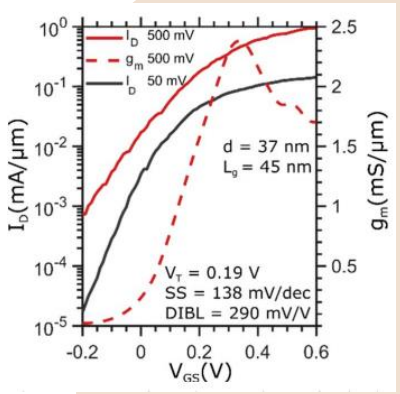
- Axial growth rate varies with
  - diameter
  - neighborhood
- Radial growth

→ Morphology variations

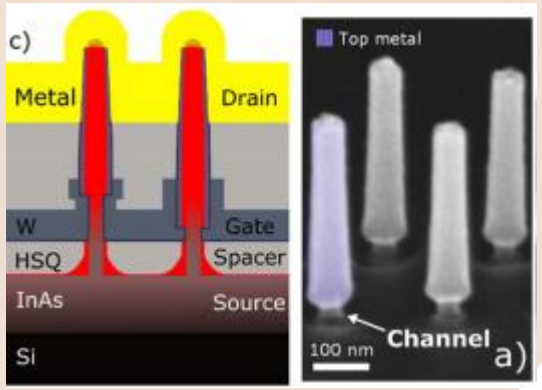
Latest status of vertical nanowire devices

NANO ELECTRONICS GROUP

VLS Nanowires

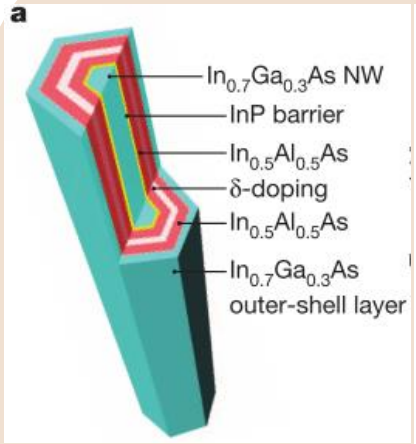


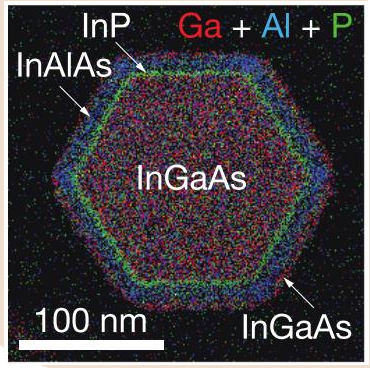
- Self-aligned S/D → lower R_{on}
- I_{on} = 407 μA/μm (V_{DS}=0.5V)
- g_m = 2.4 mS/μm (V_{DS}=0.5V)
- μ_{FE} ~ 1200 cm²/Vs
- SS = 85 mV/dec

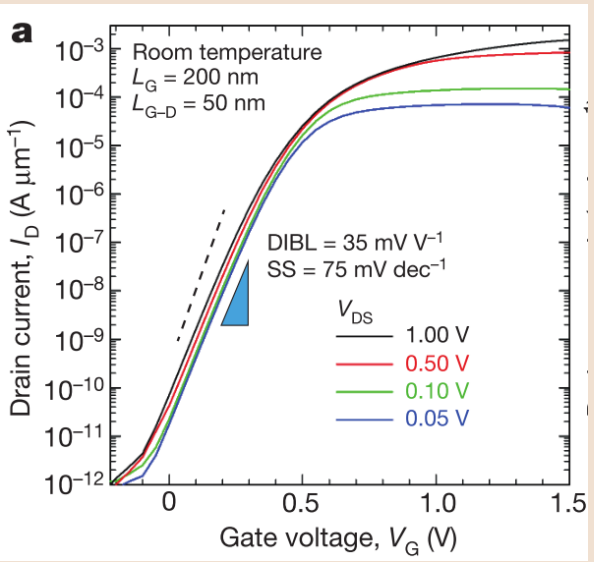


Kilpi et al. IEDM 2017

Selective-area Nanowires







- HEMT structure
- InGaAs QW
- I_{on} = 450 μA/μm (V_{DS}=0.5V)
- g_m = 1.42 mS/μm (V_{DS}=0.5V)
- μ_{FE} = 7850 cm²/Vs
- SS = 75 mV/dec

Tomioka et al. Nature 2012

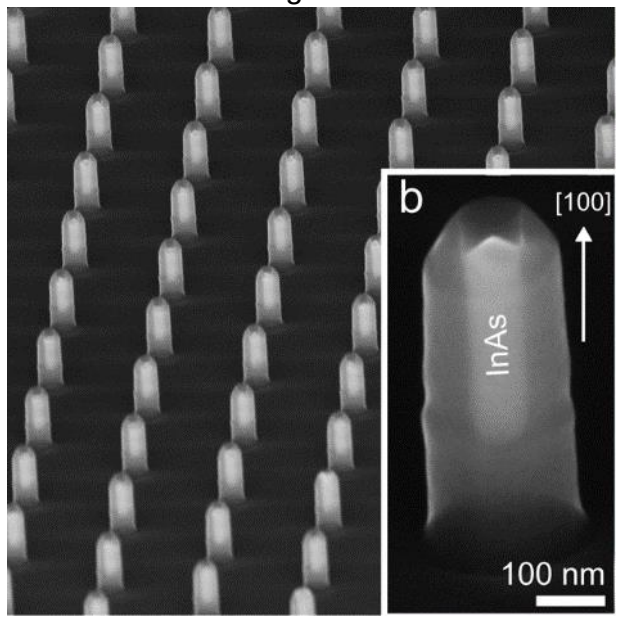
Template-assisted selective epitaxy (TASE)

- A combination of ELO, ART, and nanowire growth

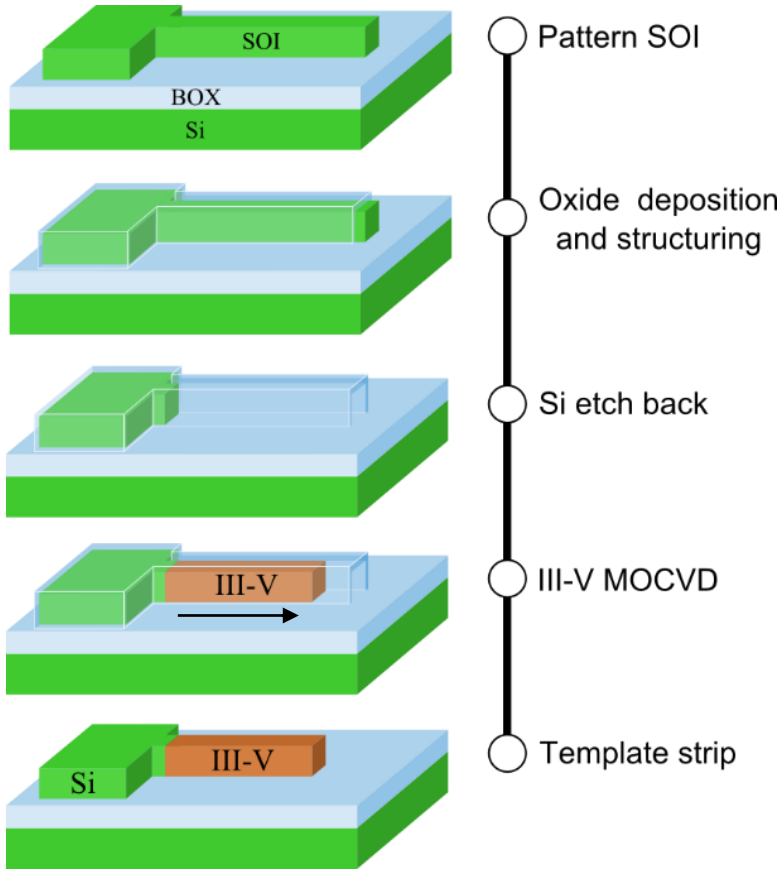
Key concepts:

1. Limit epitaxy to start from a **single nucleation point**
2. Assist the crystal growth to desired shape by confining epitaxy within an **oxide template**.

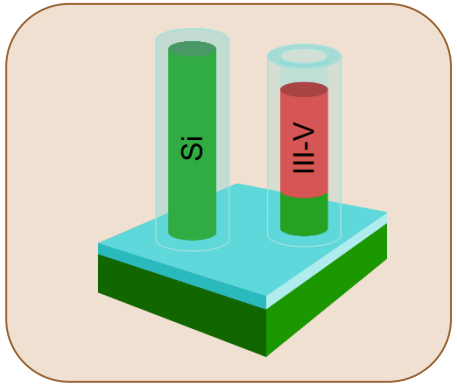
Borg et al. Nano Lett. 2014



In practice

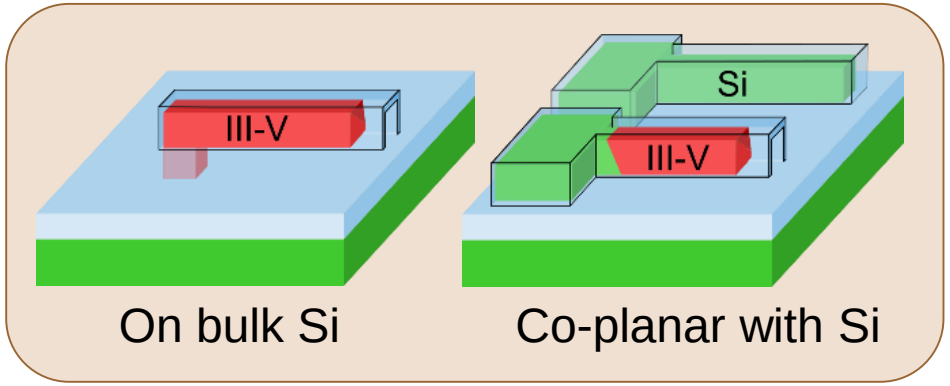


Vertical process



Borg et al. Nano Letters 2014

Horizontal process

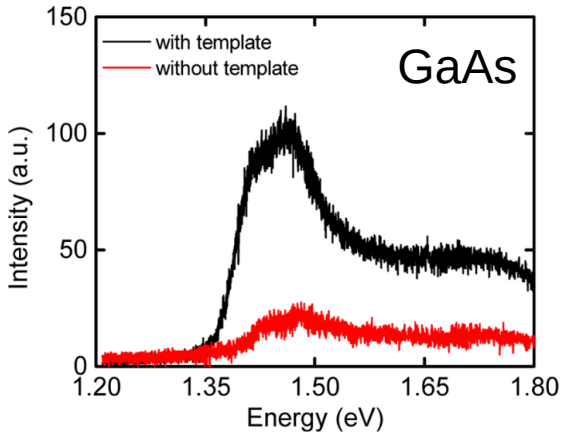


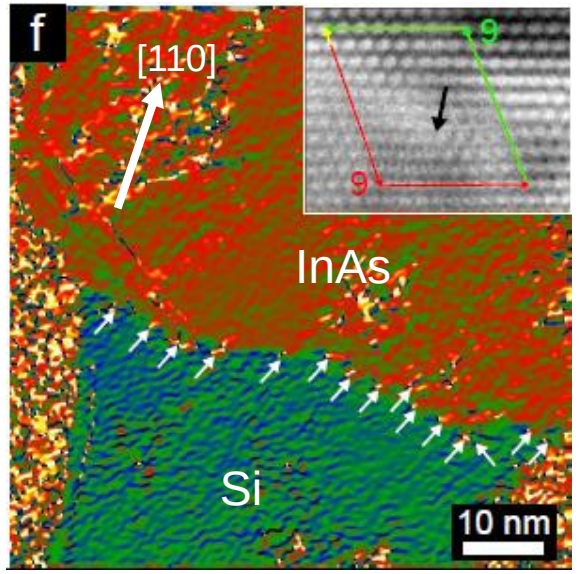
Czornomaz et al. VLSI 2015

Schmid et al. APL 2015

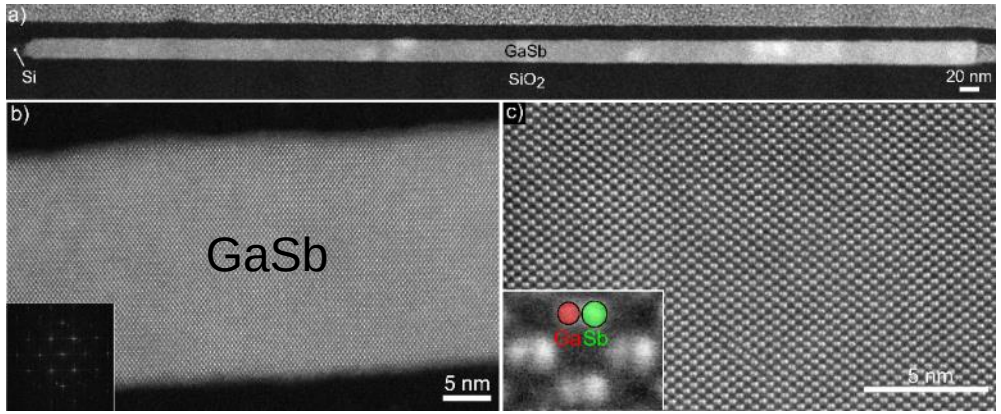
Material quality with TASE

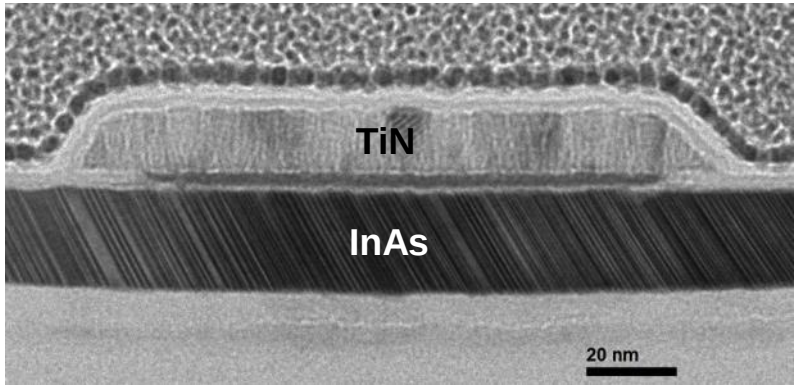
- Misfit dislocations contained at heterojunction
- Twin plane defects often present in arsenide materials (InAs, GaAs,..)
  - → Increased carrier scattering
  - – GaSb has been made twin-free
- The surface is intrinsically protected from oxidation
  - → Less surface electronic states?





Borg et al. Nano Lett. 2014

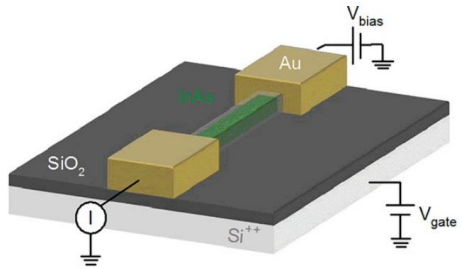


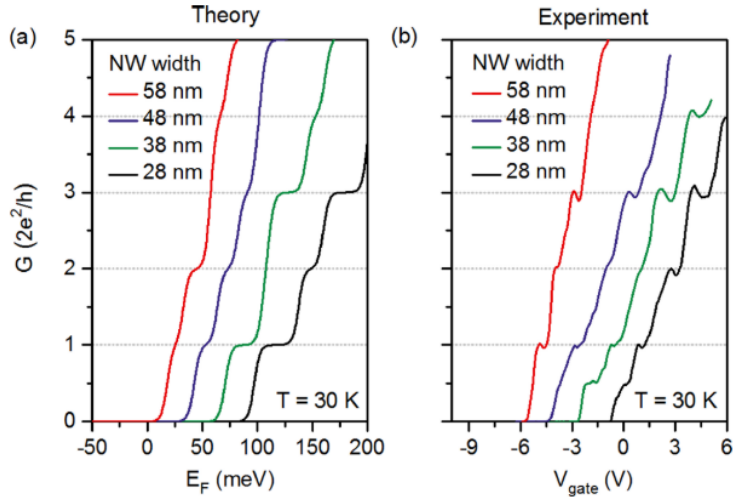


Transport properties in TASE

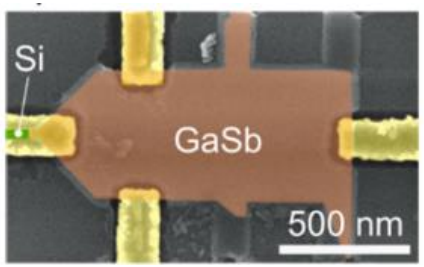
- High carrier mobility (at 300 K)
  - 23 nm InAs: μ_n = 5400 cm^2/Vs
  - 20 nm GaSb: μ_p = 760 cm^2/Vs
- Ballistic transport in InAs 1D nanowires < 50 K
  - Conductance quantization observed
  - Mean free path =

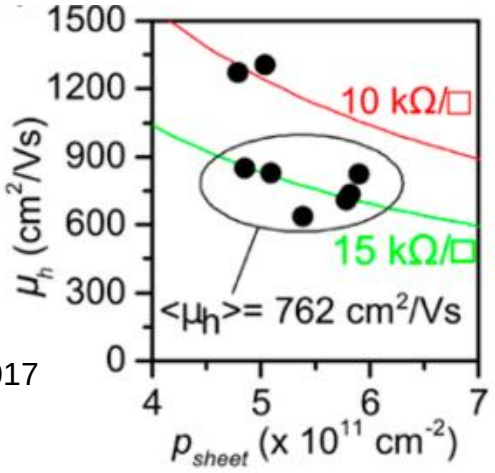
    470 nm @ 30 K, 1 µm @ 4 K
- Ballistic transport maintained over up to four cross junctions



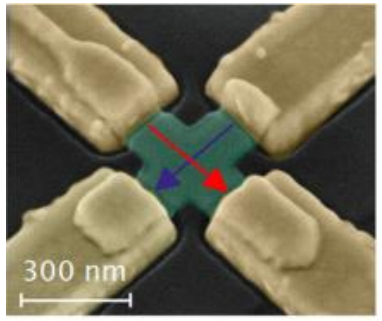


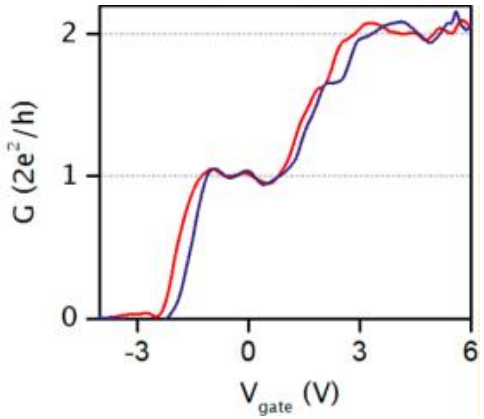
Gooth et al. APL 2017





Borg et al. ACS Nano 2017

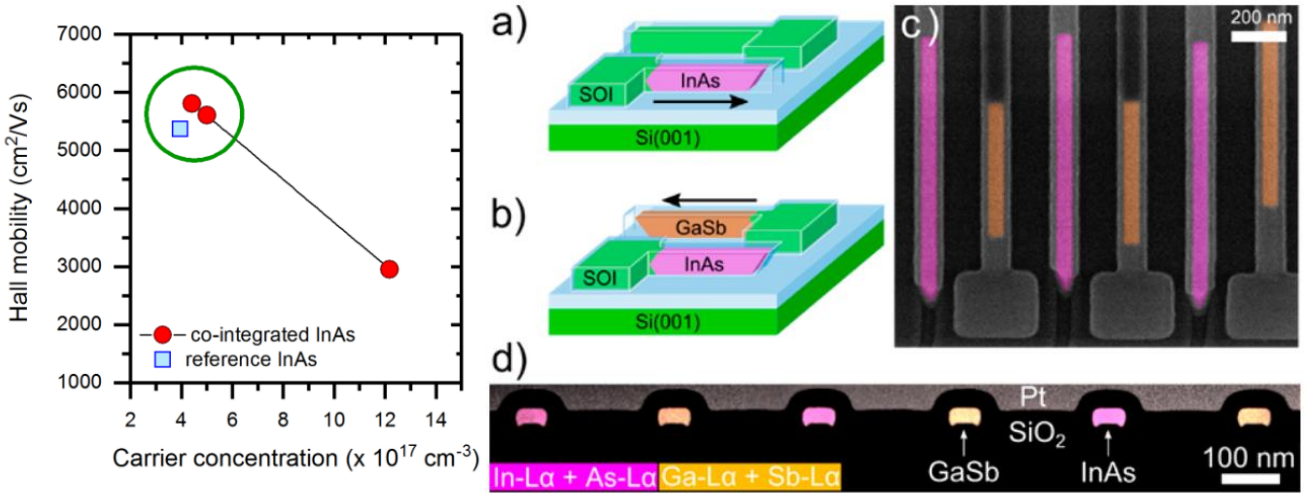




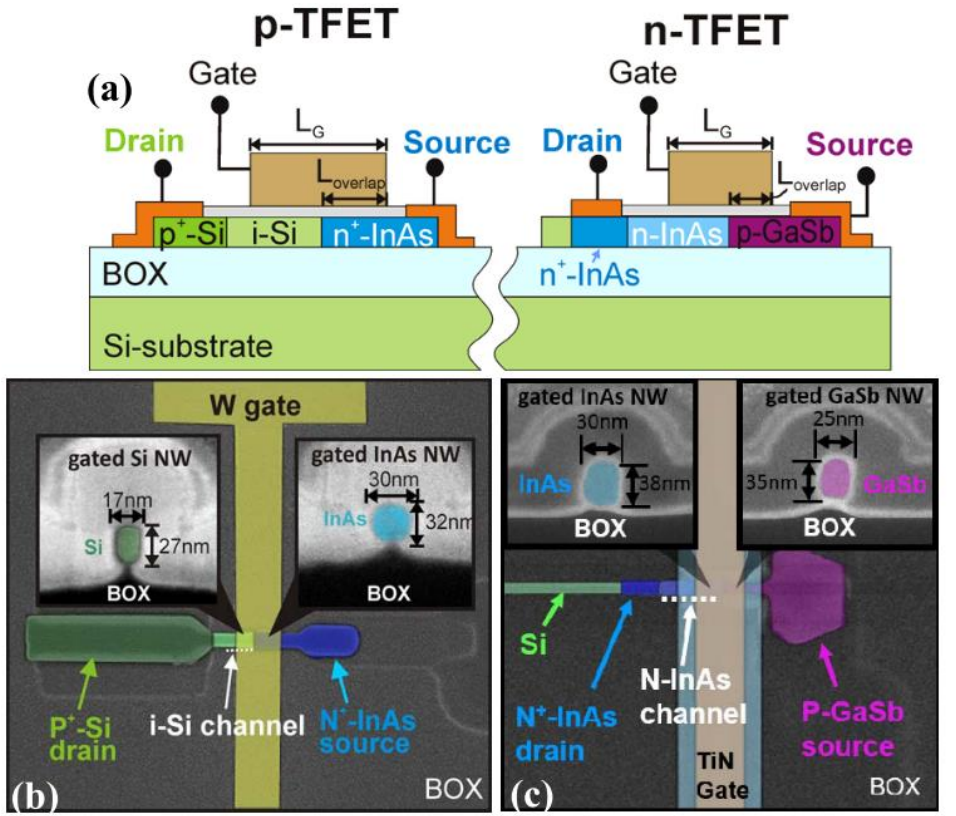
Gooth et al. Nano Lett. 2017

Cointegration of multiple materials

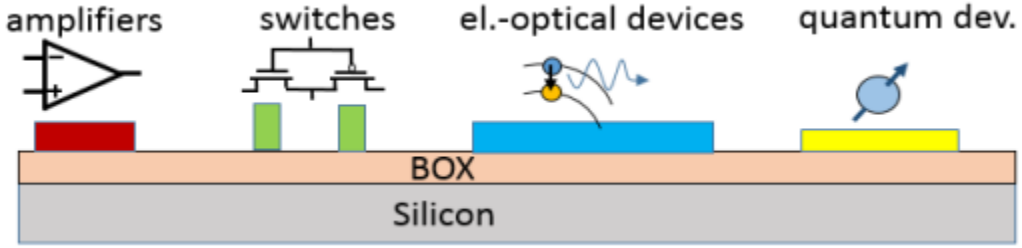
- Sequential repetition of TASE allows for multiple channel materials densely spaced.
  → III-V Complementary logic
- GaSb and InAs cointegrated
- First material remains unchanged



Borg et al. ACS Nano 2017

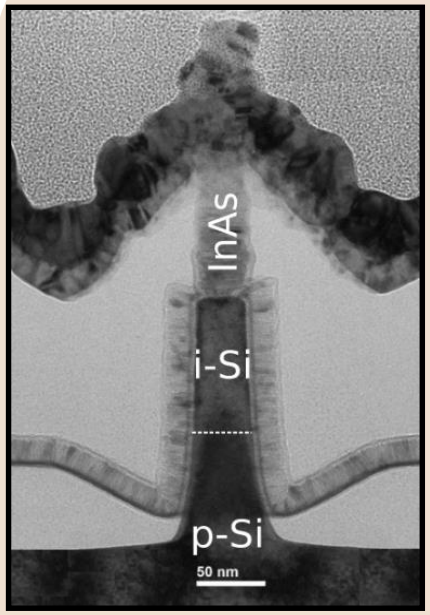


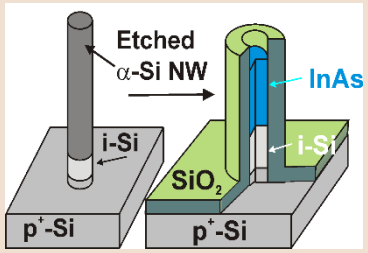
Cutaia et al. VLSI 2016

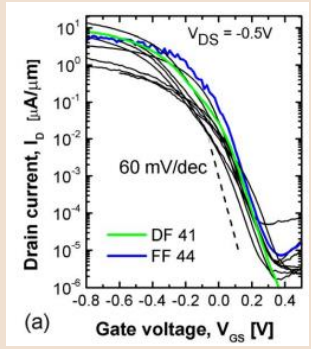


Device implementations

Vertical Tunnel Field effect-transistors





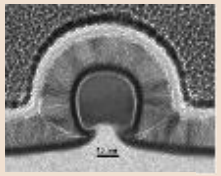


Cutaia et al. J-EDS 2015
Moselund et al. TED 2016

- I_{on} = 5 μA/μm (V_{DS}=0.5 V)
- I_{on}/I_{off} = 10^6
- SS = 70 mV/dec

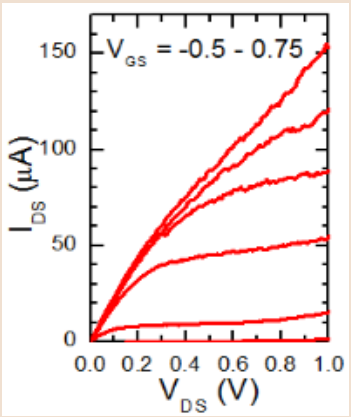
finFETs for III-V CMOS

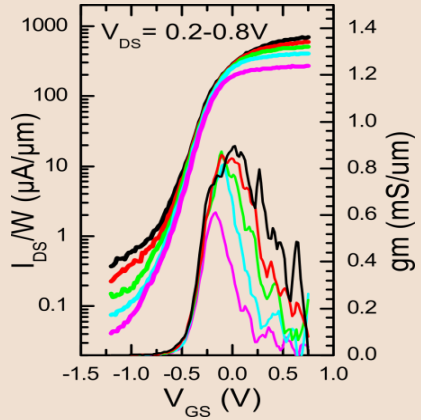
InAs fin



23x25 nm

- I_{on} = 480 μA/μm (V_{DS}=0.5V)
- g_m = 0.9 mS/μm (V_{DS}=0.5V)
- μ_{FE} ~ 500 cm^2/Vs
- SS = 250 mV/dec

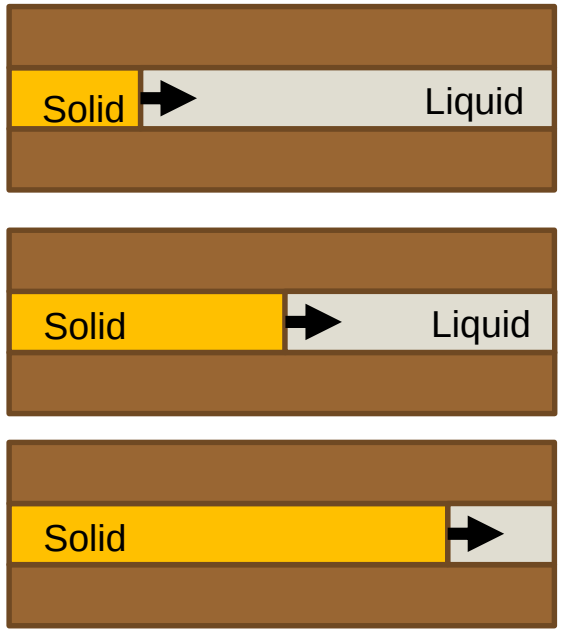


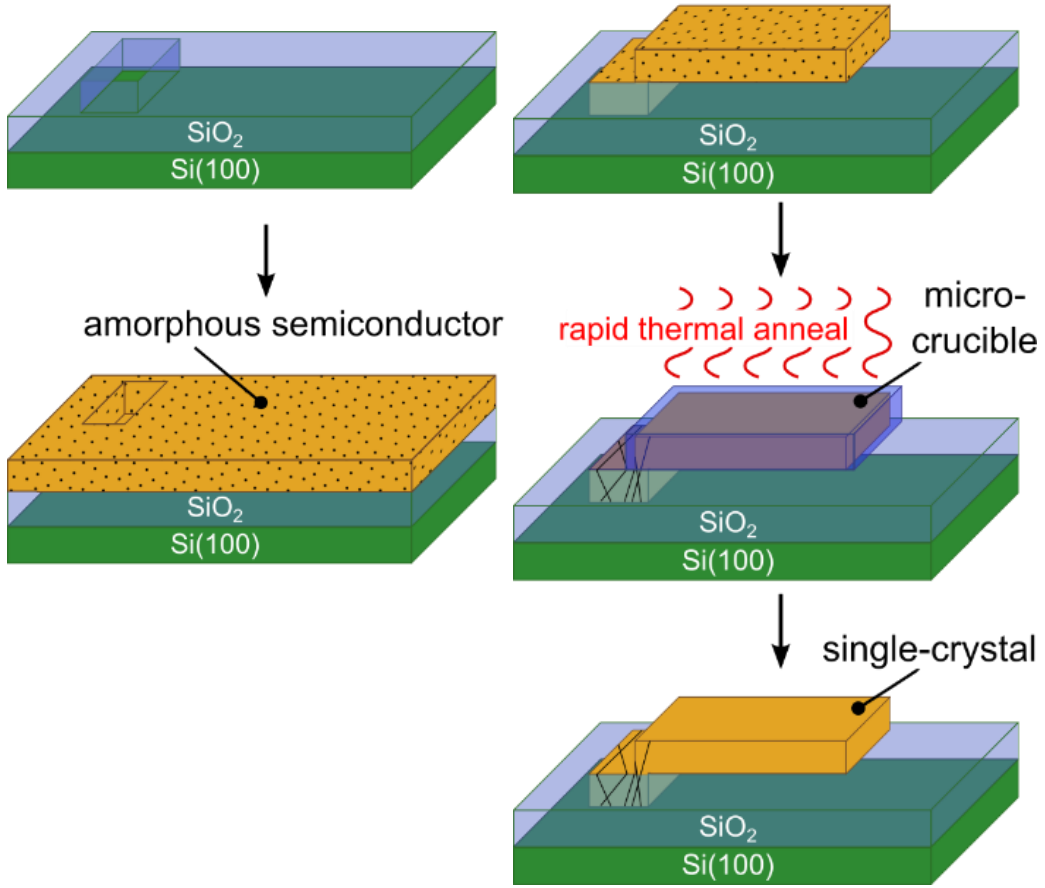


Schmid et al. APL 2015

Rapid Melt Epitaxy

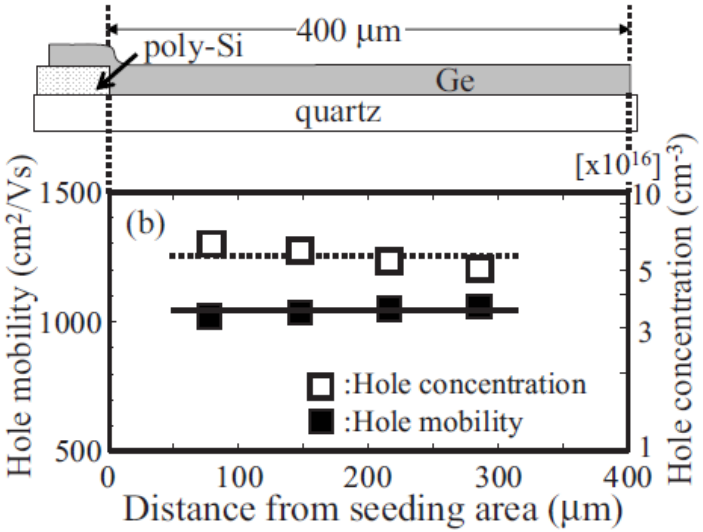
- **Single crystalline heteroepitaxy is achieved by melting and recrystallizing nanostructured III-V (or Ge)**



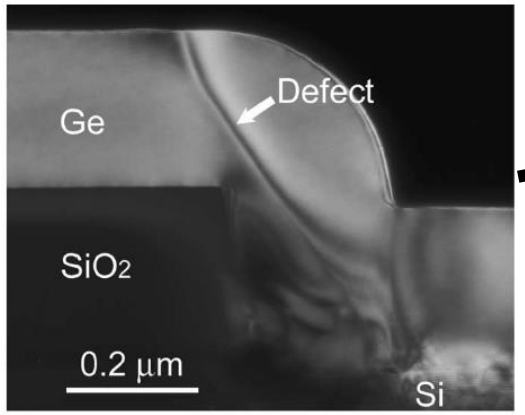


Rapid Melt Epitaxy

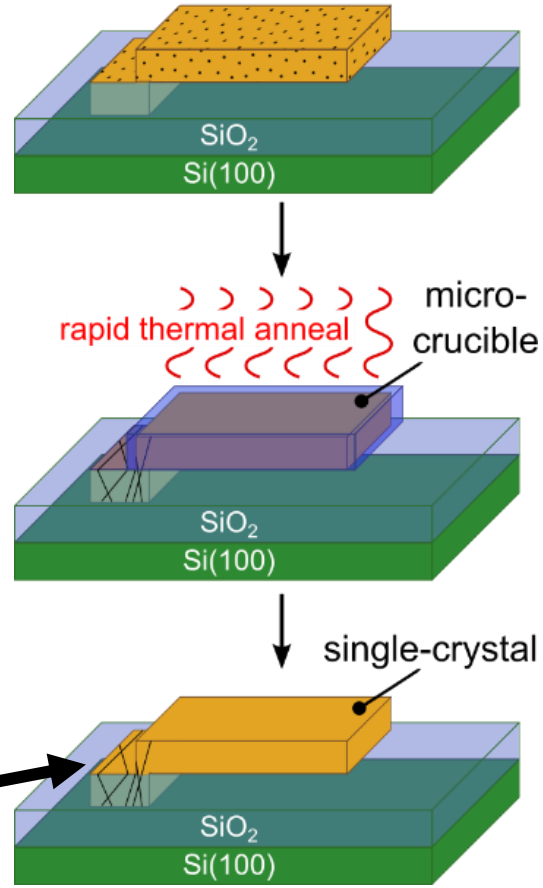
- Small contact point between Si and III-V /Ge.
  - Heterogeneous nucleation at this interface
  - Defects are confined near this interface
- Very high crystal quality (μ_h(Ge) ~ 1000 cm^2/Vs)



Miyao APL 2009

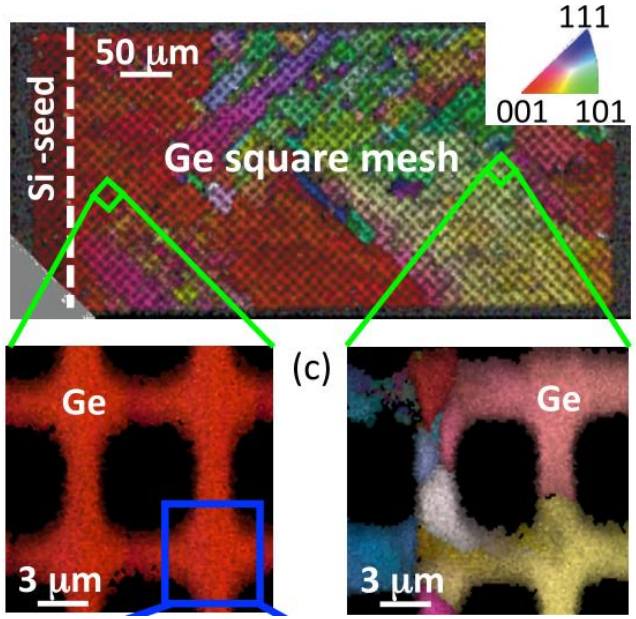


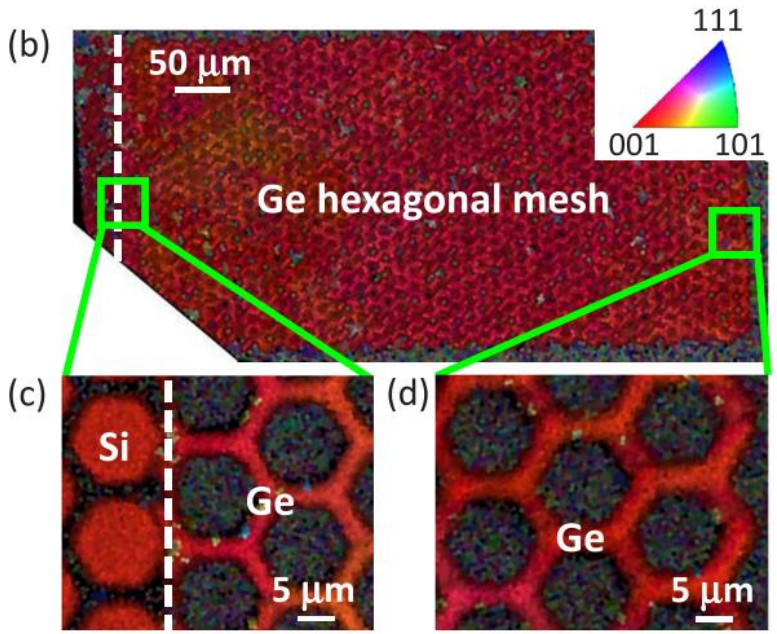
Feng EDL 2006



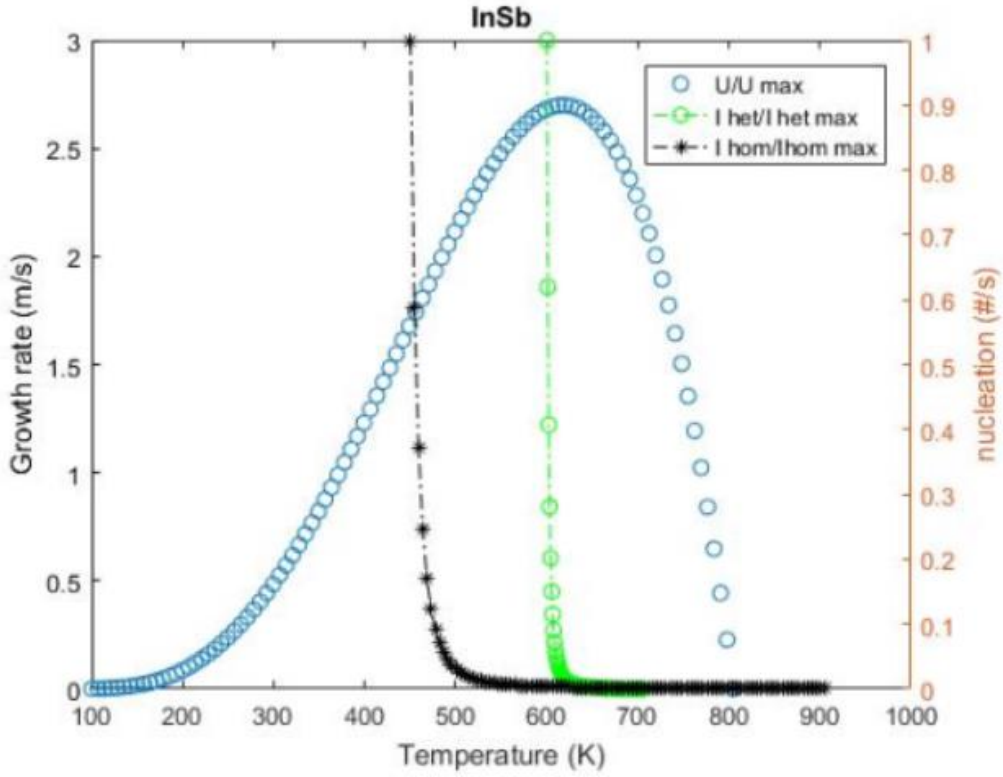
Importance of nucleation rates

- Onset of heterogeneous and homogeneous nucleation at different T → Process window
  - Limits the maximum size of the single crystal
  - Too fast cooling rate → poly-crystal
    - Example: Square vs hexagonal mesh



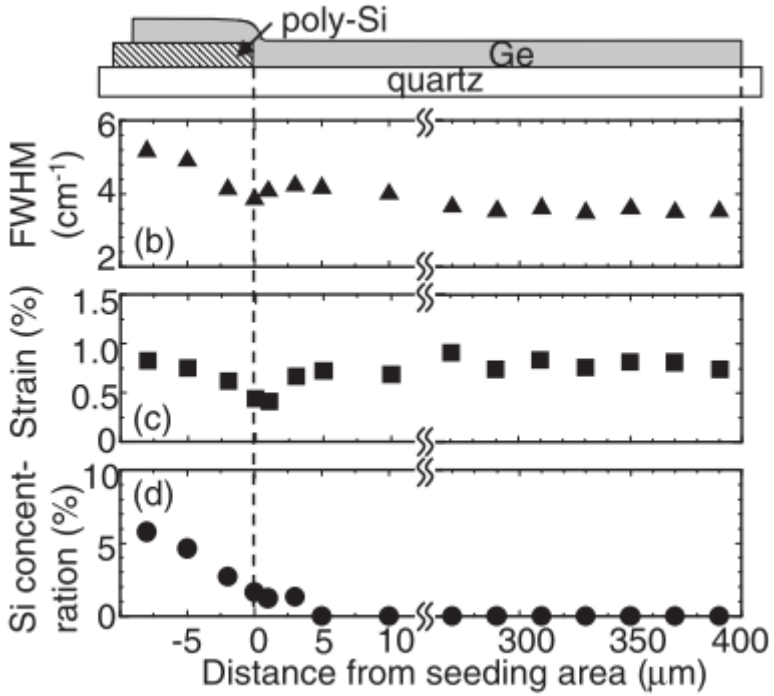


Toko et al. APL 2011

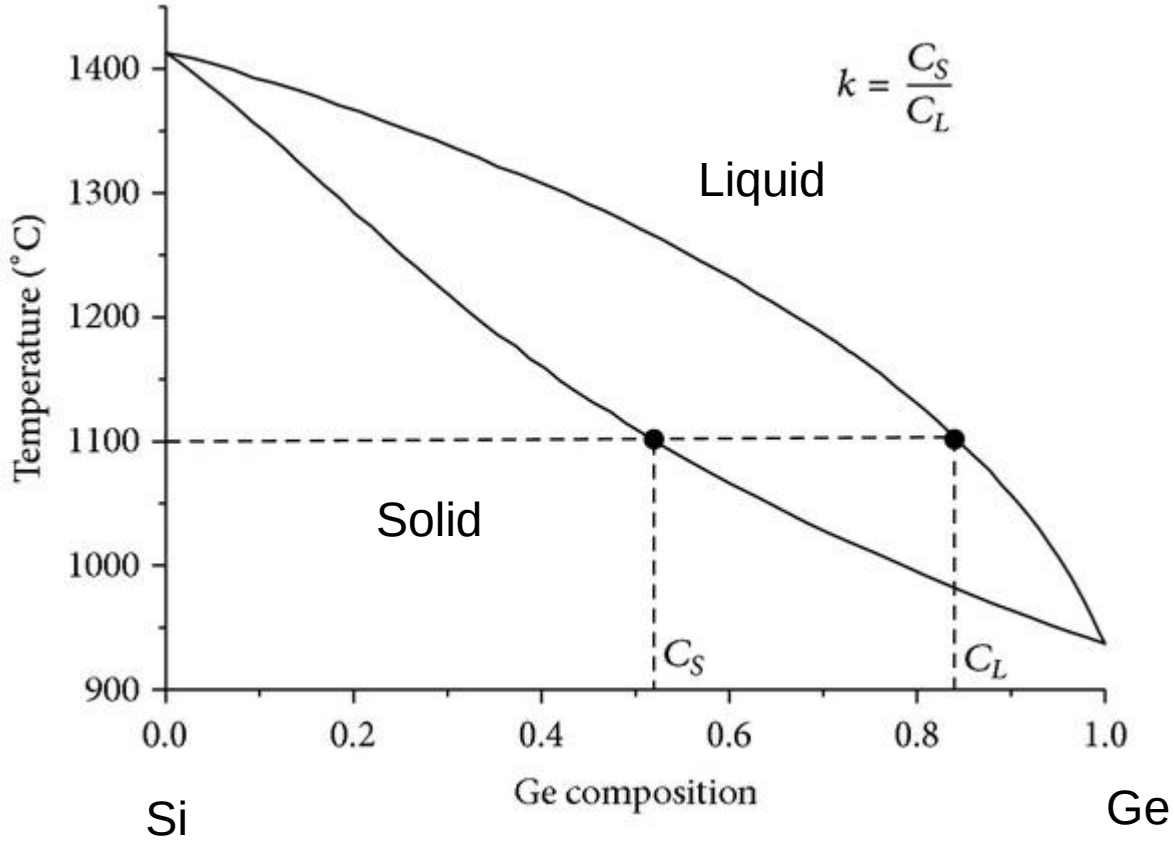


Si interdiffusion problem

- Solid Si in connection with a Ge or III-V liquid
  → dissolution of the Si into the liquid

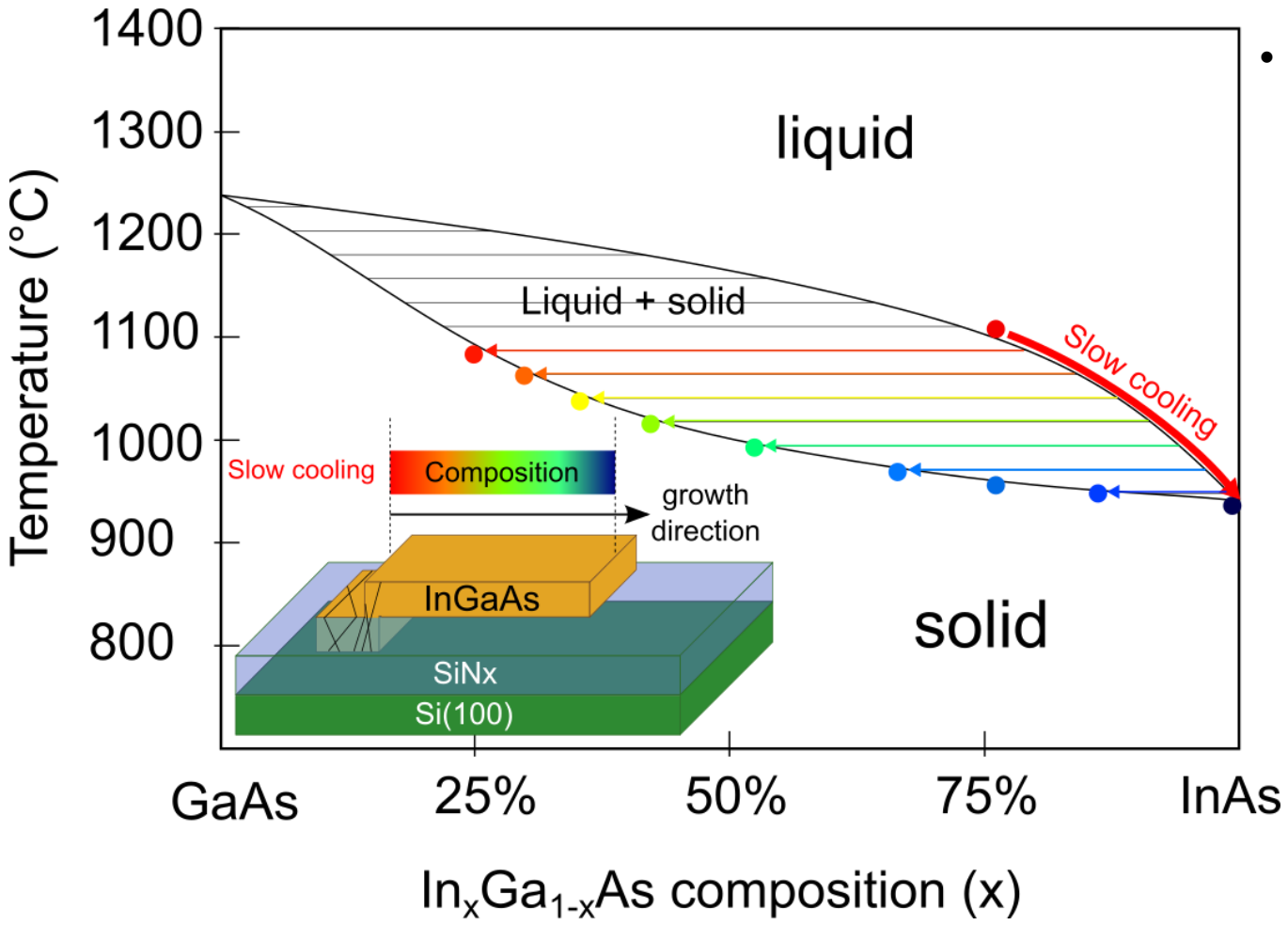


Toko et al. JJAP 2010

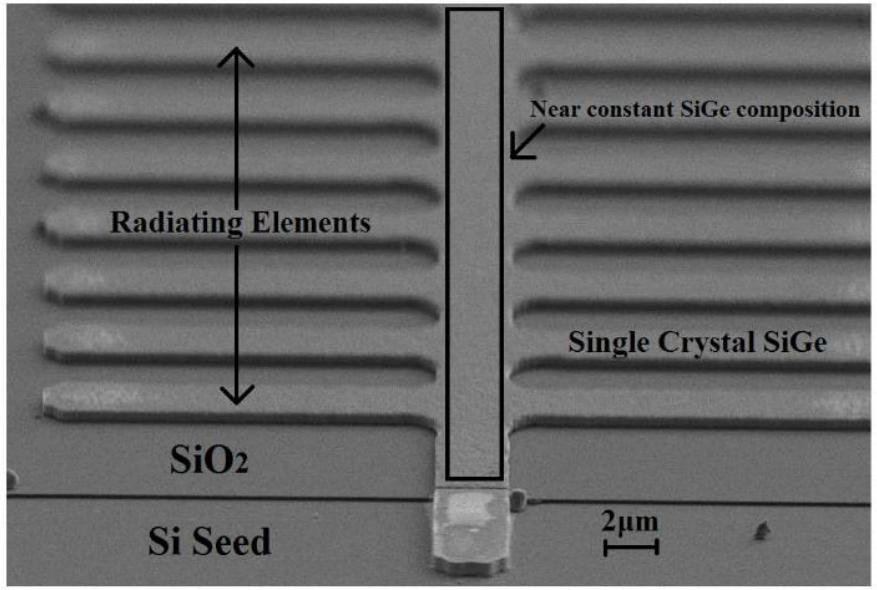


Si Ge

Problem of ternaries in RME



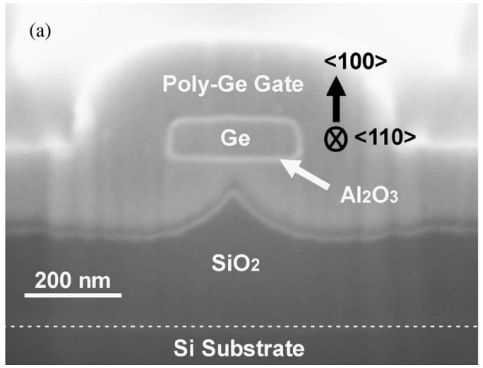
- Thermodynamics favors compositional gradient
- Higher cooling rates → homogeneous composition



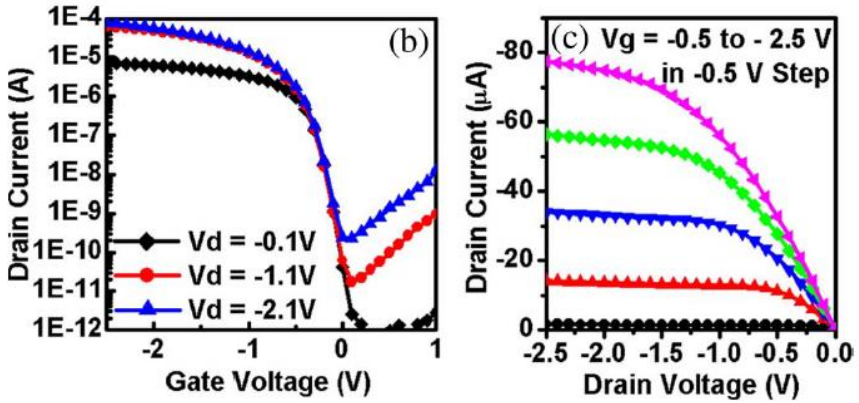
Littlejohns Sci. Rep. 2014

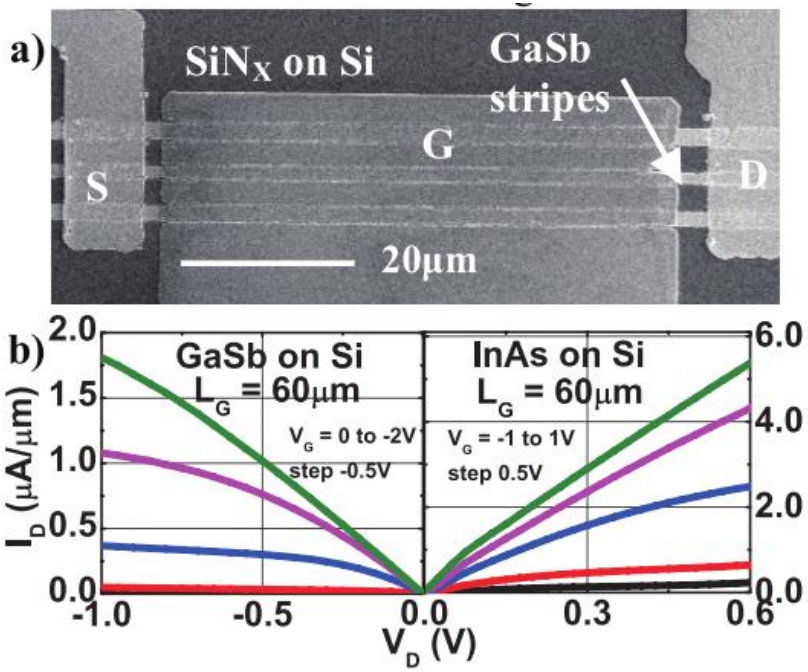
Device results - Rapid Melt Epitaxy

- Not really so many device metrics, focus on larger devices
- Demonstrates good slope and good I_{on}/I_{off}
  - But not performance yet.



Feng EDL 2008

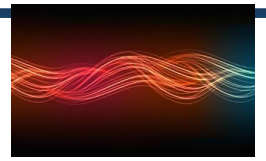




Yuan et al. VLSI 2013

The future

Integrated III-V Comm/Optical/Quantum technology


Si CMOS technology