# Simulation Lab

Optimum NW MOSFET for 100GHz operation

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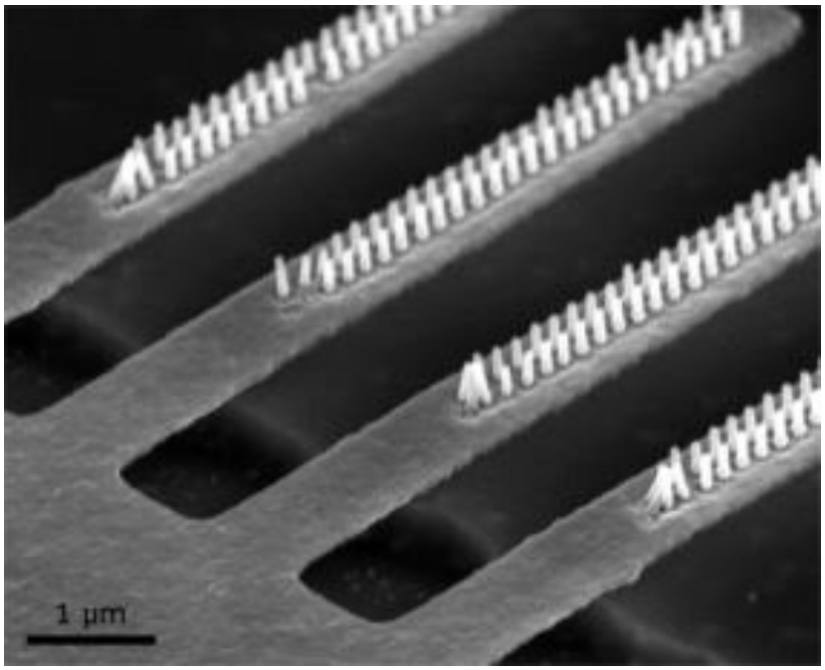
## Lab task: 100 GHz optimum NW MOSFET

The aim of this short lab is to design vertical nanowire MOSFET to maximize power gain and minimize noise figure. Additionally, stabilization and impedance matching are considered as well. To meet the lab goals, the entire task is divided into separate subtasks:

1. DC characterization of the device
2. S-parameter sweep, $\Gamma_{opt}$ analysis
3. Number for wires vs number of gate fingers
4. Stabilization

## Preparation task - Nanowire (NW) MOSFET Technology

Before starting with lab tasks, download and unarchive Nanoelectronics Student Component Library from course homepage (*NSCL_wrk_20190924.7zads*). Start-up and workspace unarchive procedure are available in *ADS Start-up assistance* document from course homepage. Upon opening the workspace, in Folder view, several cells will appear. For the purpose of this project, we are interested in a specific component: NSCL_NW_NMOS. This component represents a model of vertical nanowire MOSFET (see Figure below).




**Above**: Electron micrograph of vertical NW MOSFET mid-process, adapted from O.-P. Kilpi.

Note that the size of the NW MOSFET is described by the gate length, $L$, the number of nanowires, $NW$, and the number of gate fingers, $F$ . The equivalent gate width per nanowire, $W_{eq}$ ≈ 100 nm, can be used to find the traditional gate width, $W = W_{eq} \cdot NW$, of the NW MOSFET. The NWs are typically designed in multiple parallel-connected gate fingers to minimize series-parasitic resistances. The total number of nanowires is divided among gate fingers, which means that no fractional number of nanowires per gate finger is possible.

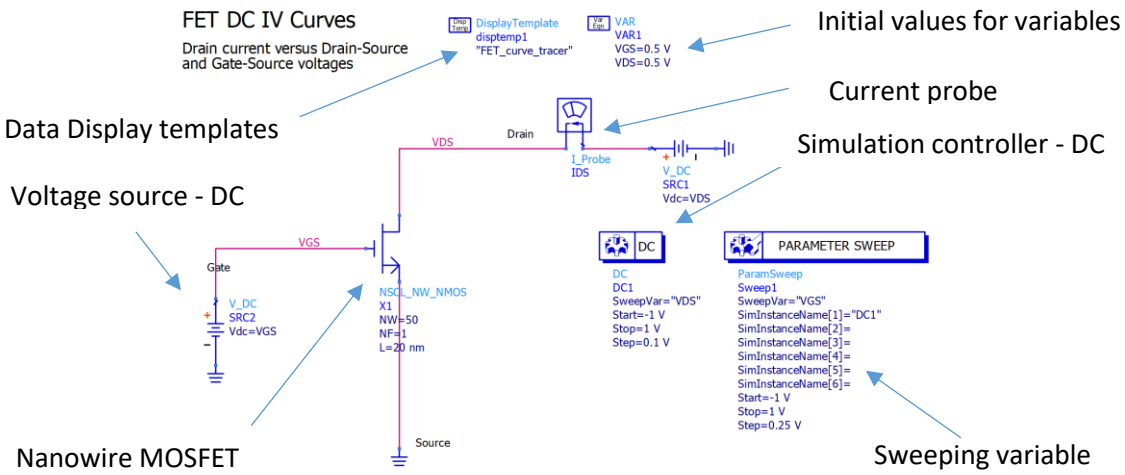
## Getting Started

Create a project workspace, based on ADS start-up assistance (separate document). Link the Nanoelectronics Student Component Library (NSCL) to your project workspace.

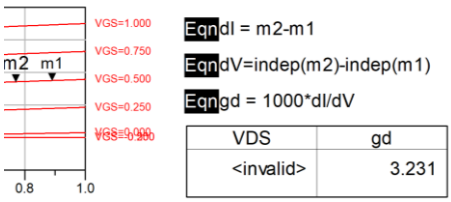
In library view, under '*Read-Only Libraries*' you will find *NSCL_lib* library which contains necessary components as well as test benches

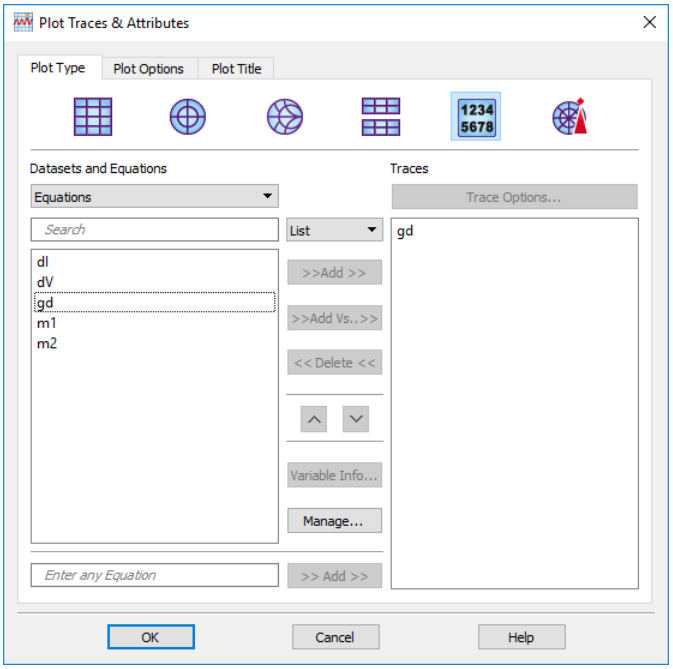
## Task 1: NW MOSFET DC characterization

For characterizing NW MOSFET device, we use pre-defined testbench circuits. Open "*NSCL_TB_NW_NMOS_OUTPUT*" and examine components present in the testbench, as shown in the figure below:




1. Set bias conditions as follows: $V_{GS}$ sweep from -0.5 to 1 [V] (0.25V step); $V_{DS}$ sweep from 0 to 1 [V] (0.01 V step). Press the cogwheel ('simulate') button to start simulation.
2. A data display window will appear, with pre-defined plots. Here, you will determine the output conductance of NW MOSFET ($g_d = {\partial I_D}/{\partial V_{DS}}\Big|_{V_{GS}}$). Difference in current and voltage can be achieved with use of markers in Data Display editor. Place markers on trace which corresponds to $V_{GS}$=0.5V and insert equations as shown in the figure below. Next, insert a list plot and display $g_d$ value (Datasets → Equations). What happens when you change number of wires? How big device do we need to get RF-matched (50Ω) output resistance?

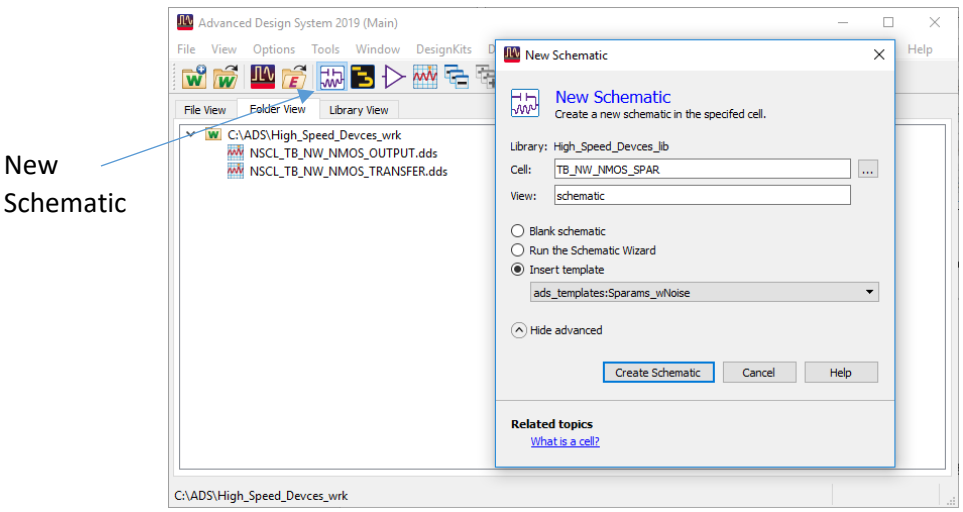


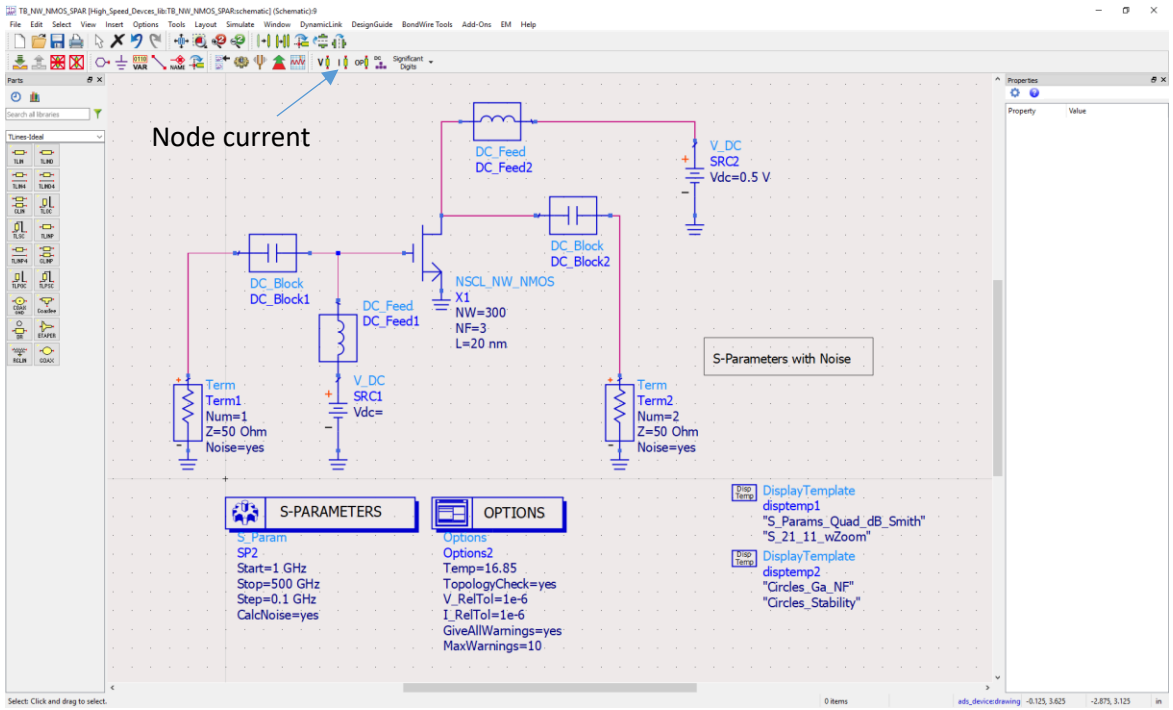

3. Open "*NSCL_TB_NW_NMOS_TRANSFER*". Set $V_{DS}$ to 0.5V (Delete Parameter sweep box), and $V_{GS}$ sweep from -0.5 to 1V (0.01 V step). Repeat the same procedure in data display, but this time locate the peak transconductance ($g_m = {\partial I_D}/{\partial V_{GS}}\Big|_{V_{DS}}$). What is the minimum $V_{GS}$ for which we achieve peak $g_m$?
4. Discuss your results with the TA

## Task 2: S-parameter characterization

To determine MOSFET RF properties, we will built an s-parameter testbench. Build a new schematic by clicking on button as shown in the figure below. Insert the schematic name ("*TB_NW_NMOS_SPAR*"), and under '*Show advanced*' tab, insert template, as shown in the figure [ads_templates:Sparams_wNoise]. Confirm with '*Create Schematic*'.



A window will appear with pre-defined components, simulation controllers and template files. Build a circuit by inserting NW MOSFET into the schematic, as well as voltage sources and bias routes for DC and RF signals, as shown in the figure below. Using hotkey "I" and typing the name of the component will allow you to insert the component directly into the schematic. DC_block and DC_feed components can be found in the *Lumped Components* palette, while voltage sources can be found in *Sources-Time Domain* palette. For placing wires and grounds consult start-up assistance. The final schematic is shown below.




1. In S-Parameters controller set start frequency 1 GHz, and stop frequency 500 GHz. In order to bias the MOSFET, set $V_{DS}$ to 0.5V, and $V_{GS}$ to minimum value that gives the peak transconductance. Select 300 wires, organized into 3 gate fingers. After pressing the cogwheel ('simulate') button, a Data Display window appears with four pages.
2. On page "*S_Params_Quad_dB_Smith*" place markers on all s-parameters and set frequency value to 100GHz. Read impedance and gain values. On page "*Circles_Ga_NF*" find marker named "*FreqCGN*" and set it to 100GHz. Read corresponding maximum gain and minimum noise figure values from corresponding list boxes.
3. Reduce $V_{GS}$ further to achieve minimum noise figure. Compare DC current from previous and new case (Click on Node current to see current in each node in the circuit). What is the reduction in power dissipation ($P_{DC}=V_{DS}\times I_D$)? How much gain in lost at 100GHz? Read the optimum impedance for which we can get minimum noise figure ($Z_{opt}$).
4. Discuss results with your TA

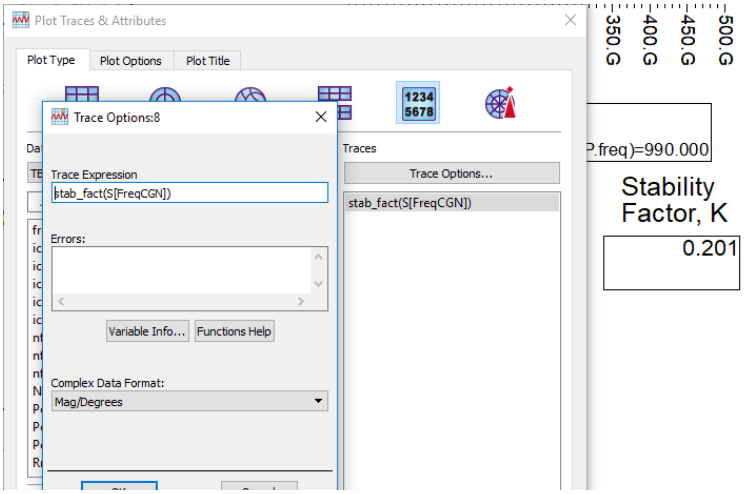
## Task 3: Number of wires and number of gate fingers

To further optimize NW MOSFET for operation at 100 GHz, we need to minimize the device size. At the same time, we need to adapt $Z_{opt}$ and $Y_{22}$ for 50Ω – operation. So far, simulated device has 3x100 wires (300 nanowires organized into 3 fingers).

1. Reduce number of wires to 240, while keeping the number of gate fingers the same (we now have 3x80 configuration). Read $Z_{opt}$. Continue reducing number of wires in steps of 30 wires,

until you have reached approximately real($Z_{opt}$)= 50Ω ± 5Ω. Note the changes in power dissipation, noise figure, and gain of the device.

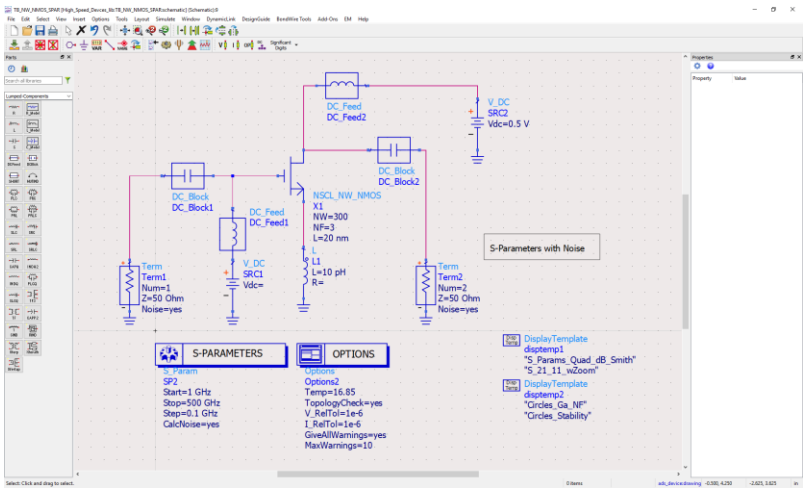
2. Change number of gate fingers to 2. What happened to $\Gamma_{opt}$? Open page "*Circles_Stability*". Here we can see stability analysis of our NW MOSFET. In the list “Stability Factor, K” under Traces, double click on the expression for stability factor. Change the expression to “stab_factor(S[FreqCGN])”, as shown in the figure below. What value is displayed? What value should K have in order to consider the device unconditionally stable?




3. Change number of gate fingers to 4. How did K change? Compare gain and noise of the device with the previous case.
4. Discuss your results with the TA

## Task 4: Stabilization

To complete our device design task, we need to ensure unconditional stability of the device. There are many ways to stabilize the transistor. Here we will attempt stabilization through inductive source degeneration.



1. Place an inductor in series with the source lead, and set the value to 10pH, as shown in the figure above. Gradually increase the inductance until the device is unconditionally stable at 100 GHz. What is the gain of the device after stabilization?
2. Discuss your results with the TA.