High-speed electronics HT2019 – Exercise 3

"Transistor AC and Noise"

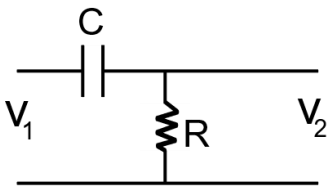
1. Consider an NQS InGaAs FET with C_{GS}=10fF, g_m=20 mS, R_g=5Ω and $\gamma = 1$.
   a. Calculate the minimum noise figure and optimum noise impedance for f=10 GHz and f=94 GHz.
   b. If the transistor is connected directly to a 50Ω source. What is the corresponding noise figure, NF_{50}?
   c. Estimate the smallest voltage signal that the transistor can accurately amplify (when connected to a very low impedance voltage source), assuming a low frequency ($\omega RC \ll 1$) signal bandwidth of Δf=1MHz.
   d. A 50Ω resistor is placed in parallel to C_{GS}. What is the minimum noise figure (at $f \approx 0\ Hz$) for this device augmented with the 50Ω resistor? Adding resistances to the device input is typically *NOT* a good idea in terms of noise performance!

2. Calculate C_{GS} (fF/μm) per unit gate width (in saturation) for HEMTs with channels of
   a) InAs
   b) $In_{0.53}Ga_{0.47}As$
   c) GaN

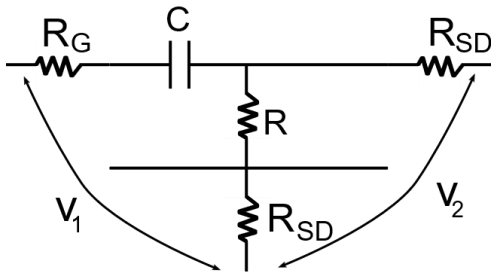
   Assume L_g=20 nm, t_w=8 nm, t_{ox}=5 nm, ε_{rox}=25.

   d) Which device of a-c should have the highest I_{DS} given that there is no scattering?

3. Given the following circuit,



   a) Calculate the y-parameter matrix
   b) Calculate the z-parameter matrix from the y-matrix
   c) Now add parasitic resistances to the system (as shown below) and calculate the z-matrix of the full system. Assume $R_{SD} = R_G/2 = R$.



   d) Transform the circuit into a hybrid-π model.