High-speed electronics VT2019 – Exercise 2

"Transistors DC"

1. An InAs (ε_r=14.6, m^*=0.023m$_0$) quantum well FET has t_{ox}=4nm, ε_{ox}=22 and t_w=6 nm.

   a) Calculate the total gate capacitance, including the contribution of band bending.

   b) Calculate the position of the two lowest bound states, assuming the infinite well approximation.

2. Show that the total 1D gate capacitance for a quantum well FET can be written as $C_G = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}+\Delta t}$. Determine Δt for the FET from (1).

3. The device in (1) is biased with V_{GS} -V_T = 0.3 V. Assuming degenerate conditions, calculate:

   a) $V_{DS,sat}$

   b) $I_{DS,sat}$

4. You will here demonstrate that for a 2D ballistic FET there is an optimal m*.

   a) Show in saturation that $I_{DS} \to 0$ if m* is very large or very small.

   b) Obtain an expression for $\frac{\partial I_{DS}}{\partial m^*}$ for the $i_{DS,sat}$ assuming degenerate conditions.

   c) Set $\frac{\partial I_{DS}}{\partial m^*} = 0$, and show that the optimal m* is a function of C'_{ox}.

   d) What is the optimal m* for the FET in (1)?

5. The device in (1) has Source/Drain contacts with the following dimensions (L_c x W) 100 nm x 500 nm, located at a 50 nm distance from the gate electrode. The specific contact resistivity is ρ_σ= 1 x 10^{-8} Ωcm^2. The doping level in the S/D regions is n = 5 x 10^{19} cm^{-3} and μ = 4000 cm^2/Vs.

   a) Calculate the transfer length of the contact. Can one assume a vertical contact?

   b) What is the contact resistance of the contact?

   c) How large are the access resistances?

   d) How much will the total added series resistance reduce the measured saturation current of the transistor in (1)?