

High-speed Electronics 2019 – Exercise 1

"Basic Properties"

- Calculate $E_F - E_C$ for a 3D $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ at $N_d = 10^{16}, 10^{18}$ and 10^{19} cm^{-3} for $T = 300\text{K}$.
 - Calculate the number of holes at each N_d from $E_F - E_V$.
 - Calculate $n_0 p_0$ and compare with the mass action law. When is the mass action law valid?
- To describe the carrier concentration in a semiconductor one can use the Fermi-Dirac integral: $F_j(\eta_F) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{x^j dx}{1+e^{x-\eta_F}}$, where the order $j = D/2 - 1$ is given the dimensionality $D = 0, 1, 2, 3$ of the system, while $\eta_F = (E_F - E_C)/k_B T$. Assuming GaAs with $E_F - E_C = 0.1 \text{ eV}$, use this integral to calculate
 - $n_{1D} = N_{1D} F_{-\frac{1}{2}}(\eta_F)$
 - $n_{2D} = N_{2D} F_0(\eta_F)$
 - $n_{3D} = N_{3D} F_{\frac{1}{2}}(\eta_F)$
 - Plot and compare n_{1D}/N_{1D} , n_{2D}/N_{2D} and n_{3D}/N_{3D} in the range $-10 < \eta_F < 10$. What is the general trend?
- A single subband 2D quantum well has $n_s = 3 \times 10^{12} \text{ cm}^{-2}$ at a low temperature. Obtain $E_F - E_1$ if the quantum well is made of
 - InAs, b) GaAs or c) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.
- For a double gate FET with an oxide thickness $t_{ox} = 2 \text{ nm}$ and $L_g = 10 \text{ nm}$ – estimate the thickest quantum well that can be utilized with reasonable small short channel effects? You can assume $\epsilon_r = \epsilon_{ox} = 12$.
- For a single subband $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ quantum well FET with $t_{well} = 5 \text{ nm}$, $t_{ox} = 2 \text{ nm}$ ($\epsilon_{ox} = 20$),
 - Calculate the oxide capacitance
 - Calculate the quantum capacitance
 - Calculate the total gate capacitance
- A single subband quantum well FET has an effective mass m^* and a high-k dielectric with thickness t_{ox} and dielectric constant $\epsilon_r = 25$.
 - Ignoring effects due to band bending inside the quantum well, derive an expression for the total gate capacitance, C_G .
 - For GaN ($m^* = 0.20m_0$) plot C_G as a function of $0.1 < t_{ox} < 10 \text{ nm}$.
 - For InAs ($m^* = 0.023m_0$) plot C_G as a function of $0.1 < t_{ox} < 10 \text{ nm}$.
 - Calculate C_G / C_{ox} for GaN and InAs as function of t_{ox} and compare the two materials. In which material is the gate stack most scalable? Why is this?