Written Exam High Speed Devices, April 7 2018.

Constants:

$$\hbar = 1.055 \times 10^{-34}\, Js$$
$$k_B = 1.38 \times 10^{-23}\, \frac{J}{K}$$
$$m_0 = 9.109 \times 10^{-31}\, kg$$
$$\epsilon_0 = 8.85 \times 10^{-12} Fm^{-1}$$
$$e = q = 1.602 \times 10^{-19} C$$

1)

A quantum well ($t_w = 7nm$) MOS ($t_{ox} = 5\ nm, \epsilon_{ox} = 15$) structure has a sheet carrier density $n_s = 1.25 \times 10^{12} cm^{-2}$ from Hall measurements.

a) The device capacitance is measured to be 0.1147 F/m2, what is m^*.
b) What is the Fermi level position?
c) If $T \approx 0$K, what is the largest group velocity of an electron confined in the quantum well?
d) Since T≈0K, the systems lacks any thermal energy. Explain why the velocity obtain in c) >> 0?

2)

a) For a ballistic FET - why does the current increase exponentially $e^{q(V_{gs}-V_T)/kT}$ for $V_{GS} << V_T$
b) For a ballistic FET - why does the current increase super linearly $\left(V_{gs} - V_T\right)^{1.5}$ for $V_{GS} >> V_T$
c) Explain why $C_q \rightarrow \frac{C_q}{2}$ for a ballistic device in saturation.

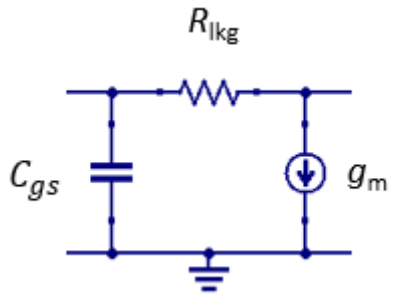
3)

A quasi-ballistic InGaAs FET (m^*=0.03m_0, ε_r=13) quantum well FET (t_w=7 nm) has t_{ox}=5 nm (ε_{rox}=15). The device width is 1 µm and L_g=30 nm.

a) Calculate the total gate capacitance in saturation.
b) Calculate the ballistic drain current in saturation when V_{GS}-V_T=0.5V.
c) Calculate the ballistic device transconductance at V_{GS}-V_T=0.5V.
d) If the transconductance is measured to be 3mS/µm, calculate the device mean free path (assuming that scattering is the only effect that lowers the current.)

4)

Due to a fabrication error, a transistor accuires a large gate-drain leakage. The simplest equivavelent model is then as shown below.



a) Derive an expression for the current gain.
b) Derive an expression for the maximum stable gain.
c) Derive an expression for the highest frequency where power amplification is possible.

5)

A 50Ω source is connected to a 50Ω ($\varepsilon_{r,eff}$=4) waveguide environment. A transistor is connected to the source to build a single stage LNA. The transistor has an optimum noise impedance at *f*=50GHz given by $Z_{opt} = 100 + 200j$.

a) Design an input matching network, which minimizes the noise of the amplifier using one discreet (L/C) and one waveguide component.
b) What is the minimum noise figure, if γ=1 and g_m=20mS and R_g=10Ω and f_T=300 GHz?
c) If the LNA is operated at *f*=60GHz with the same matching network – how will the noise figure be affected? Motivate your answer by considering two effects.